EEE 212
Microprocessors

Syllabus

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Syllabus

Assistants:
Namik Sengezer, Room: EA 226Tel: x1613 (coordinator assistant)
Laboratory WEB page:
http://www.ee.bilkent.edu.tr/~ee212/lab
Homework WEB page:
http://www.ee.bilkent.edu.tr/~ee212/homework

Textbook:

- M. A. Mazidi & J. G. Mazidi, "The 80x86 IBM PC and Compatible Computers", Prentice Hall,2000.
- **Useful Books:**
- K.R. Irvine, "Assembly Language for Intel Based Computers", Prentice Hall,1999.
- Antonakos, "An Introduction to the Intel Family of Microprocessors", Prentice Hall, 1999
- W. A. Triebel and A. Singh, "The 8088 and 8086 Microprocessors: Programming, Interfacing,
  Software, Hardware, and Applications" Prentice Hall, 2000.
- Brey, "The Intel Microprocessors", Prentice Hall, 2000
- D. W. Smith, "PIC in practice: An introduction to the PIC microcontroller", Butterworth-Heinemann, 2001
- Art of Assembly Language Programming, http://webster.cs.ucr.edu/Page_AoAWin/aoapdf.zip
- V. Heuring, H. Jordan Computer Systems Design and Architecture , Addison Wesley

- **Computer Usage:**
  Microsoft's Macro Assembler, Debugger, and Conventional High Level Programming languages in the PC environment.
- **Prerequisites:**
  Logic circuits, digital design
  Number representations and basic computing algorithms
- **Grading (tentative):**
  - **Midterm:Essay/written -- 30 %**
    - One Midterm: March 20th 5:40-
      –Closed book
  - **Final:Essay/written -- 35 %**
  - **Labwork -- 20 %**
  - **Quizzes -- 15 %**
    - A grade (e.g., B+ to B) is lowered if the students attend less than 70% of the time unless the grade is an A

Labs and Policy

- Three of the labs are introduction labs; these labs will **not** be graded.
- For each of the remaining five labs, there will be a quiz at the start of the lab and an assignment which must be completed before coming to the lab.
- All students are required to attend all lab sessions. Unattending a session without a valid excuse(medical report) has a penalty of 10% decrement per unattended session from the overall lab grade, in addition to getting a zero for the grade of that lab.
- **By registering with this course it is assumed that you fully understood and will obey the Bilkent University Policy on Academic Honesty**

Schedule

WEEK(1): Introduction to Microcomputers and Microprocessors,Computer Codes, Programming and Operating Systems

WEEK(2): 80x86 Processor Architecture, registers, addressing

WEEK(3): 8088/8086 Instruction Set, Machine Codes, Addressing Modes, Debug

WEEK(4): 8088/8086 Microprocessor Programming, sw interrupts

WEEK(5): 8088/8086 Microprocessor Programming , arithmetic logic instructions

WEEK(6): 8088/8086 Microprocessor Programming, advanced prog.

Schedule

WEEK(7): 8088/8086 Microprocessor Programming, memory interfacing
WEEK(8): The 8088 and 8086 Microprocessors and Their Memory and Input/Output Interfaces,

WEEK(9): IO devices, PIA, 8255 and AD DA converters

WEEK(10): IO devices, PIA, 8255 and AD DA converters
WEEK(11): IO devices, PIA, 8255 and AD DA converters

WEEK(12): An Introduction to PIC(8051) microcontrollers Interrupts and Interfaces

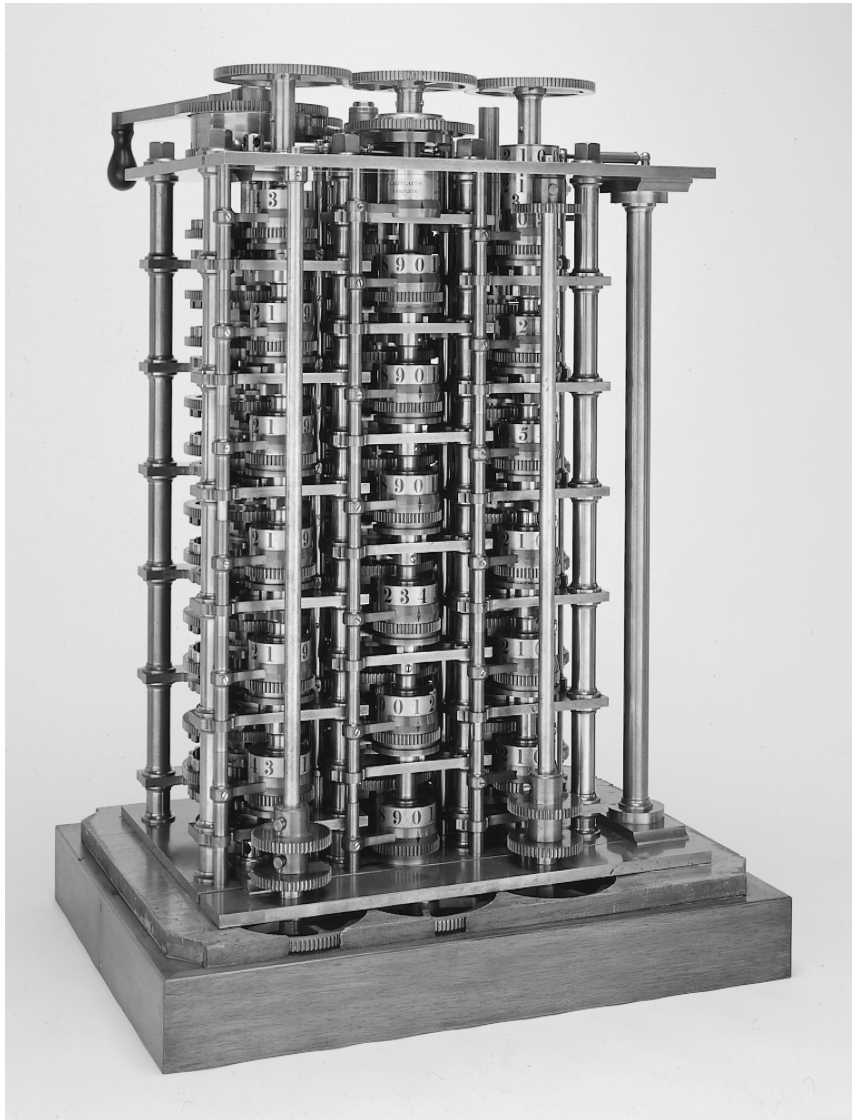
WEEK(13): An Introduction to PIC(8051) microcontrollers

WEEK(14): Programmable Interrupt Controller (8259)

Week 1

Introduction to Microcomputers and Microprocessors, Computer Codes, Programming, and Operating Systems

First Computer



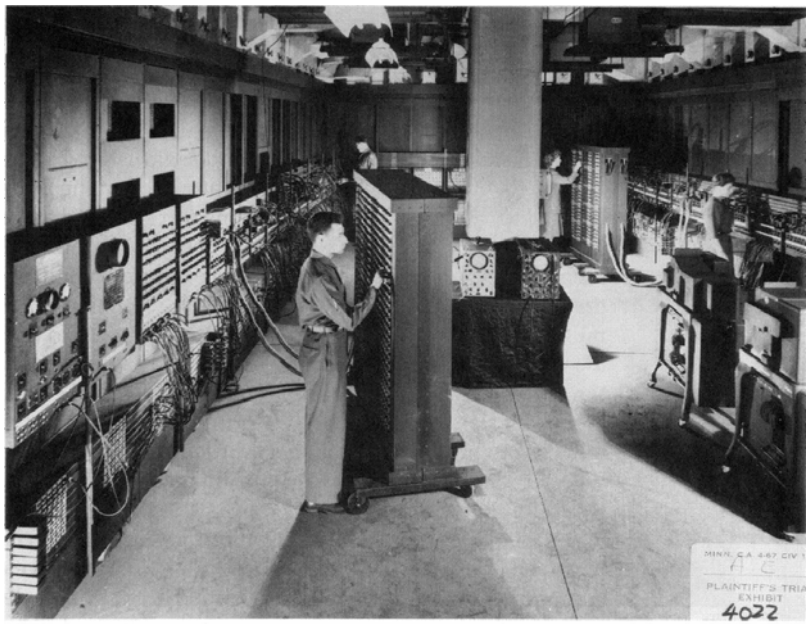
•It all started with the 1832 Babbage mechanical machine to calculate the navigation tables for the Royal Army, U.K.

The Babbage Difference Engine (1832)

25,000 parts

cost: £17,470

ENIAC



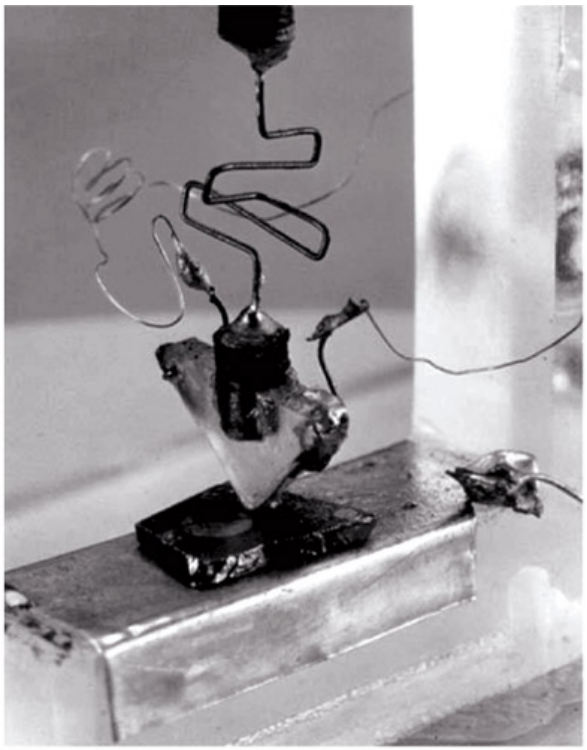
- Vacuum tube based
- "BIG BRAIN"
- ENIAC

–1,800 sq. Feet area
–30 ton
– 18000 vacuum tubes

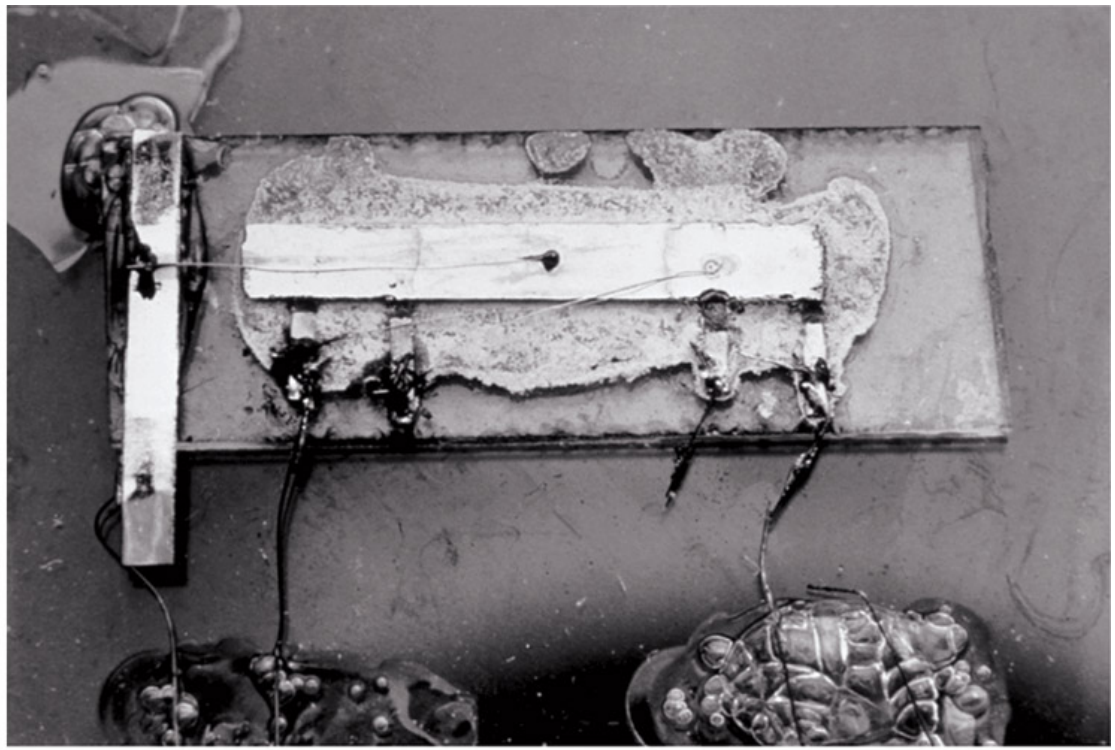
- Application: IInd WW

1943 First electronic computer is used to decode the German Army secret codes, coded by the Enigma machine: Colossus,
1946 First General Purpose computer: ENIAC 17000 vacuum tubes, 500 miles of wire 30 tons, 100 000 ops per sec.@ U.of Penn

First Transistor



(a)

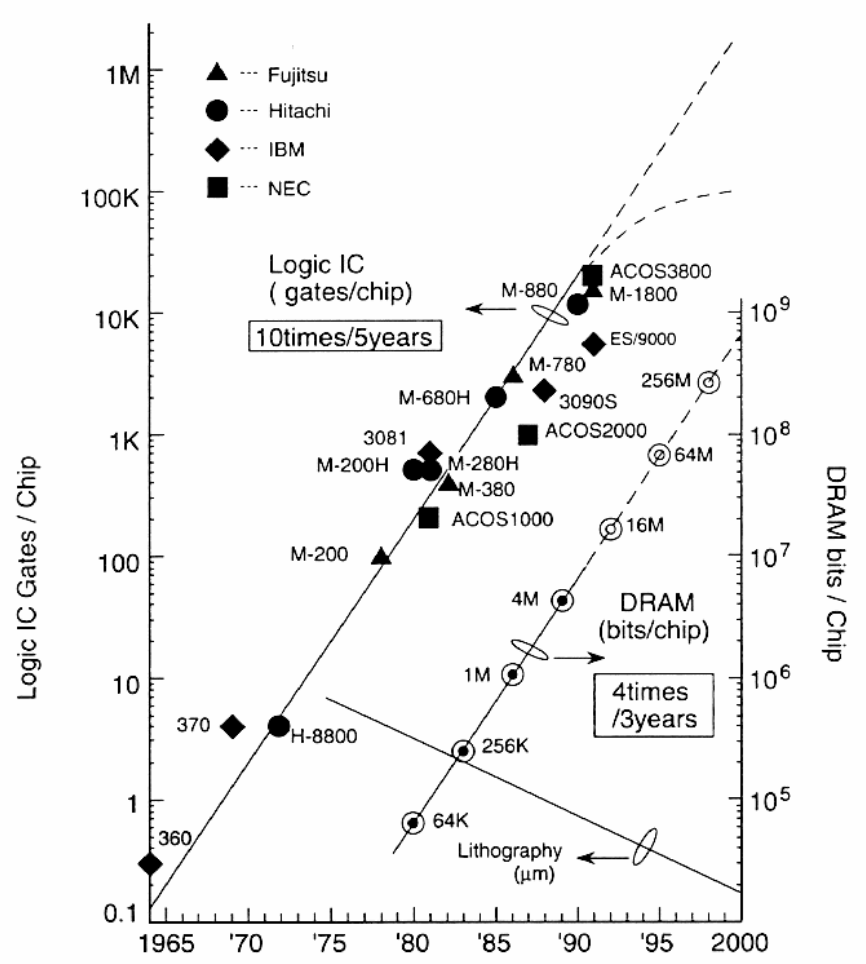


(b)

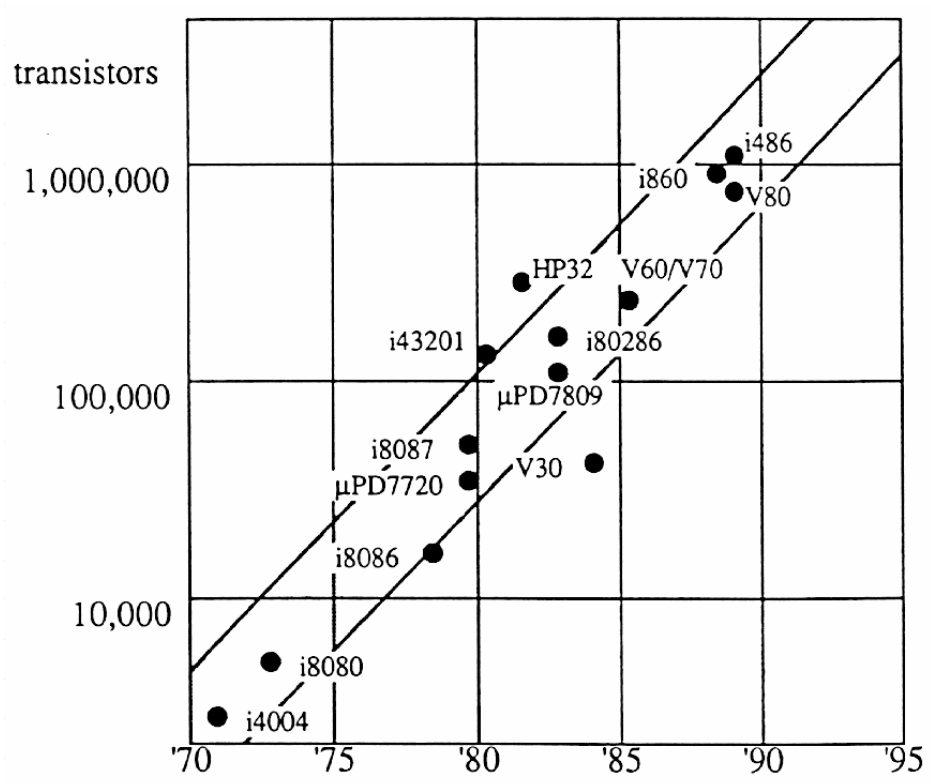
FIG 1.2 (a) First transistor (Courtesy of Texas Instruments.) and (b) first integrated circuit. (Property of AT&T Archives. Reprinted with permission of AT&T.)

Bell Labs 1946

Change over the years

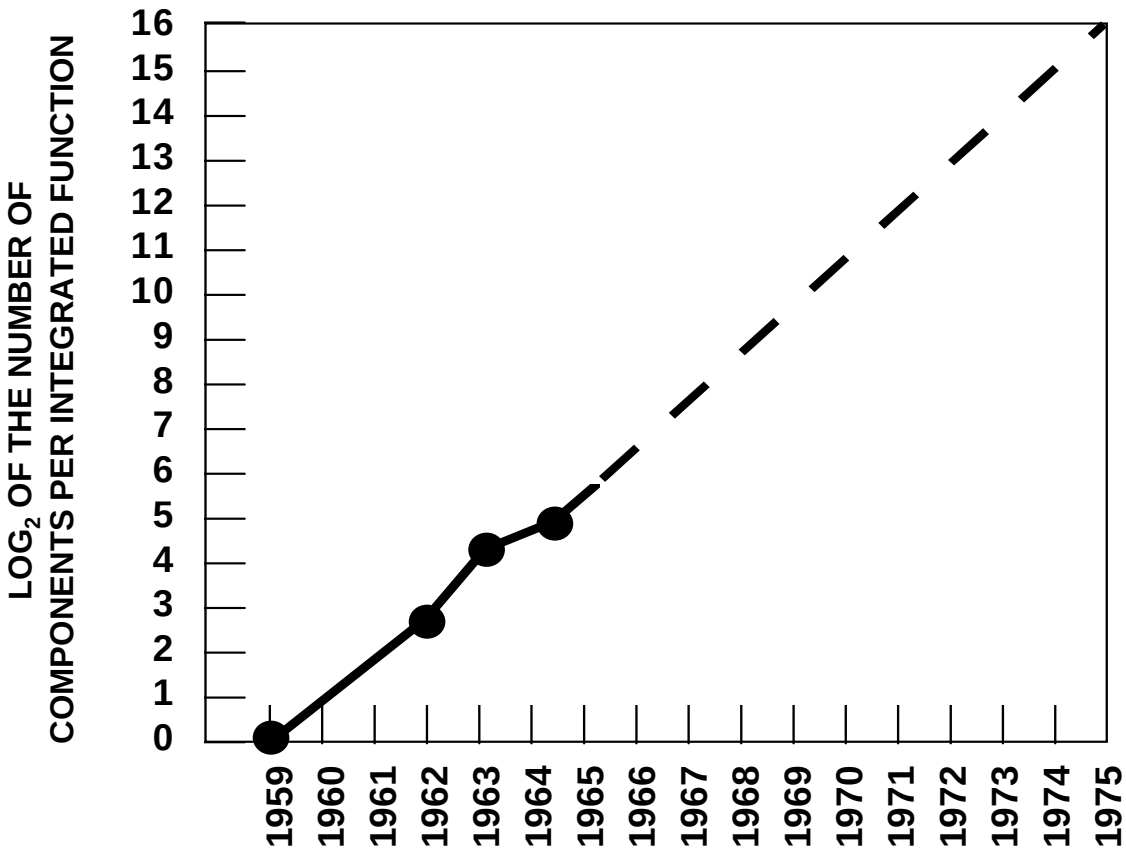


Change in Complexity



Change in Transistors

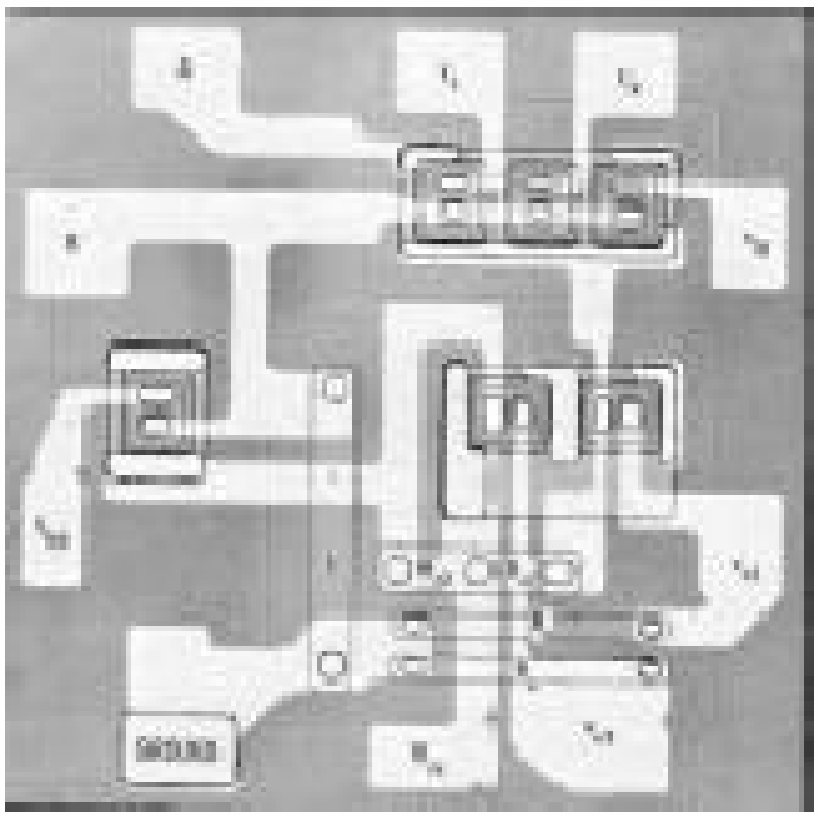
Moore's Law



Intel's Founder Gordon Moore 19 April 1965, Electronics

First IC

•1958 Invention of the IC by Jack Kilby at Texas Instruments



Bipolar logic
1960's

ECL 3-input Gate
Motorola 1966

A brief history

- First microprocessor at Intel in 1971--- 4004
- Intel 4004 was a 4 bit up. Only 45 instructions P Channel Mosfet technology. 50 K instructions per second (< ENIAC!).
- Later 8008 as an 8 bit µ processor then 8080 and Motorolla 6800.
- 8080 was 10x faster than 8008 and TTL compatible (easy interfacing)
- MITS Altair 8800 1974. The BASIC Interpreter was written by Bill Gates. Assembler program was written by Digital Research Corporation (Author comp. Of Dr-DOS)
- 1977 8085 microprocessor. Internal clock generator, higher frequency at reduced cost and integration. There are 200 million 8085's around the world!
- 1978 8086+8088 microprocessors 16 bit. Addressed 1 Mbyte of memory. Small instruction cache (4-6 bytes) enabled prefetch of instructions.
- IBM decided to use 8088 in PC.

A brief history

- In 1983 80286 released, identical to 8086 except the addressing and higher clock speed.
- 32 bit microprocessor era. In 1986 major overhaul on 80286 architecture → 80386 DX with 32bit data + 32 bit address (4 G bytes)
- 1989 80486 = 80386 +80387co processor + 8KB cache
- 1993 Pentium (80586). Includes 2 execution engines.
- Pentium Pro included 256K Level 2 cache mechanism as well as Level 1 cache. Also 3 execution engines which can execute at the same time and can conflict and still execute in parallel. The address bus was expended to 36.
- Pentium 2 included L2 cache on its circuit board (called slot)
- Later Pentium 3 and 4 released with several architectural and technological innovations.

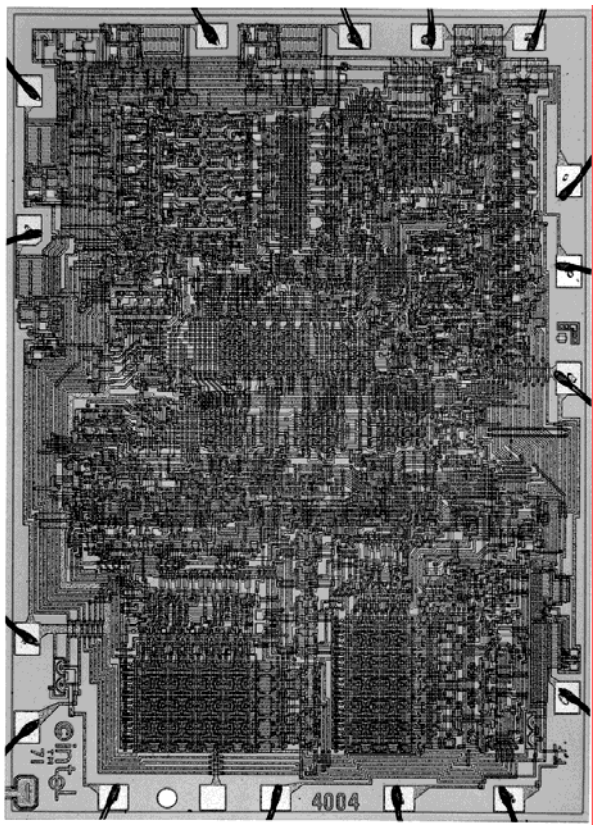
Evolution of Intel Microprocessors

Processor	Codename	Year Introduced	Transistors	Minimum Feature Size (microns)	Package	Socket or Slot	Core/Bus Frequency (Max)[1]	External Data Bus Width	Internal Register Widths	Address Bus Width	NDP[2]	L1 Cache	L2 Cac
4004		1971	2,250	10.0	16 pin DIP		.108 MHz	4	8	12	none	none	nor
8008		1972	3,500	10.0	18 pin DIP		.200 MHz	8	8	14	none	none	nor
8080		1974	6,000	6.0	40 pin DIP		3 MHz	8	8	16	none	none	nor
8085[3]		1976	6,000	6.0	40 pin DIP		6 MHz	8	8	16	none	none	nor
8086		1978	29,000	3.0	40 pin DIP		10 MHz	16	16	20	external	none	nor
8088		1979	29,000	3.0	40 pin DIP		10 MHz	8	16	20	external	none	nor
80286		1982	134,000	1.5	68 pin PLCC or PGA[4]		12.5 MHz	16	16	24	external	none	nor
80386DX		1985	275,000	1.0	132 pin PGA or QFP[5]		33 MHz	32	32	32	external	none	exter
80386SX		1988	275,000	1.0	100 pin PQFP[7]		33 MHz	16	32	24	external	none	exte
80486DX		1989	1.2 million	0.8	168 pin PGA	Socket 3	50 MHz	32	32	32	on-chip	8 KB	exte
80486SX		1991	1.185 million	1.0	196 lead PQFP or 168 pin PGA	Socket 3	33 MHz	32	32	32	none	8 KB	exte
80486DX2		1992	1.2 million	0.6	168 pin PGA	Socket 3	66/33 MHz	32	32	32	on-chip	8 KB	exte
80486DX4		1994	1.2 million	0.6	168 pin PGA	Socket 3	100/ 33 MHz	32	32	32	on-chip	8 KB	exte
Pentium Classic	P5	1993	3.1 million	0.8	273 pin PGA	Socket 4, 5	66 MHz	64	32	32	on-chip	8/8 KB C/D[8]	exte
Pentium Classic	P54	1994	3.3 million	0.35, 0.5	296 pin PGA	Socket 7	200/66 MHz	64	32	32	on-chip	8/8 KB C/D	exte
Pentium MMX	P55	1997	4.5 million	0.25, 0.28	296 pin PGA	Socket 7	300/66 MHz	64	32	32	on-chip	16/16 KB C/D	exte
Pentium Pro	P6	1995	5.5 million[9]	0.35, 0.5	387 pin dual cavity PGA or PPGA[10]	Socket 8	200/66 MHz	64	32	36	on-chip	8/8 KB C/D	256, 1M

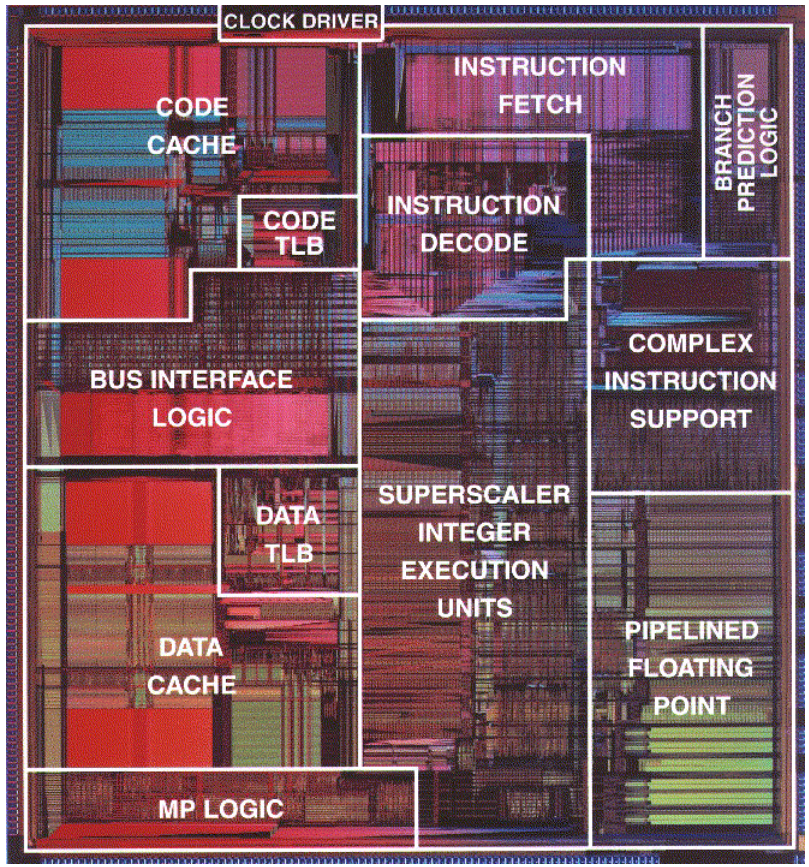
Pentium II	(Klamath) Deschutes[12]	(1997) 1998	7.5 million	(0.28), (0.25)	242 contact SEC cartridge	Slot 1	(233/66 MHz) 450/100 MHz	64	32	36	on-chip	16/16 KB C/D	512 KB[13]
Celeron	(Covington) Mendocino[14]	1998	(7.5 million) 19 million[15]	0.25	(242 contact SEP cartridge)	Slot 1	(300/66 MHz)						
					370 pin PPGA	Socket 370	466/66 MHz	64	32	36	on-chip	16/16 KB C/D	(external) 128 KB[16]
Pentium III	Katmai	1999	9.5 million	0.25	242 contact SEC cartridge	Slot 1	550/100 MHz	64	32	36	on-chip	16/16 KB C/D	512 KB[17]
					330 contact SEC cartridge	Slot 2							
	Coppermine	1999		0.18	370 pin PGA	Socket 370	733/133 MHz						256 KB[18]
Itanium[19]	Merced	2000		0.18			6XX/133 MHz	128	64	64	on-chip		256 KB[20]

[1]It is likely that higher frequency versions of the newer processors will be offered in the future.
[2]Numeric data processor (also called coprocessor or floating point unit).
[3]Improved 8080 with three new instructions to enable/disable three added interrupt pins. Simplified hardware with single +5 V power supply and on-board clock generator.
[4]Plastic leaded chip carrier or pin grid array.
[5]Quad flat package (QFP).
[6]Some 386 computers (and nearly all later processors) incorporated external L2 caches.
[7]Plastic quad flat package.
[8]Separate code and data caches are supplied
[9]On-board 256 KB L2 cache (separate silicon die) has 15.5 million transistors (31 million for 512 KB cache). 1 MB cache has two separate 512 KB die.
[10]Plastic pin grid array
[11]Separate die in package. Cache operates at core speed.
[12]Specifications for Klamath processor are shown in parentheses.
[13]Separate die in SEC package. Cache operates at one-half core speed.
[14]Specifications for the Covington processor are shown in parentheses. The Mendocino processor is also called Celeron A.
[15]Includes integrated 128 KB L2 cache.
[16]128 KB cache is on the same die with the processor and operates at the core frequency of the processor.
[17]Separate die operating at 0.5 times core speed (slot 1) or integrated with the processor operating at core speed (slot 2).
[18]Integrated with the processor and operating at core speed. Includes 256-bit (vs. 64 bit on previous chips) processor–cache data bus.
[19]Specifications for this processor have not yet been finalized by Intel.
[20]Integrated with the processor die and operating at full core speed.

Old and New



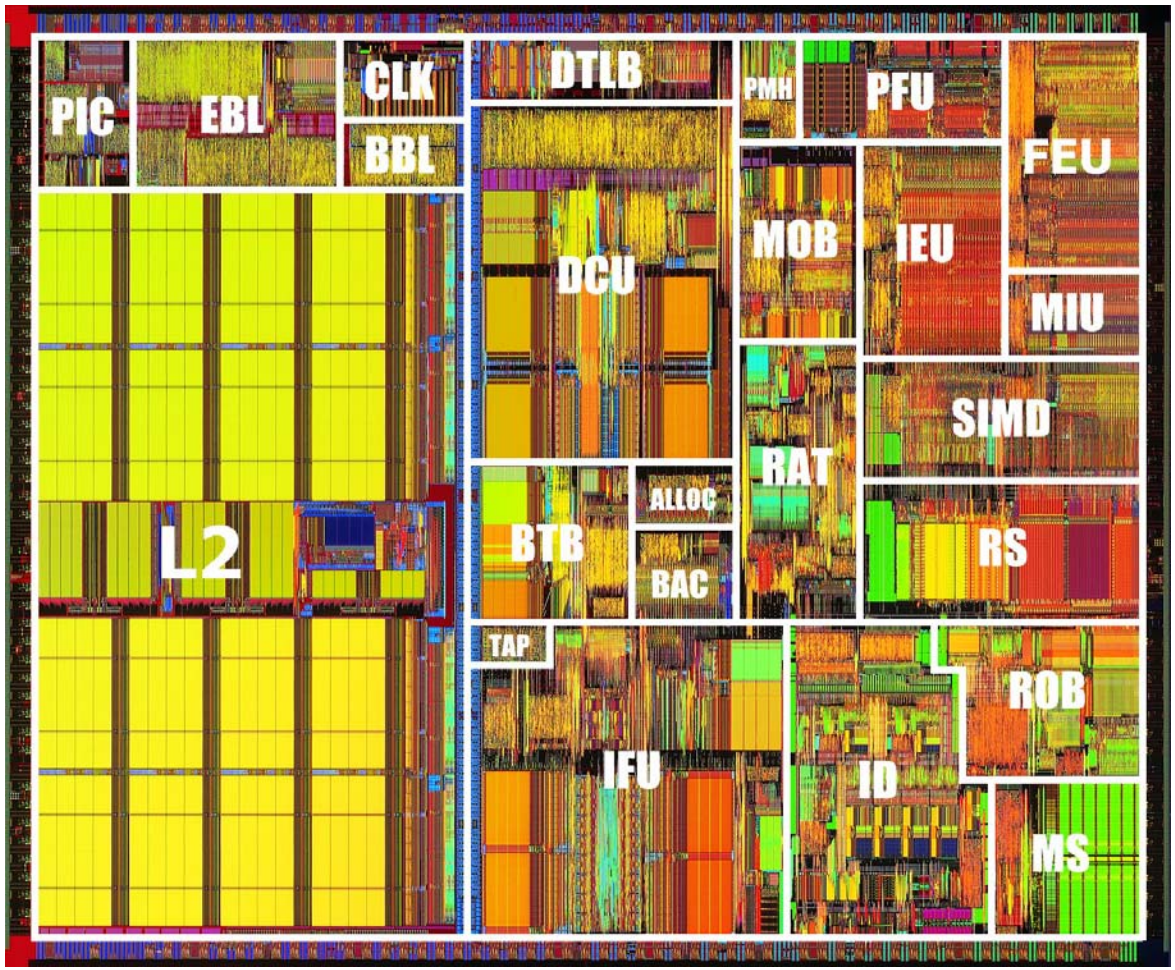
Intel 4004 Microprocessor



Intel Pentium Microprocessor

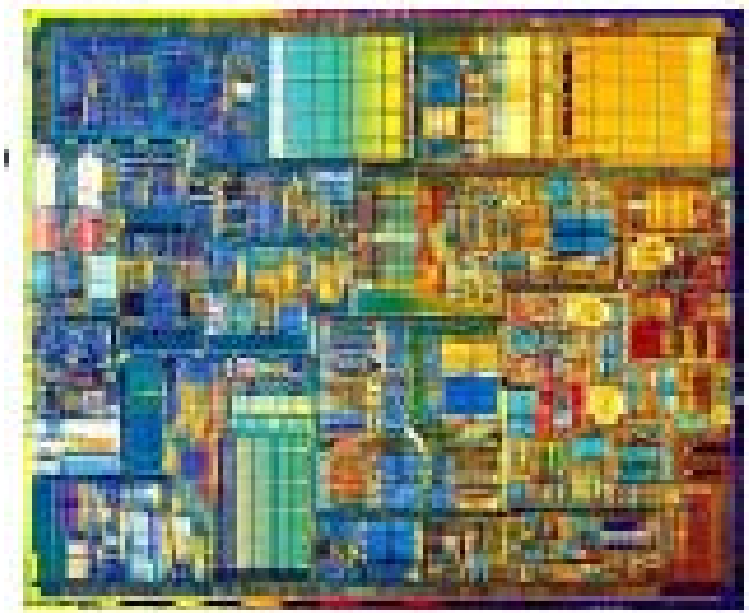
[Adapted from http://infopad.eecs.berkeley.edu/~icdesign/. Copyright 1996 UCB]

Pentium III



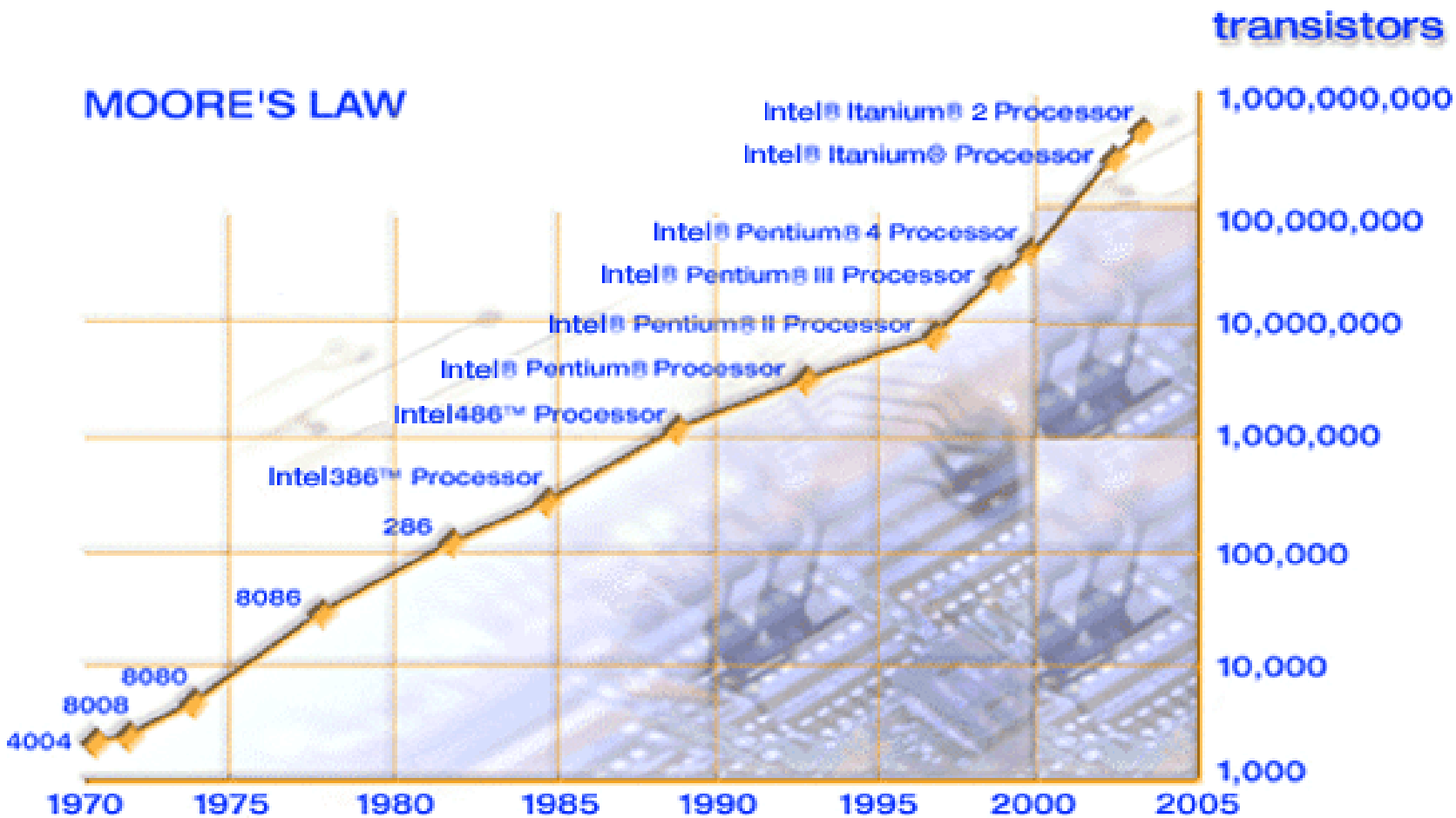
- Info
  - 28.1M transistors
  - 0.18 micron, 6-layer metal CMOS
  - 106 mm^2 die area
  - 3-way superscalar, 256K L2 cache, 133 MHz I/O bus

Pentium IV

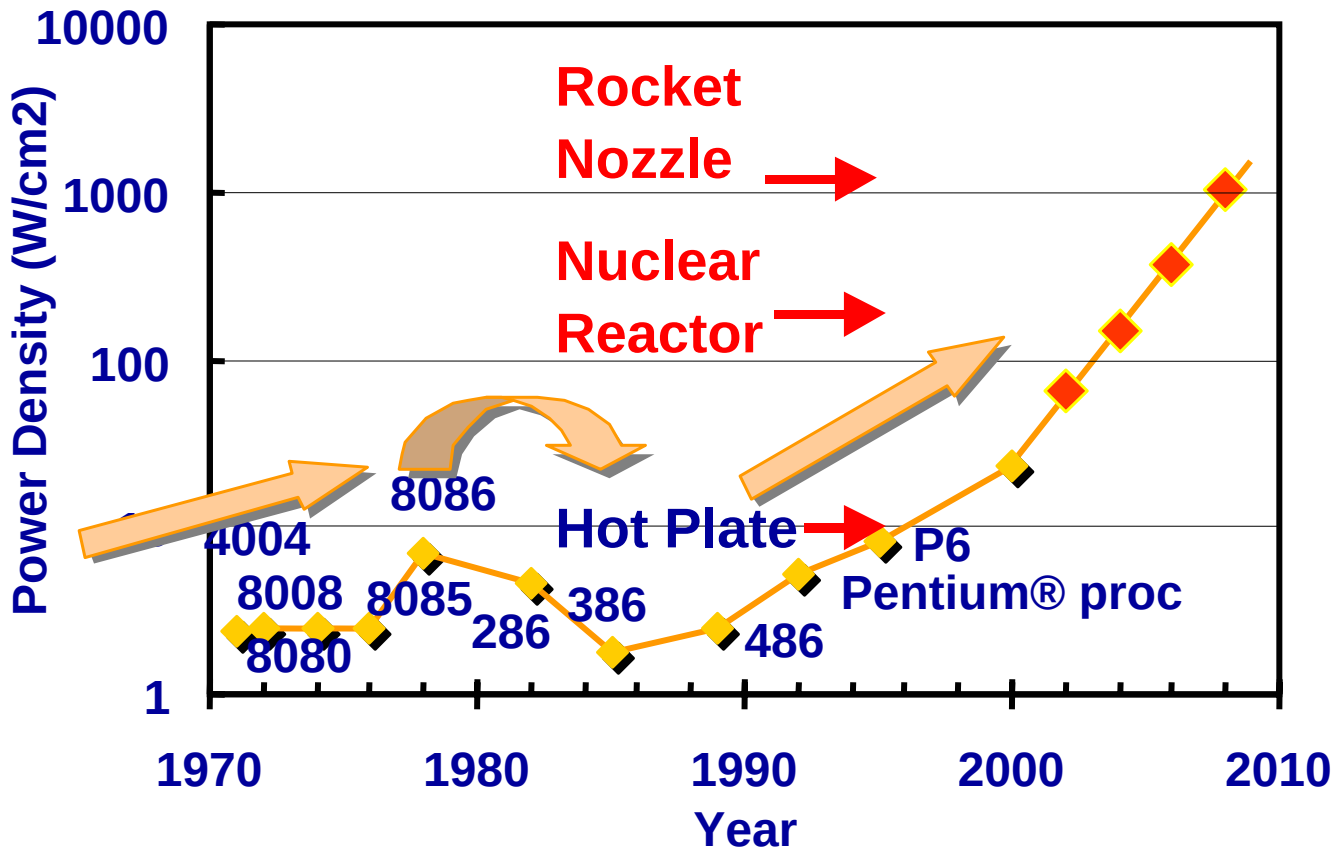


- **0.18-micron process technology (2, 1.9, 1.8, 1.7, 1.6, 1.5, and 1.4 GHz)**
  - Introduction date: August 27, 2001 (2, 1.9 GHz); …; November 20, 2000 (1.5, 1.4 GHz)
  - Level Two cache: 256 KB Advanced Transfer Cache (Integrated)
  - System Bus Speed: 400 MHz
  - SSE2 SIMD Extensions
  - Transistors: 42 Million
  - Typical Use: Desktops and entrylevel workstations
- **0.13-micron process technology (2.53, 2.2, 2 GHz)**
  - Introduction date: January 7, 2002
  - Level Two cache: 512 KB Advanced
  - Transistors: 55 Million

Change in Microprocessors



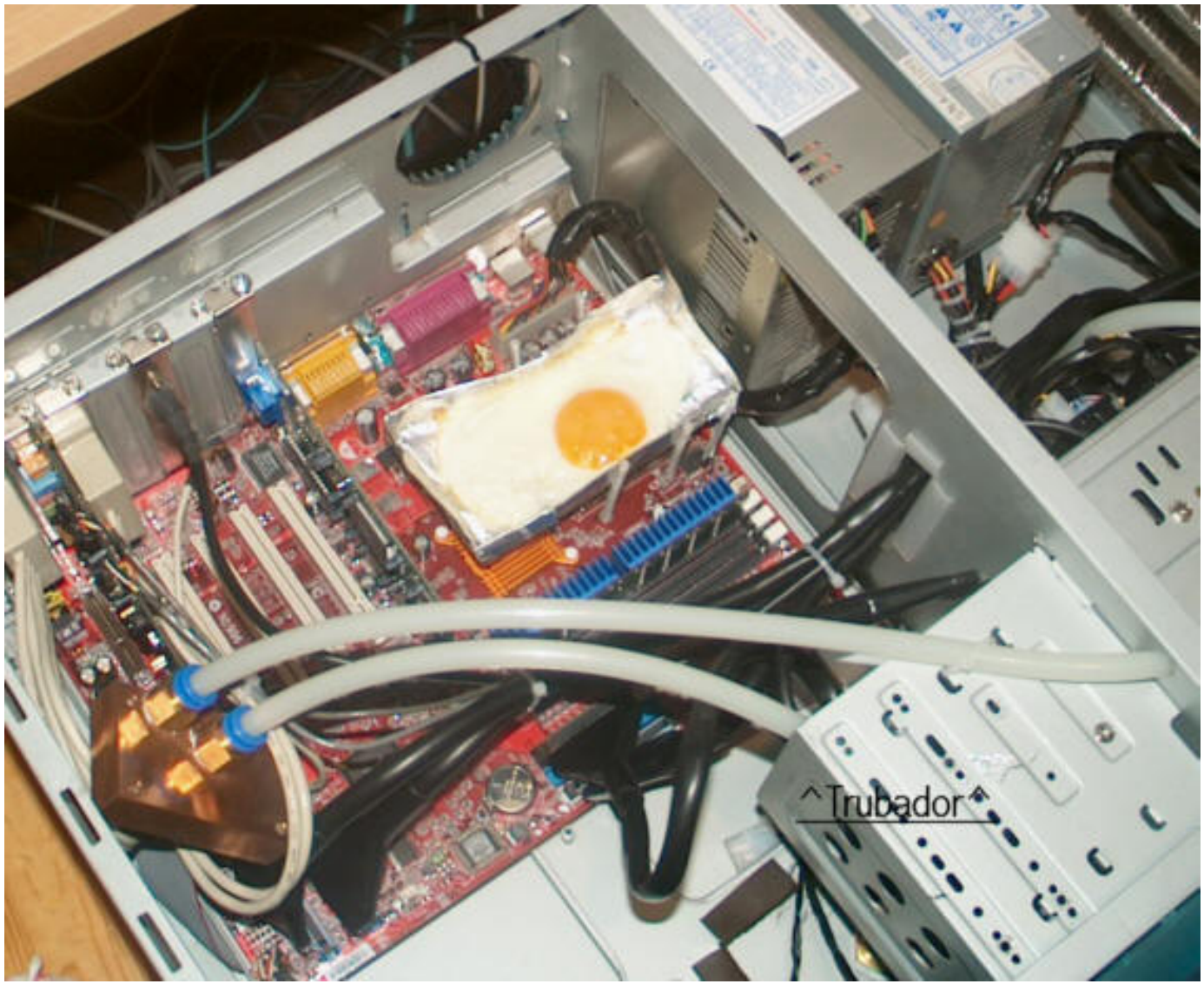
Power Density



Courtesy, Intel

Power Density increase

Power Density

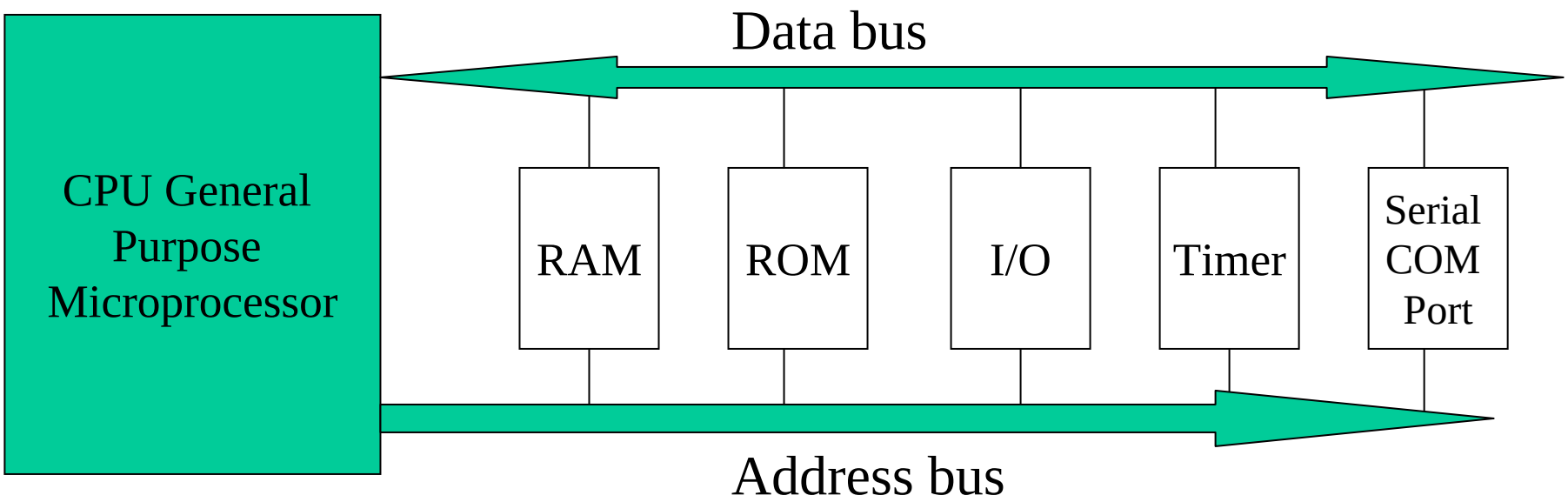


Types of Microcomputers

- *Microprocessor:* Processor on a chip
- In 1982, IBM began selling the idea of a *personal computer*. It featured a system board designed around the Intel 8088 8-bit microprocessor, 16 K memory and 5 expansion slots.
  - This last feature was the most significant one as it opened the door for 3rd party vendors to supply video, printer, modem, disk drive, and RS 232 serial adapter cards.
  - Generic PC: A computer with interchangable components manufactured by a variety of companies
- *Microcontroller* is an entire computer on a chip, a microprocessor with on-chip memory and I/O.
  - These parts are designed into (embedded within) a product and run a program which never changes
  - Home appliances, modern automobiles, heat, air-conditioning control, navigation systems
  - Intel's MCS-51 family, for example, is based on an 8-bit microprocessor, but features up to 32K bytes of on-board ROM, 32 individually programmable digital input/output lines, a serial communications channel.

General Purpose Microprocessors

Microprocessors lead to versatile products

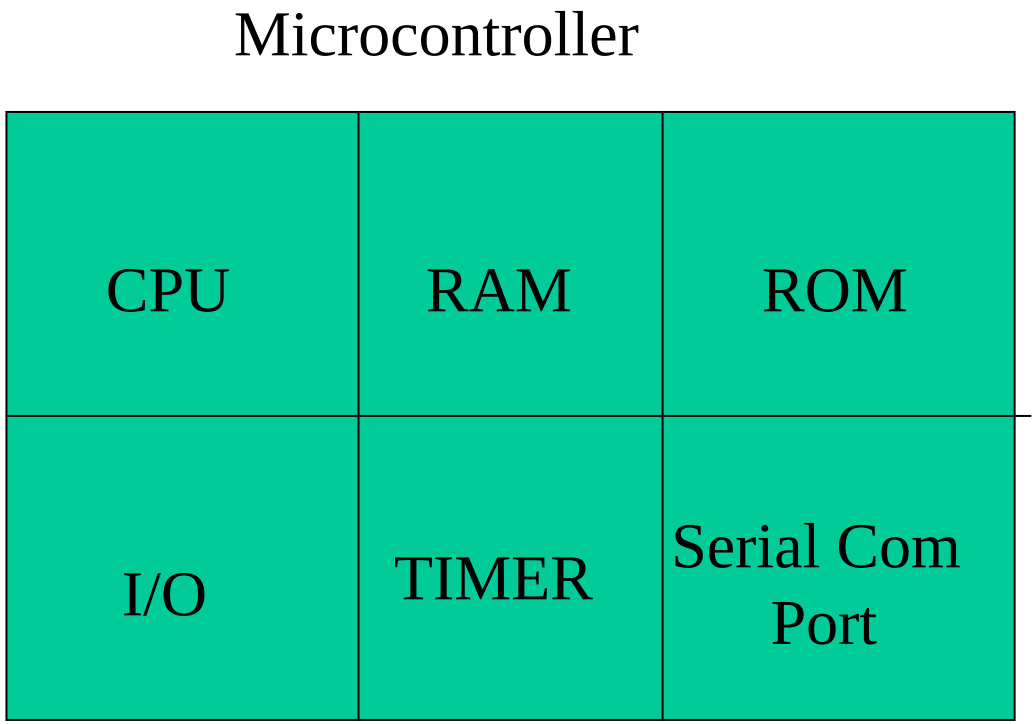


These general microprocessors contain no RAM, ROM, or I/O ports on the chip itself

Ex. Intel's x86 family (8088, 8086, 80386, 80386, 80486, Pentium)

Motorola's 680x0 family (68000, 68010, 68020, etc)

Microcontrollers



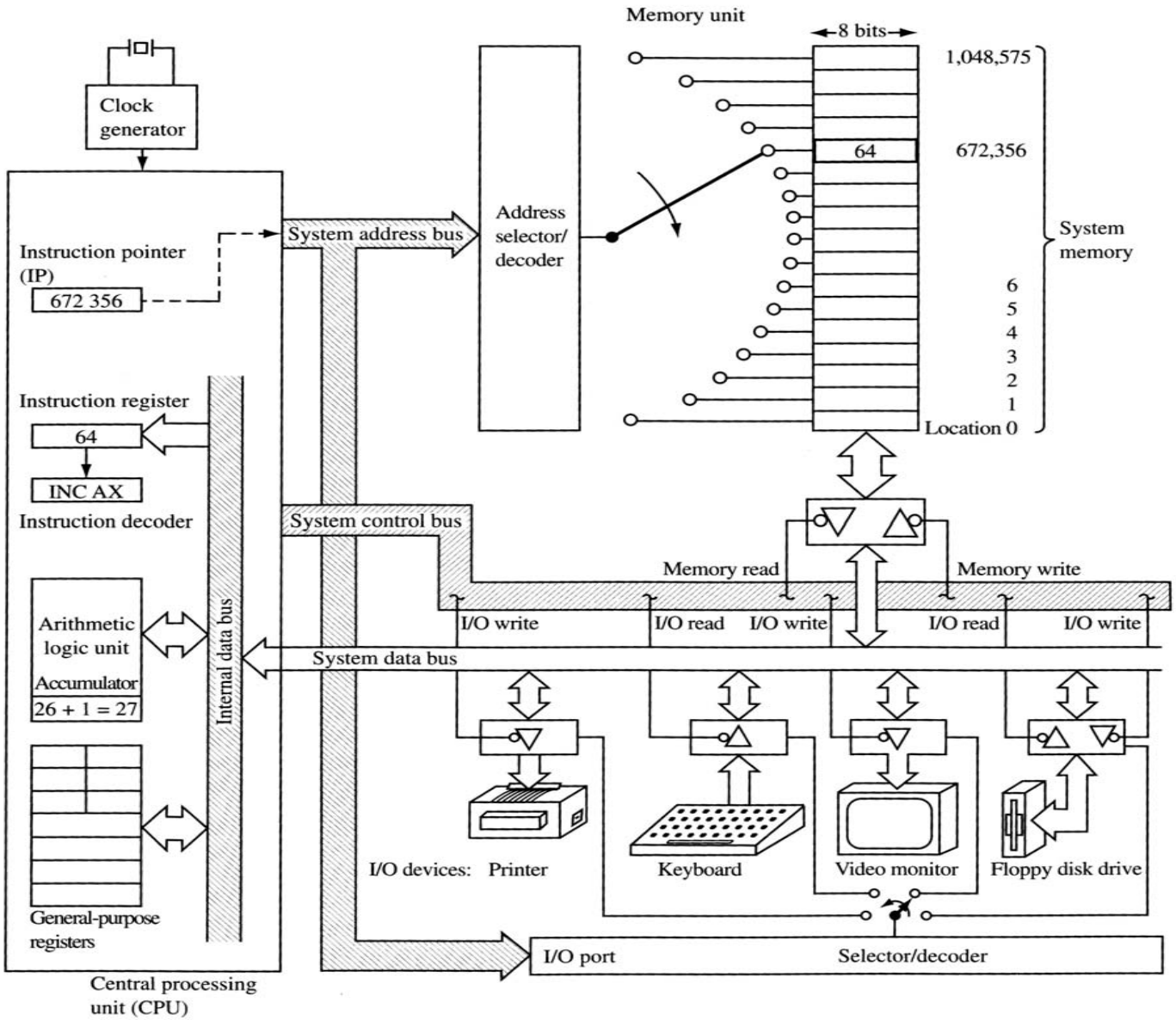
A microcontroller has a CPU in addition to a fixed amount of RAM, ROM, I/O ports on one single chip; this makes them ideal for applications in which cost and space are critical

Example: a TV remote control does not do computing power of a 486

Embedded Systems

- An embedded system uses a microcontroller or a microprocessor to do one task and one task only
  - Example: toys, garage door openers, answering machines, ABS, keyless entry, etc.
  - Inside every mouse, there is a microcontroller that performs the task of finding the mouse position and sends it to the PC
- Although microcontrollers are the preferred choice for embedded systems, there are times that the microcontroller is inadequate for the task
- Intel, Motorola, AMD, Cyrix have also targeted the embedded market with their general purpose microprocessors
- For example, Power PC microprocessors (IBM Motorola joint venture) are used in PCs and routers/switches today
- Microcontrollers differ in terms of their RAM,ROM, I/O sizes and type.
  - ROM: One time-programmable, UV-ROM, flash memory

Stored Program Concept



Stored Program Concept

- There are three major parts
  - The CPU (Central Processing Unit) which acts as the brain coordinating all activities within the computer
  - The Memory Unit where the program instructions and data are stored
  - The I/O (Input/Output) devices which allow the computer to input information for processing and then output the result
- Today the CPU circuitry has been reduced to *ICs* called the microprocessing unit (MPU) or the *microprocessor*, the entire computer with the three parts is called a *microcomputer*
- Several registers
- The basic timing of the computer is controlled by a square wave oscillator or a *clock* generator circuit.
  - Synchronization
  - Determines how fast the program can be fetched from memory and executed
- Memory Read or Fetch Cycle
  - IP: Instruction Pointer

Stored Program Concept

- Memory unit consists of a large number of storage locations each with its own address. As a Prime Memory it can be observed as:
  - RAM (Random Access Memory) and its volatility. *Typically 8 bit wide*
  - ROM (Read Only Memory)

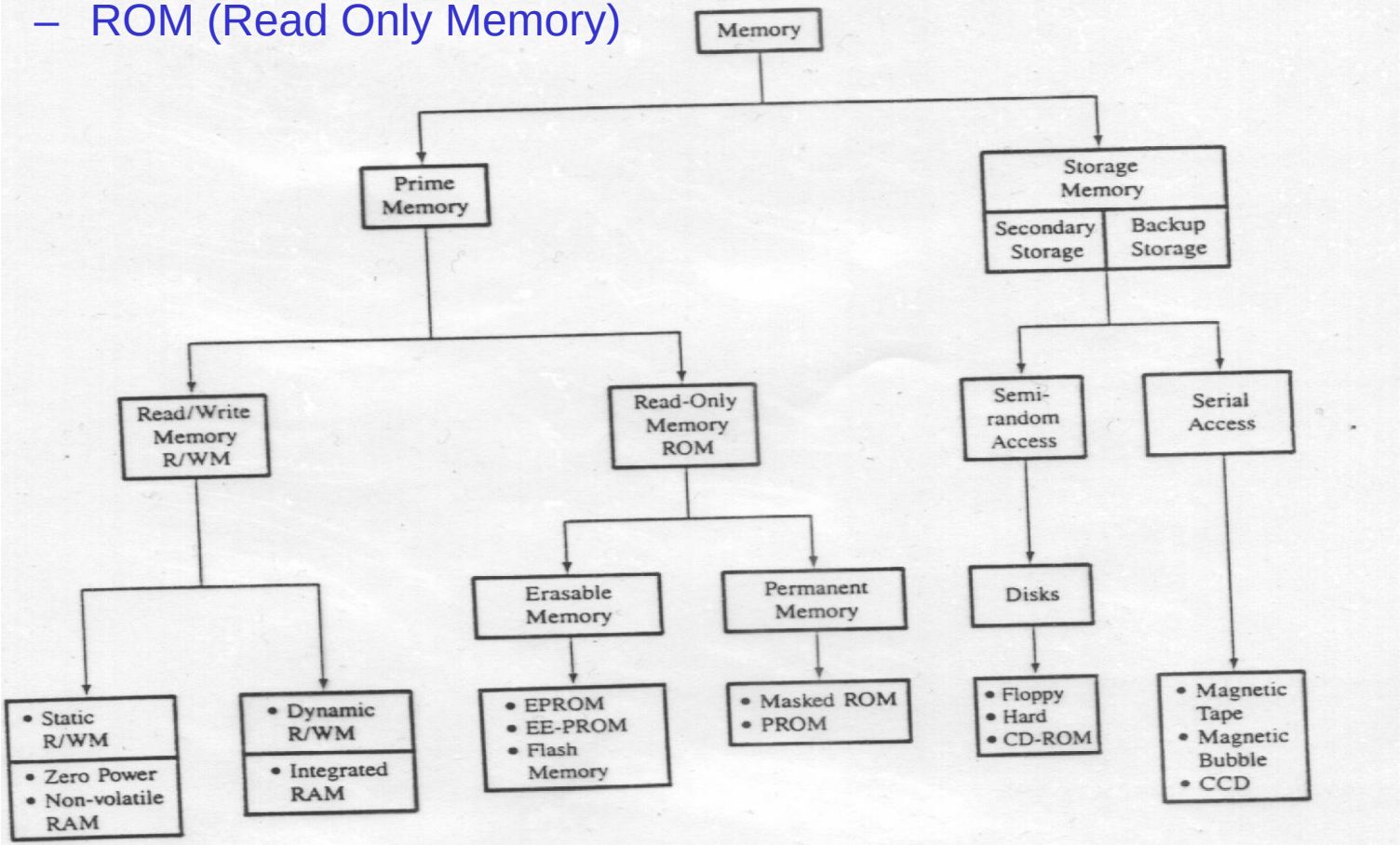


FIGURE 2.13
Memory Classification

Instruction Fetch

- The memory unit's address selector/decoder circuit examines the binary number on the address line and selects the proper memory location to be accessed.
  - In this example, CPU is reading from memory, it activates its MEMORY READ control signal
  - This causes the selected data byte in memory to be placed onto the data lines and routed to the instruction register in the CPU
- Once in the CPU, the instruction is decoded and executed
  - In the example, instruction has the decimal code 64 which for a 8086 microprocessor is decoded to be INC AX
  - The ALU (Arithmetic Logic Unit) is instructed to add 1 to the contents of the AX
- The cycle repeats itself

Instruction Set

- The list of all recognizable instructions by the instruction decoder is called the instruction set
  - CISC (Complex Instruction Set Computers), e.g., 80x86 family has more than 3000 instructions
  - RISC (Reduced Instruction Set Computers) - A small number of very fast executing instructions
- Most microprocessor chips today are allowed to fetch and execute cycles to overlap
  - This is done by dividing the CPU into
    - EU (Execution Unit)
    - BIU (Bus Interface Unit)
  - BIU fetches instructions from the memory as quickly as possible and stores them in a queue, EU then fetches the instructions from the queue not from the memory
    - The total processing time is reduced
  - Modern microprocessors also use a *pipelined* execution unit which allows the decoding and execution of instructions to be overlapped.

RISC versus CISC

- **Advantages of complex instruction set machines (CISC)**
  - Less expensive due to the use of microcode; no need to hardwire a control unit
  - Upwardly compatible because a new computer would contain a superset of the instructions of the earlier computers
  - Fewer instructions could be used to implement a given task, allowing for more efficient use of memory
  - Simplified compiler, because the microprogram instruction sets could be written to match the constructs of high-level languages
  - More instructions can fit into the cache, since the instructions are not a fixed size
- **Disadvantages of CISC**

Although the CISC philosophy did much to improve computer performance, it still had its drawbacks:

- Instruction sets and chip hardware became more complex with each generation of computers, since earlier generations of a processor family were contained as a subset in every new version
- Different instructions take different amount of time to execute due to their variable-length
- Many instructions are not used frequently; Approximately 20% of the available instructions are used in a typical program

RISC versus CISC

Advantages of RISC

Advantages of a reduced instruction set machine:

- Faster
- Simple hardware
- Shorter design cycle due to simpler hardware

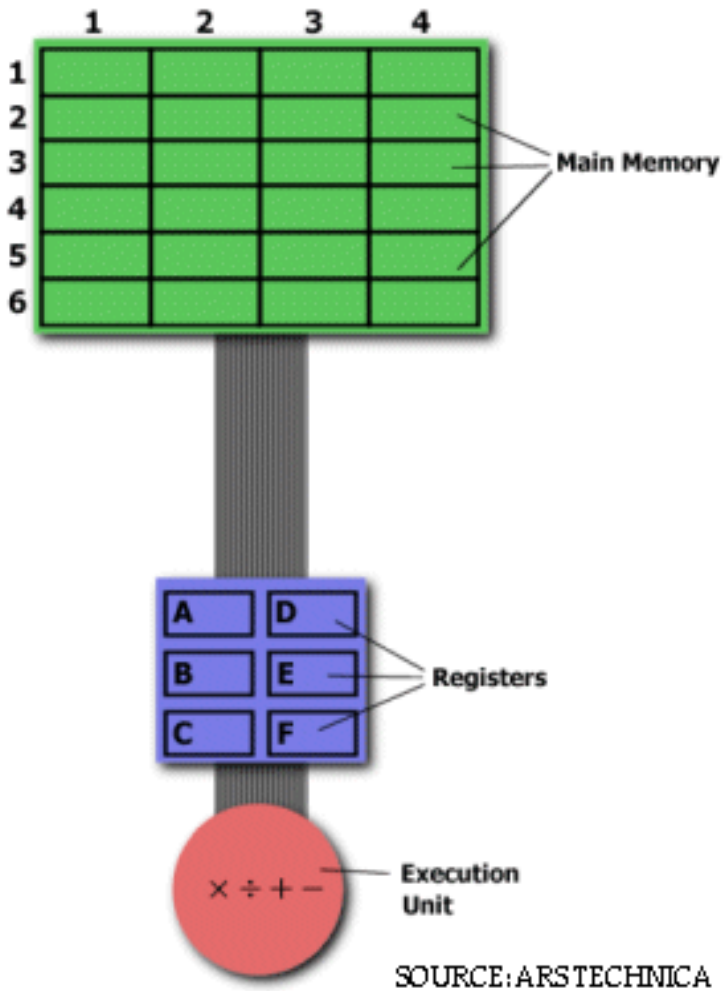
Disadvantages of RISC

Drawbacks of a reduced instruction set computer include

- Programmer must pay close attention to instruction scheduling so that the processor does not spend a large amount of time waiting for an instruction to execute
- Debugging can be difficult due to the instruction scheduling Require very fast memory systems to feed them instructions

•Nearly all modern microprocessors, including the Pentium, Power PC, Alpha and SPARC microprocessors are superscalar

More on RISC and CISC



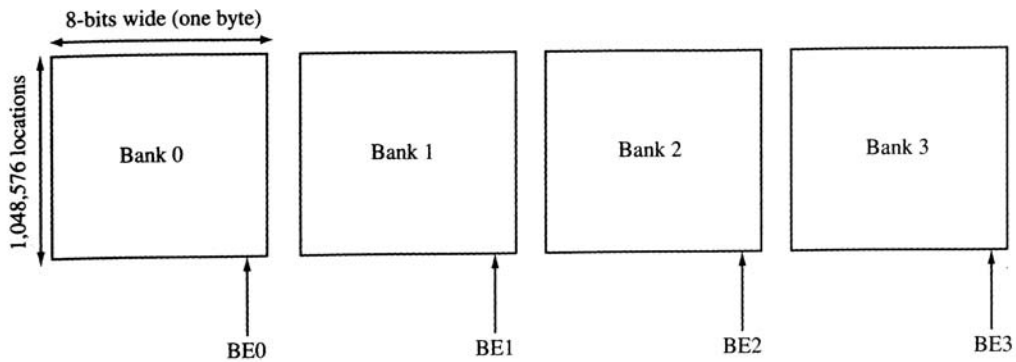
MULT 2:3, 5:2

LOAD A, 2:3
LOAD B, 5:2
PROD A, B
STORE 2:3, A

Three Bus System Architecture

- A collection of electronic signals all dedicated to particular task is called a *bus*
  - *data bus*
  - *address bus*
  - *control bus*
- **Data Bus**
  - The width of the data bus determines how much data the processor can read or write in one memory or I/O cycle (**Machine Cycle)**
  - 8-bit microprocessor has an 8-bit data bus
  - 80386SX 32-bit internal data bus, 16-bit external data bus
  - 80386 32-bit internal and external data busses
  - Data Buses are bidirectional.
  - More data means more expensive computer however faster processing speed.

Address Bus



Here the Total amount of memory is 4Mbytes

- **Address Bus** - Unidirectional
  - The address bus is used to identify the memory location or I/O device (also called port) the processor intends to communicate with
  - 20 bits for the 8086 and 8088
  - 32 bits for the 80386/80486 and the Pentium
  - 36 bits for the Pentium Pro
- 8086 has a 20-bit address bus and therefore addresses all combinations of addresses from all 0s to all 1s. This corresponds to 2^{20} addresses or 1M (1 Meg) addresses or memory locations.
- Pentium: 4Gbyte main memory

Control Bus

- Control bus is Uni-directional
- How can we tell the address is a memory address or an I/O port address
  - Memory Read
  - Memory Write
  - I/O Read
  - I/O Write
- When Memory Read or I/O Read are active, data is *input* to the processor.
- When Memory Write or I/O Write are active, data is *output* from the processor.
- The control bus signals are defined from the processor's point of view.

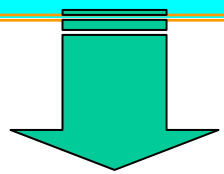
Some Important Terminology

- Bit is a binary digit that can have the value 0 or 1
- A byte is defines as 8 bits
- A nibble is half a byte
- A word is two bytes
- A double word is four bytes
- A kilobyte is 2^10 bytes (1024 bytes), The abbreviation K is most often used
  - Example: A floppy disk holding 356Kbytes of data
- A megabyte or meg is 2^20 bytes, it is exactly 1,048,576 bytes
- A gigabyte is 2^30 bytes

Internal Working Of Computers

Assume:
An imaginary CPU has registers A,B,C,D

8 bit data bus + 16 bit address bus



Addressable 0000

Memory FFFF

10000H locations =
2^16 locations

Action: 21 -> Reg A ;

Then Add 42 and 12 to Reg A

Internal Working Of Computers

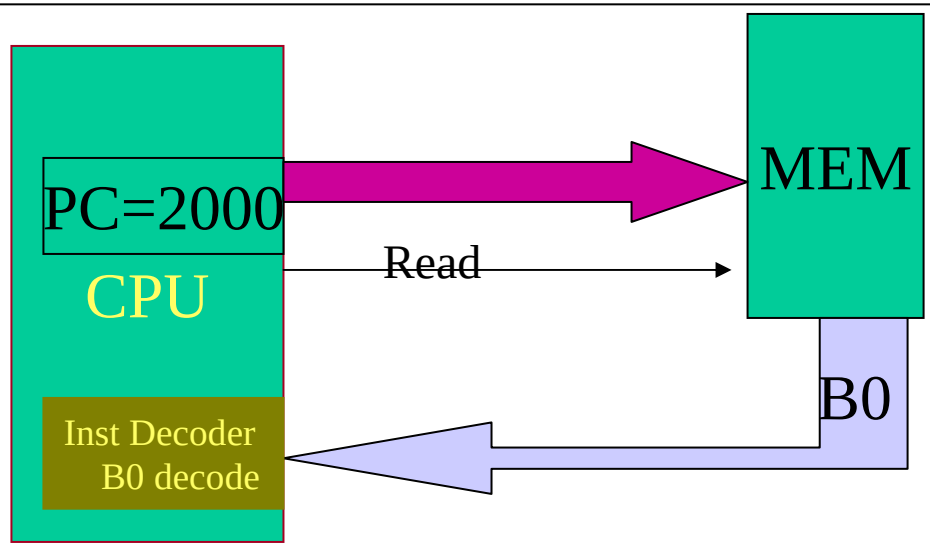
ACTION	Code	Data
Move value 21 into register A	B0H	21H
Add value 42H to register A	04H	42H
Add value 12H to register A	04H	12H

Memory Address	Contents of memory address
1400	code -(B0) the code for move to A
1401	data -(21) the value for A
1402	code -(04) the code for adding a value to A
1403	data -(42) the value to be added
1404	code -(04) the code for adding a value to A
1405	data -(12) the value to be added
1406	code -(F4) the code for halt

Internal Working Of Computers

1- the CPU program counter can have any value between 0000 → FFFFH. This one is set to start with 2000

2- the CPU puts out 2000. The memory circuitry finds the location. Activates the read signal, indicating the memory location 1400. B0 is put on the bus and brought to the CPU



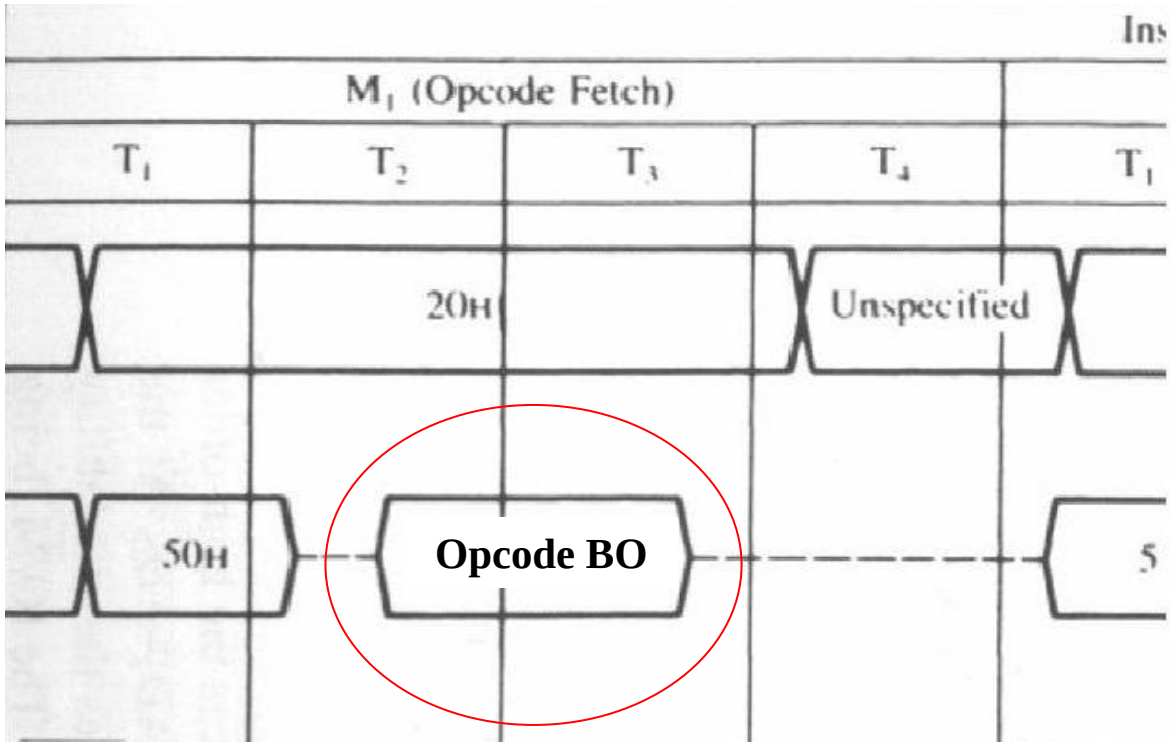
3- B0 is decoded internally it now knows it needs to fetch the next byte!. It brings 21h from 1401. The program counter automatically increments itself to the next location to fetch the next data/instruction.

Basic Timing Of The Initial Fetch

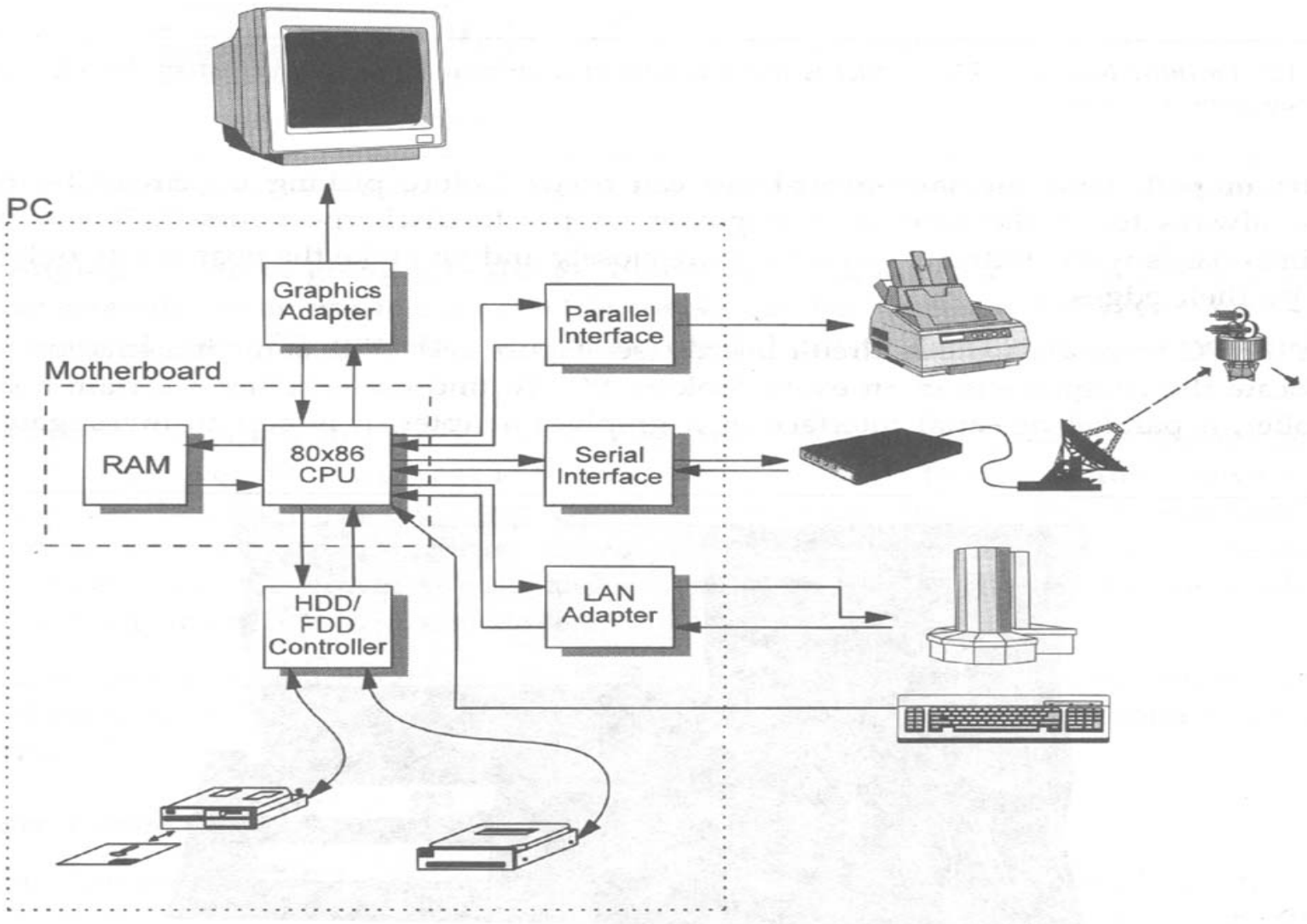
Clock Cycles

Program Counter

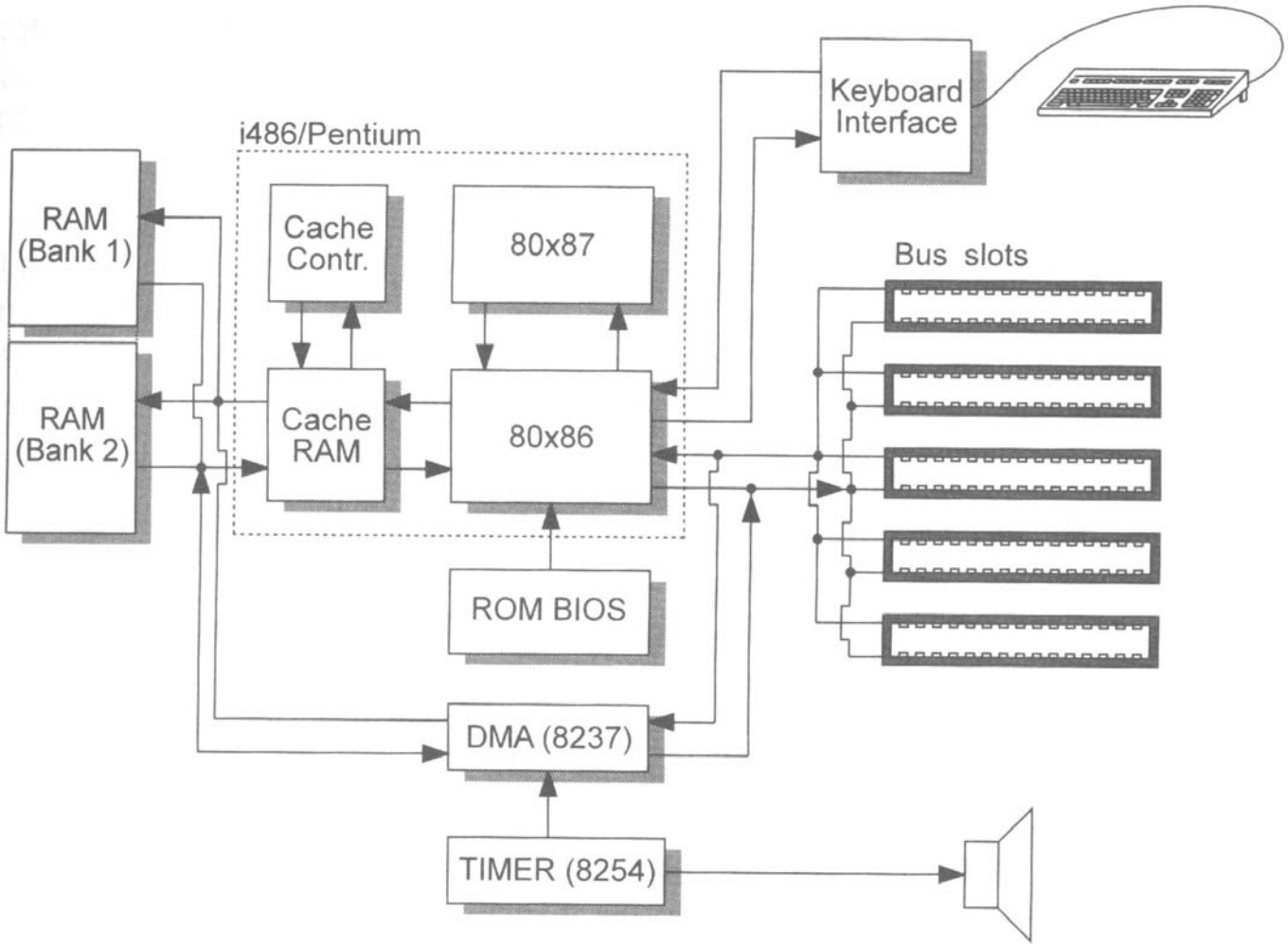
INSTRUCTION OPCODE FETCH



Data Flow Inside the PC



Motherboard



Motherboard

- The motherboard is the heart of the PC on which all components that are absolutely necessary are located.
- Motherboard and several *slots* into which the circuit boards of the graphics adapter and the interfaces are located.
- 80x86 is the central unit of the board.
  - It executes all data processing, that is, numbers are added, subtracted, multiplied, etc. logic operations with two operations with two items are executed (logical AND, XOR).
- For extensive mathematical operations (like the tangent of a real number), a mathematical coprocessor is available. Intel calls the processor as 80x87.
    - Other companies also supply coprocessors (Weitex, Cyrix).
    - May be 100 times faster than normal processors.
    - Sometimes PCs are not equipped with a coprocessor when shipped, only with a socket for it.
    - The 486DX and its successors Pentium and Pentium Pro already implement an FPU on-chip so that a coprocessor is obsolete.

Motherboard

- Another important motherboard component is the main memory or RAM.
  - Usually, the main memory is divided into several *banks;* each bank has to be fully equipped with memory chips.
  - AT-386s main memory size is typically 4 Mbytes, fully equipped Pentium PCs have at least 32 Mbytes of RAM.
  - CPU stores data and intermediate results, as well as programs, in its memory and read them later.
  - *Address:* house number of the data unit requested
  - Transferring the address to the memory is carried out by an *address bus* and the transfer of data by a *data bus*.
  - *Bus* means a number of lines through which data and signals are transferred.
  - Address bus is
    - 20 for PC XT/AT
    - 24 for AT
    - 32 for 386, 486, and Pentium

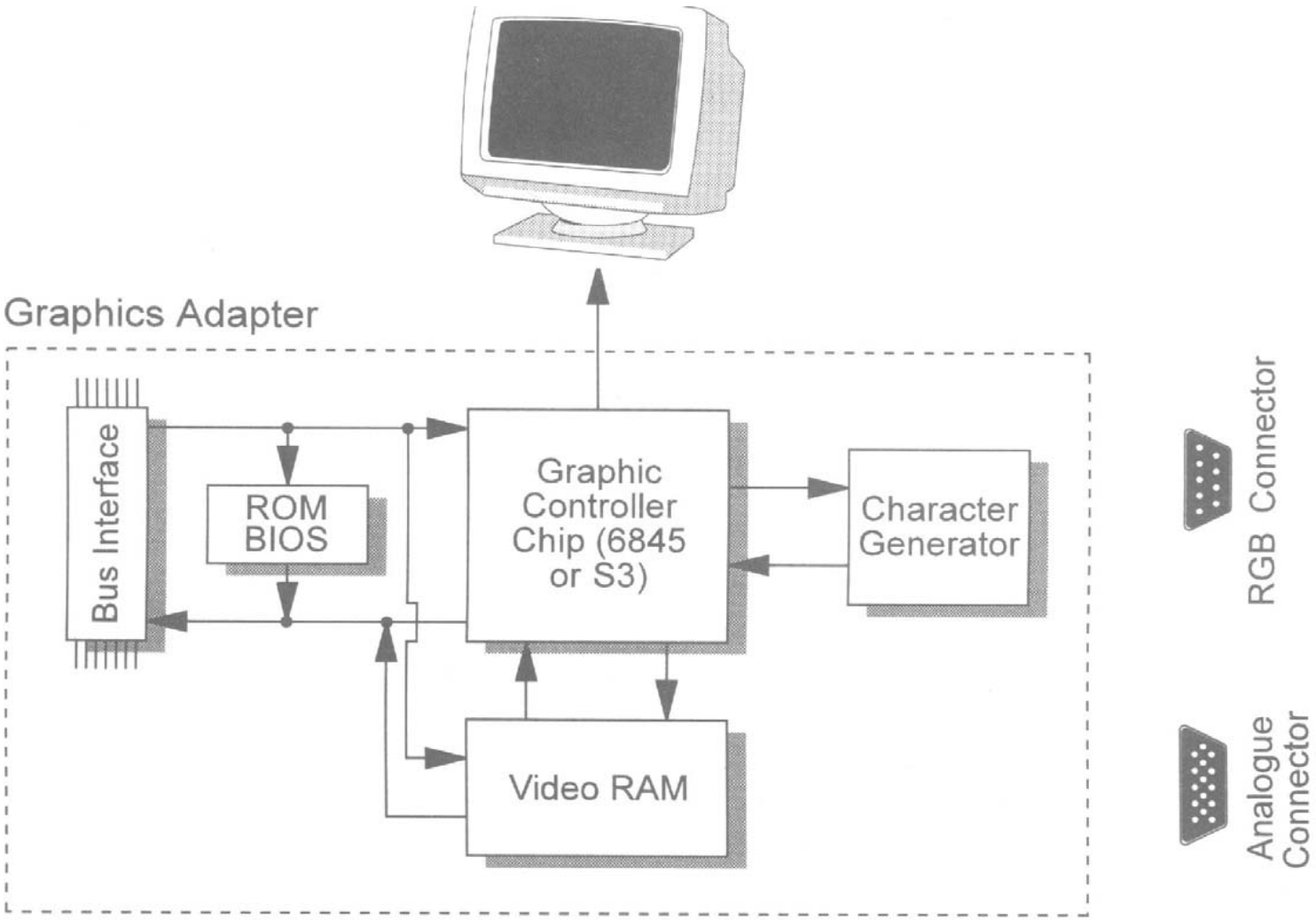
Motherboard

- Fast-clocked computers above 150 Mhz have a *cache* or *cache memory* which is significantly smaller than the main memory but much faster (access time of 10-20 ns) (level 1 or 2 in today's computers)
  - Cache holds data that is frequently accessed by the CPU.
  - Uses a cache controller to check if the required data is in the cache.
  - On the new and powerful 80x86 processors, the processor, coprocessor, cache memory, and a cache controller are all integrated on a single chip to form the i486 or Pentium.
- Motherboard also includes *Read Only Memory (ROM)*
  - Located on this chip are the programs and data that the PC needs at power-up.
  - In the ROM, there are also various support routines for accessing the keyboard, graphics adapter, etc. known collectively as ROM-BIOS.
- To control the data transfer process, additional control signals are required: e.g., write-enable signal for which one bus line is reserved.
  - Data bus, address bus, and and all control lines are known as the *system bus*.
  - 62 contacts for the XT (XT's system bus) and 62 contacts for the AT
- Bus slots: memory expansion card may be inserted in one bus slot**.**

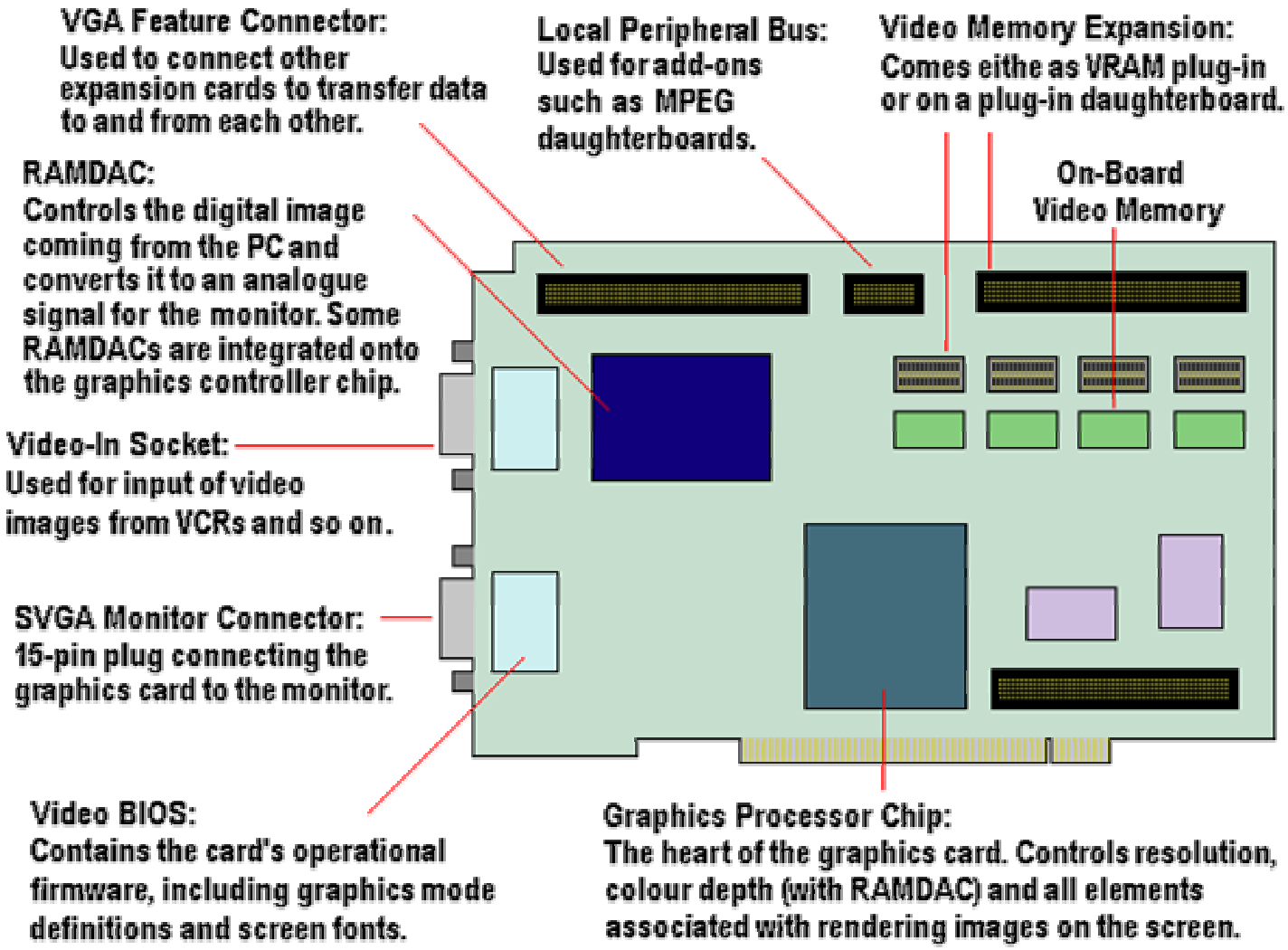
Motherboard

- Frequently, extensive amounts of data must be transferred from a hard or floppy disk into the main memory (word processor application for example). For this purpose, the motherboard has several chips optimized for data transfer within the computer - the *DMA chips (Direct Memory Access).*
  - The CPU is bypassed in this process.
- Timer chip for memory refresh (Dynamic RAM) and for supporting DOS routines time and date.

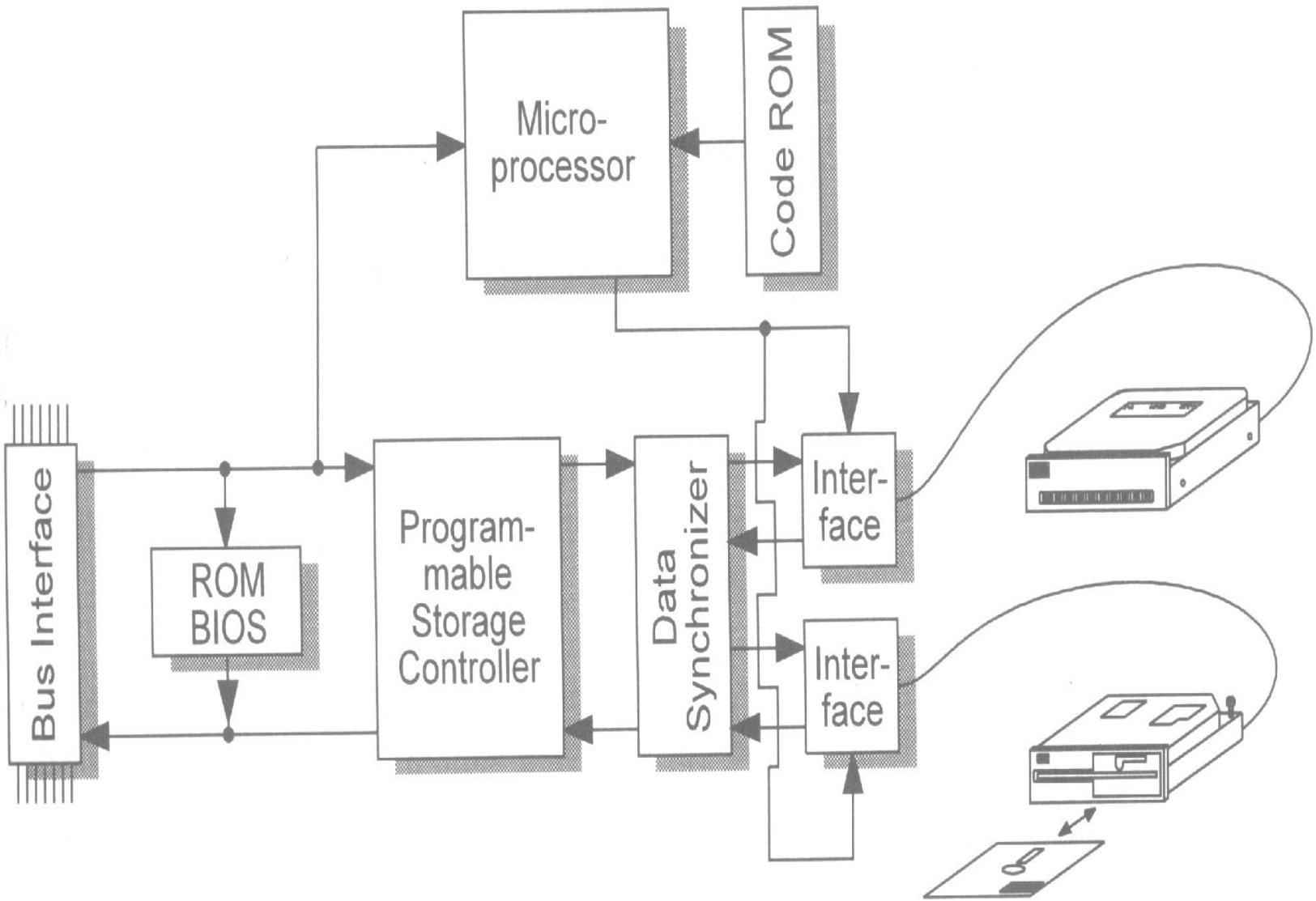
Graphics Adapters and Monitors



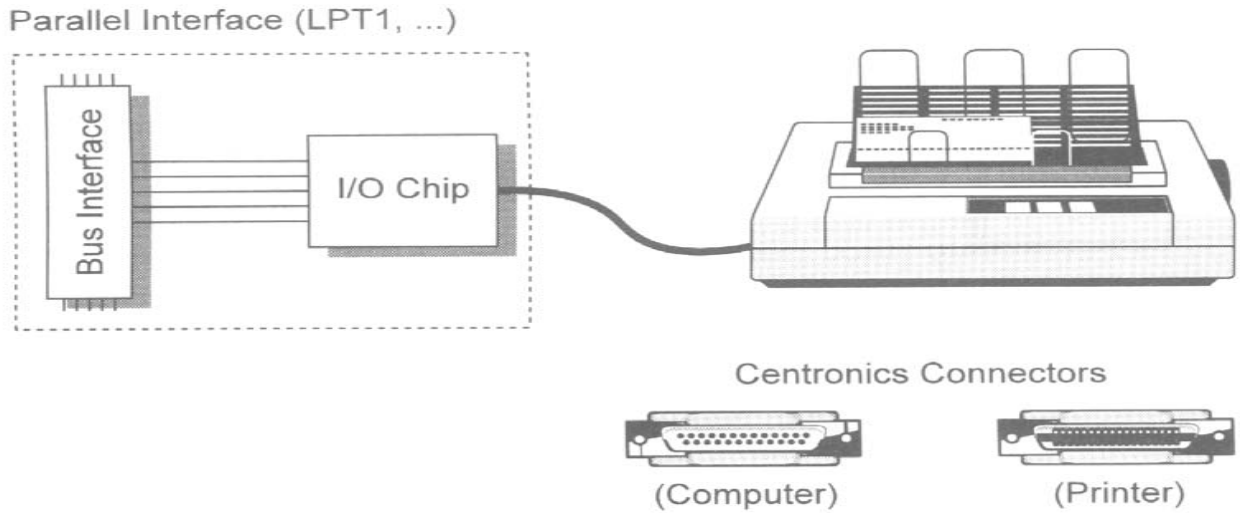
Modern Graphics Card



Drive Controllers, Floppy and Hard Disk Drives

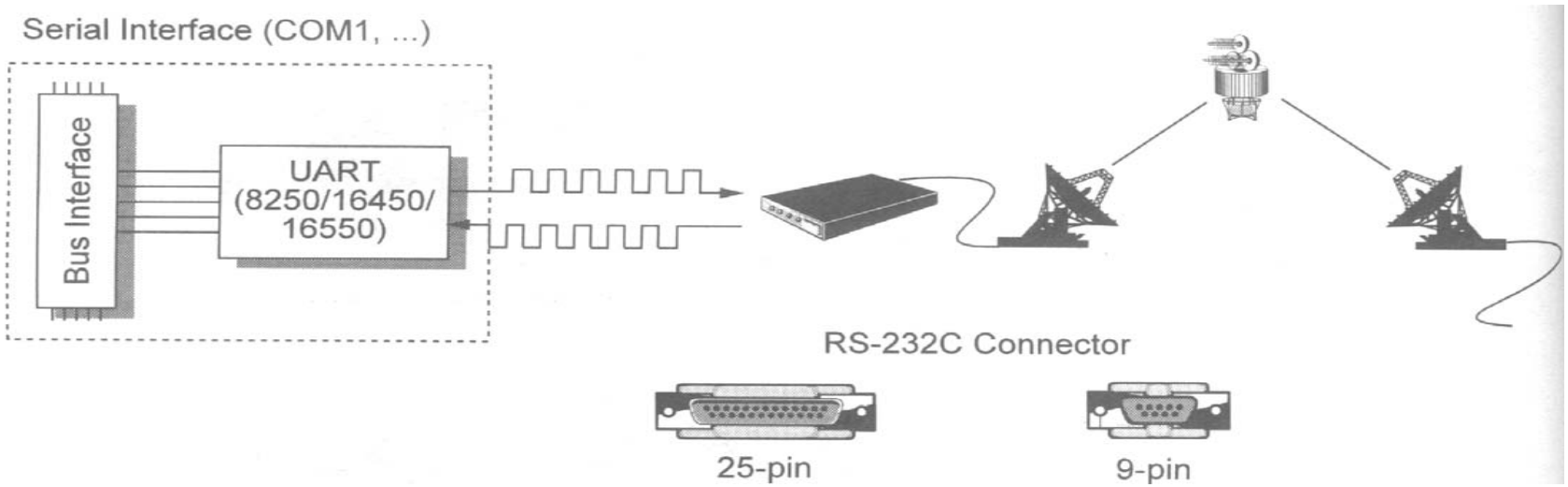


Parallel Interfaces and Printers



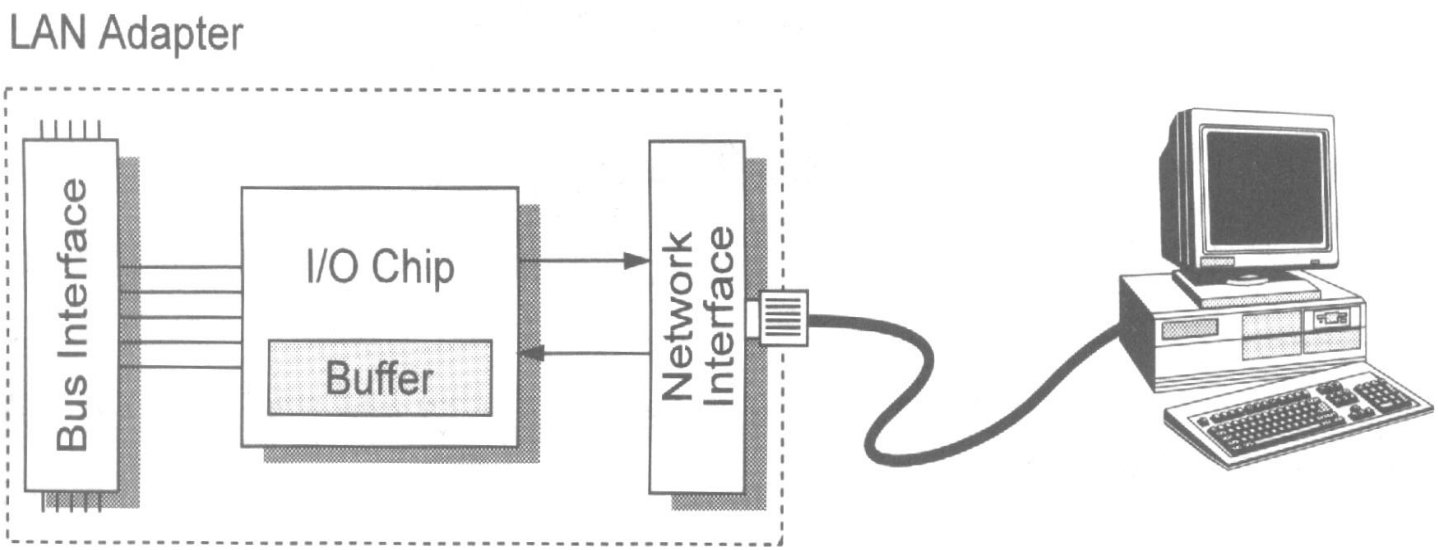
- I/O chip on the interface card accepts eight bits together and transfers them together (that is, in parallel) to the connected device (printer).
- Besides the data byte, control signals are also present to indicate whether the data has arrived.
- Up to 100 Kbytes of data can be transferred per second if the interface and the connected peripheral are correctly adapted.
- On the interface is a jack with 25 holes which supply signals according to the Centronix standard.
- The standard claims 36 holes, IBM uses 25 of them: de-facto standard
- The max distance between the computer and the printer is about 5m
- Data is exchanged via handshaking
- Usually the parallel interface only supplies data but does not receive any.
- New versions of I/O chips can receive data and it is thus possible to exchange data between computers via the parallel interface and a suitable software.

Serial Interfaces and Modems



- A PC usually has one or more serial interfaces; these are integrated on an interface adapter card together with a parallel interface.
- The central component is a so-called UART which transmits via single data line as opposed to eight as in the case for the parallel interface.
- Older PC/XTs have an 8250 chip, the AT has the more advanced 16450/16550 chip.
- UART adds additional bits; start, stop and parity bits.
- Much longer distances are possible (up to 100 m) but the transfer rate is lower.
- Serial interfaces conform to the RS232 standard which requires 25 contacts; only 14 at most are used.
- Used in modems

Network Adapters and LANs



- Networking is essential.
- A network adapter has two interfaces: one to the PC's CPU and a network interface for accessing the network.
- Network adapter can be inserted in any free slot.
- The network interface depends on the network used: Ethernet, token ring, or ATM
- 10/100T Ethernet
- I/O chip converts the data into a form that is adapted for transmission via the network.

Binary and Hexadecimal Systems - Overview

- Conversion to decimal:
  - 110.101 b = ?
  - 6A.C h = ?
- Conversion from decimal
  - for a whole number: divide by the radix and save the remainder as the significant digits
  - 10 = ? B
  - 10 = ? $_8$
- Converting from a decimal fraction
  1. multiply the decimal fraction by the radix
  2. save the whole number part of the result
  3. repeat above until fractional part of step 2 is 0
  - 0.125 = ? b
  - 0.046875 = ? h

- 110.101 b = 6.625
- 6A.C h = 106.75

- 10 = 1010 b
- 10 = 12 $_8$

- 0.125 = 0.001 b
- 0.046875 = 0.0C h

Two's Complement

- If the number is positive make no changes
- If the number is negative, complement all bits and add by 1
  - -6 => $\overline{0000\ 0110}$ + 1 = 1111 1001 + 1 = FAh
- 8 bit signed numbers
  - 0 to 7Fh (+127) are positive numbers
  - 80h (-128)to FFh (-1) are negative numbers
- Conversion of signed binary numbers to their decimal equivalent
  - 1101 0001
    - $\overline{1101\ 0001}$ + 1 = 0010 1110 + 1 = 0010 1111 = 2Fh => -47
  - 1000 1111 0101 1101
    - 0111 0000 1010 0010 + 1 = 0111 0000 1010 0011 = 70C3h => -28835
- Two's complement arithmetic
  - +14 - 20
  - 0000 1110 + $\overline{0001\ 0100}$ + 1 = FAh

Sign Flag indicates the polarity

- *Overflow:* Whenever two signed numbers are added or subtracted the possibility exist that the result may be too large for the number of bits allocated Ex: +64 +96 using 8-bit signed numbers

Two's Complement

- -128 1000 0000b 80h
- -127 1000 0001b 81h
- -126 1000 0010b 82h
- -2 11111110b FEh
- -1 11111111b FFh
- 0 0000000b 00h
- 1 00000001b 01h
- +127 01111111b 7Fh

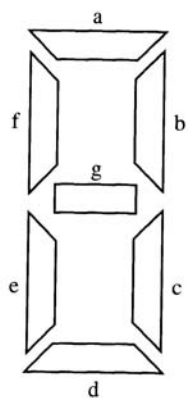
- Numbers in the range
  - -2^n …2^n –1
- are represented by signed arithmetic

ASCII

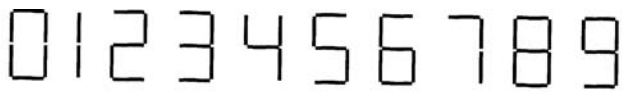
- The standard for text
- In this code each letter of the alphabet, punctuation mark, and decimal number is assigned a unique 7-bit code number
- With 7 bits, 128 unique symbols can be coded
  - e.g., Uppercase A → 41h
- Error detection codes
  - Parity
    - F has the ASCII code 46h or 100 0110
    - Even parity encoded F becomes 1100 0110 or C6h
- Which of the following are errored transmissions if even parity is used?
  - E1h = 1110 0001
  - 20h = 0010 0000 *error*
  - 72h = 0111 0010
- Parity method of error detection can only be used to detect odd numbers of errors
  - 72h => 77h *use more sophisticated checksums*

BCD

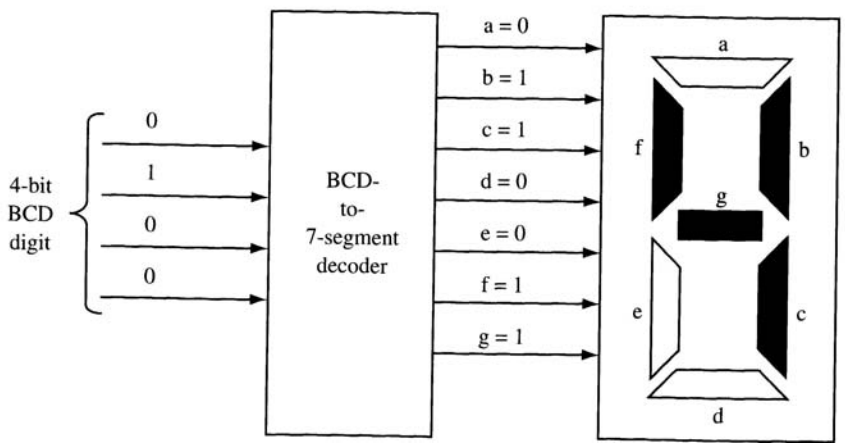
- BCD code provides a way for decimal numbers to be encoded in binary form that is easily converted back to decimal
  - 26 => 0010 0110 (BCD) => 11010 (unsigned binary)
  - 243 => 0010 0100 0011 (BCD) => 1111 0011 (unsigned binary)
- Used in seven segment displays



(a)



(b)



Computer Programming

- Von Neumann machine
- UNIVAC 1950 first assembly language used on a machine.
- Machine Language vs Assembly Language
  - Machine language or object code is the only code a computer can execute but it is nearly impossible for a human to work with
  - E4 27 88 C3 E4 27 00 D8 E6 30 F4 the object code for adding two numbers input from the keyboard
- When programming a microprocessor, programmers often use assembly language
  - This involves 3-5 letter abbreviations for the instruction codes (mnemonics) rather than the binary or hex object codes

Source code

Address	Hex Object Code				Mnemonics		Comment
					Op-Code	Operand	
0100	E4	27			IN	AL,27H	Input first number from port 27H and store in AL
0102	88	C3			MOV	BL,AL	Save a copy of register AL in register BL
0104	E4	27			IN	AL,27H	Input second number to AL
0106	00	D8			ADD	AL,BL	Add contents of BL to AL and store the sum in AL
0107	E6	30			OUT	30H,AL	Output AL to port 30H
0109	F4				HLT		Halt the computer

Edit, Assemble, Test, and Debug Cycle

- Using an *editor*, the source code of the program is created. This means selecting the appropriate instruction mnemonics to accomplish the task
- A compiler program which examines the source code file generated by the editor and determines the object code for each instruction in the program, is then run. In assembly language programming, this is called an *assembler*.
- The object code produced by the computer is loaded into the target computer's memory and is then *run.*
- *Debugging:* locating and fixing the source of error
- High-level programming Languages
  - Basic
  - C

Computer Operating Systems

- What happens when the computer is first turned on?
- MS-DOS
  - A startup program in the BIOS is executed
  - This program in turn accesses the master boot record on the floppy or hard disk drive
  - A loader then transfers the system files IO.SYS and MSDOS.SYS from the disk drive to the main memory
  - Finally, the command interpreter COMMAND.COM is loaded into memory which puts the DOS prompt on the screen that gives the user access to DOS's built-in commands like DIR, COPY, VER.
- The 640 K Barrier
  - DOS was designed to run on the original IBM PC
  - 8088 microprocessor, 1Mbytes of main memory
  - IBM divided this 1Mb address space into specific blocks
    - 640 K of RAM (user RAM)
    - 384 K reserved for ROM functions (control programs for the video system, hard drive controller, and the basic input/output system)

MS-DOS Functions and BIOS Services

BIOS: usually stored in ROM

- tells the CPU what to do at startup
- these routines provide access to the peripheral devices of the PC, such as the keyboard, video, printer, and disk
- To test all the devices connected to the PC and alert if error

- Access to the BIOS is done through the software interrupt instruction Int *n*
- For example, the BIOS keyboard services are accessed using the instruction INT 16h
- In addition to BIOS services, DOS also provides higher level functions
  - INT 21h
  - More details later