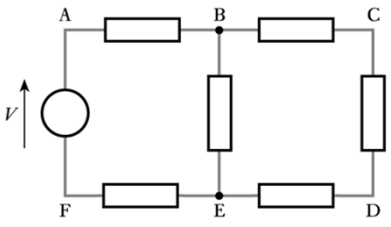
Kirchhoff's Voltage and Current Laws

Kirchhoff's Laws

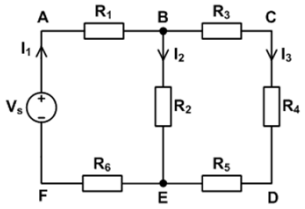
- **Node**
  - a point in a circuit where two or more circuit components are joined
- **Loop**
  - any closed path that passes through no node more than once
- **Mesh**
  - a loop that contains no other loop
- **Examples:**
  - A, B, C, D, E and F are *nodes*
  - the paths ABEFA, BCDEB and ABCDEFA are *loops*
  - ABEFA and BCDEB are *meshes*



- **Kirchhoff's Voltage Law (KVL)**

  At any instant the algebraic sum of all the voltages around any loop in a circuit is zero

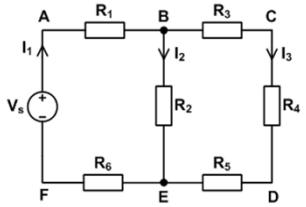
$$\sum_i V_i = 0$$



KVL around loop ABEFA: $V_{AF} + V_{BA} + V_{EB} + V_{FE} = 0$

or with the voltage polarities reversed: $V_{FA} + V_{AB} + V_{BE} + V_{EF} = 0$

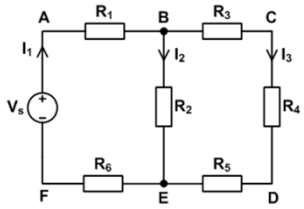
Proof: $(V_A - V_F) + (V_B - V_A) + (V_E - V_B) + (V_F - V_E) = 0$



Example 1: Let us write KVL around loop ABCDEFA

$$V_{AF} + V_{BA} + V_{CB} + V_{DC} + V_{ED} + V_{FE} = 0$$

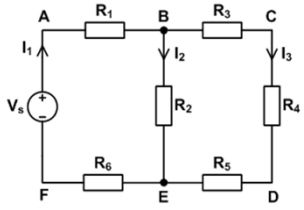
$$V_s - I_1R_1 - I_3R_3 - I_3R_4 - I_3R_5 - I_1R_6 = 0$$



Example 2: Let us write KVL around loop ABEFA

$$V_{AF} + V_{BA} + V_{EB} + V_{FE} = 0$$

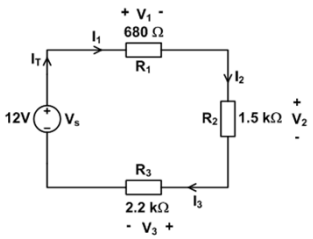
$$V_s - I_1R_1 - I_2R_2 - I_1R_6 = 0$$



Example 3: Let us write KVL around loop BCDEB

$$V_{BE} + V_{CB} + V_{DC} + V_{ED} = 0$$

$$I_2R_2 - I_3R_3 - I_3R_4 - I_3R_5 = 0$$



Example 4: Notice in the series example given earlier that the sum of the resistor voltages is equal to the source voltage.

KVL: $V_s - V_1 - V_2 - V_3 = 0$

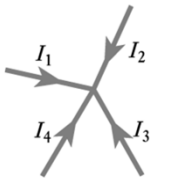
I_1= 2.74 mA	R_1= 0.68 kΩ	V_1= 1.86 V	P_1= 5.1 mW
I_2= 2.74 mA	R_2= 1.50 kΩ	V_2= 4.11 V	P_2= 11.3 mW
I_3= 2.74 mA	R_3= 2.20 kΩ	V_3= 6.03 V	P_3= 16.5 mW
I_T= 2.74 mA	R_T= 4.38 kΩ	V_S= 12 V	P_T= 32.9 mW

- **Kirchhoff's Current Law (KCL)**

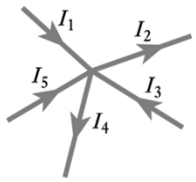
At any instant, the algebraic sum of all the currents flowing into any node in a circuit is zero

$$\sum_i I_i = 0$$

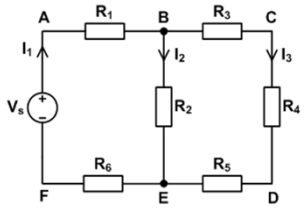
– Label the currents flowing ***into the node*** as **positive** and the currents flowing ***out of the node*** as **negative**



$I_1 + I_2 + I_3 + I_4 = 0$



$I_1 - I_2 + I_3 - I_4 + I_5 = 0$



Example 1: Let us write KCL at node A

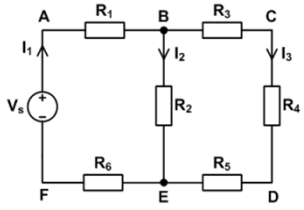
$$I_{FA} + I_{BA} = 0$$

$$I_1 - I_1 = 0$$

Example 2: Let us write KCL at node B

$$I_{AB} + I_{CB} + I_{EB} = 0$$

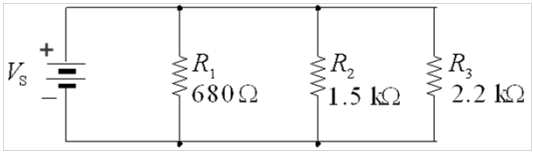
$$I_1 - I_3 - I_2 = 0$$



Example 3: Let us write KCL at node E

$$I_{BE} + I_{DE} + I_{FE} = 0$$

$$I_2 + I_3 - I_1 = 0$$



Example 4: Notice in the parallel resistors example given earlier, the current from the source was equal to the sum of the branch currents.

KCL**:** $I_s - I_1 - I_2 - I_3 = 0$

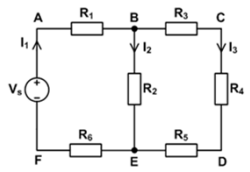
I_1=	7.4 mA	R_1= 0.68 kΩ	V_1= 5.0 V	P_1= 36.8 mW
I_2=	3.3 mA	R_2= 1.50 kΩ	V_2= 5.0 V	P_2= 16.7 mW
I_3=	2.3 mA	R_3= 2.20 kΩ	V_3= 5.0 V	P_3= 11.4 mW
I_T=	13.0 mA	R_T= 386 Ω	V_S= 5.0 V	P_T= 64.8 mW

Total Power

Total power in an electrical circuit should be zero, i.e., generated power should be equal to the dissipated power. **A negative value** for the power indicates that it is a **generated power**.

$$\boxed{\sum_i P_i = 0}$$

Example 1:

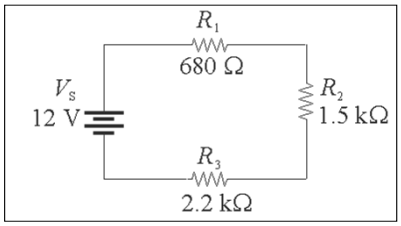


$$\boxed{P_{AF} + P_{AB} + P_{BE} + P_{BC} + P_{CD} + P_{DE} + P_{EF} = 0}$$

$$-V_s I_1 + I_1^2 R_1 + I_2^2 R_2 + I_3^2 R_3 + I_3^2 R_4 + I_3^2 R_5 + I_1^2 R_6 = 0$$

$$V_s I_1 = I_1^2 R_1 + I_2^2 R_2 + I_3^2 R_3 + I_3^2 R_4 + I_3^2 R_5 + I_1^2 R_6$$

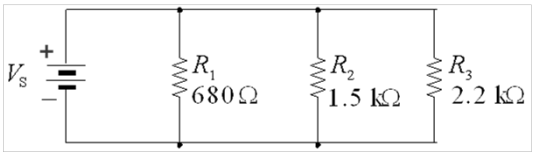
$$\boxed{V_s I_1 = I_1^2 (R_1 + R_6) + I_2^2 R_2 + I_3^2 (R_3 + R_4 + R_5)}$$



Example 2: Notice in the series example given earlier that the sum of the resistor voltages is equal to the source voltage.

KVL**:** $V_s - V_1 - V_2 - V_3 = 0$

I_1= 2.74 mA	R_1= 0.68 kΩ	V_1= 1.86 V	P_1= 5.1 mW
I_2= 2.74 mA	R_2= 1.50 kΩ	V_2= 4.11 V	P_2= 11.3 mW
I_3= 2.74 mA	R_3= 2.20 kΩ	V_3= 6.03 V	P_3= 16.5 mW
I_T= 2.74 mA	R_T= 4.38 kΩ	V_S= 12 V	P_T= 32.9 mW



Example 3: Notice in the parallel resistors example given earlier, the current from the source was equal to the sum of the branch currents.

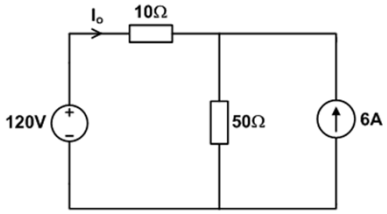
KCL**:** $I_s - I_1 - I_2 - I_3 = 0$

I_1= 7.4 mA	R_1= 0.68 kΩ	V_1= 5.0 V	P_1= 36.8 mW
I_2= 3.3 mA	R_2= 1.50 kΩ	V_2= 5.0 V	P_2= 16.7 mW
I_3= 2.3 mA	R_3= 2.20 kΩ	V_3= 5.0 V	P_3= 11.4 mW
I_T= 13.0 mA	R_T= 386 Ω	V_S= 5.0 V	P_T= 64.8 mW

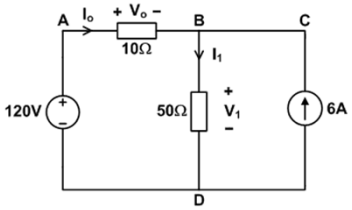
Example: Consider the electrical circuit below

a) Find I_o.

b) Verify that the total power dissipated equals to the total power generated.



Solution:

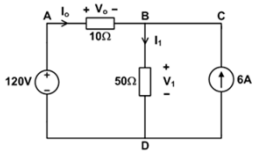


a) Let us write KCL and KVL equations for Node B and Loop ABDA, respectively.

$$\left.\begin{aligned} I_o - I_1 + 6 = 0 \\ 120 - 10I_o - 50I_1 = 0 \end{aligned}\right\} \quad \begin{aligned} I_o &= -3\,\text{A} \\ I_1 &= 3\,\text{A} \end{aligned}$$

Additionally, let us find V_o and V_1

$$\begin{aligned} V_o &= 10I_o \\ V_1 &= 50I_1 \end{aligned} \quad \Rightarrow \quad \begin{aligned} V_o &= 10(-3) = -30\,\text{V} \\ V_1 &= 50(3) = 150\,\text{V} \end{aligned}$$



b) Let us calculate powers across all the elements in the circuit

$$P_{120V} = V_{AD}I_{AD} = 120(3) = 360\,\text{W} \quad \text{(dissipated)}$$
$$P_{10\Omega} = V_{AB}I_{AB} = (-30)(-3) = 90\,\text{W} \quad \text{(dissipated)}$$
$$P_{50\Omega} = V_{BD}I_{BD} = (150)(3) = 450\,\text{W} \quad \text{(dissipated)}$$
$$P_{6A} = V_{CD}I_{CD} = (150)(-6) = -900\,\text{W} \quad \textbf{(generated)}$$

As expected total power in the circuit is zero

$$P_{120V} + P_{10\Omega} + P_{50\Omega} + P_{6A} = 0$$

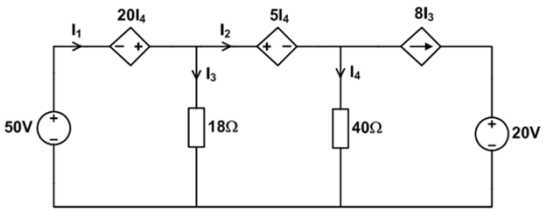
Total power dissipated $= 360 + 90 + 450 = 900\,\text{W}$
Total power generated $= 900\,\text{W}$

Example : (with dependent sources)

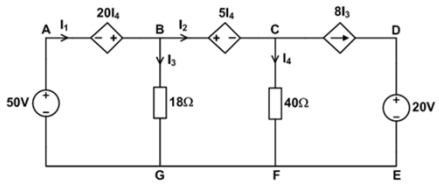
Consider the electrical circuit below

a) Find I_1, I_2, I_3 and I_4.

b) Verify the power condition ($P_{dissipated} = P_{generated}$)



Solution:



a) By writing a KVL equation Loop ABCFGA, we can find I_4

$$50 + 20I_4 - 5I_4 - 40I_4 = 0$$
$$50 - 25I_4 = 0$$
$$I_4 = 2\,\text{A}$$

Then, by writing a KVL equation Loop ABGA, we can find I_3

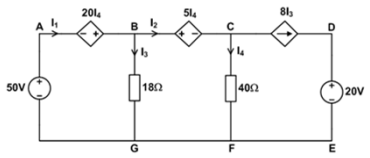
$$50 + 20I_4 - 18I_3 = 0$$
$$50 + 20(2) - 18I_3 = 0$$
$$I_3 = 5\,\text{A}$$

Then, by writing a KCL equation at Node C we can find I_2

$$I_2 = I_4 + 8I_3 = 2 + 8(5) = 42\,\text{A}$$

Finally, by writing a KCL equation at Node B we can find I_1

$$I_1 = I_2 + I_3 = 42 + 5 = 47\,\text{A}$$



b) Let us first a write a KVL equation in Loop CDEFC to find V_{CD}

$$V_{CF} - V_{CD} - V_{DE} = 0$$
$$40(2) - V_{CD} - 20 = 0$$
$$V_{CD} = 60\,\text{V}$$

Now, let us calculate powers across all the elements in the circuit

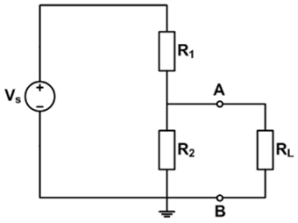
$$P_{50V} = V_{AG}I_{AG} = 50(-47) = -2350\,\text{W} \quad \textbf{(generated)}$$
$$P_{20I_4} = V_{AB}I_{AB} = (-20(2))(47) = -1880\,\text{W} \quad \textbf{(generated)}$$
$$P_{18\Omega} = V_{BG}I_{BG} = (18(5))(5) = 450\,\text{W} \quad \text{(dissipated)}$$
$$P_{5I_4} = V_{BC}I_{BC} = (5(2))(42) = 420\,\text{W} \quad \text{(dissipated)}$$
$$P_{40\Omega} = V_{CF}I_{CF} = (40(2))(2) = 160\,\text{W} \quad \text{(dissipated)}$$
$$P_{8I_3} = V_{CD}I_{CD} = (60)(8(5)) = 2400\,\text{W} \quad \text{(dissipated)}$$
$$P_{20V} = V_{DE}I_{DE} = (20)(8(5)) = 800\,\text{W} \quad \text{(dissipated)}$$

Total power dissipated $= 450 + 420 + 160 + 2400 + 800 = 4230\,\text{W}$
Total power generated $= 2350 + 1880 = 4230\,\text{W}$

Loaded Voltage Divider

The voltage-divider equation was developed for a series circuit. Recall that the output voltage is given by

$$V_2 = \left(\frac{R_2||R_L}{R_T}\right) V_s = \left(\frac{R_2||R_L}{R_1 + R_2||R_L}\right) V_s$$

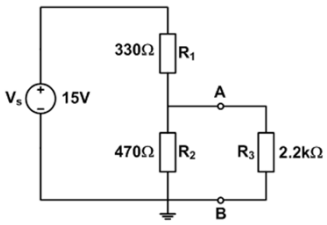


A voltage-divider with a resistive load is a combinational circuit and the voltage divider is said to be loaded.

The loading reduces the total resistance from Node A to ground.

Example:

What is the voltage across R_3?



Solution:

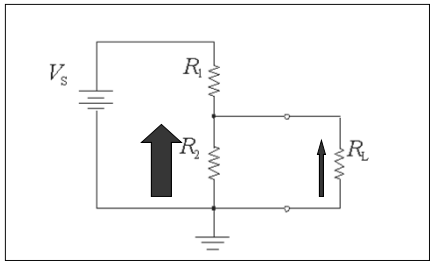
Form an equivalent series circuit by combining R_2 and R_3; then apply the voltage-divider formula to the equivalent circuit:

$$R_{2,3} = R_2 \| R_3 = 470\ \Omega \| 2.2\ \text{k}\Omega = 387\ \Omega$$

$$V_3 = V_{2,3} = \left(\frac{R_{2,3}}{R_1 + R_{2,3}}\right) V_S = \left(\frac{387\ \Omega}{330\ \Omega + 387\ \Omega}\right) 15\ \text{V} = 8.10\ \text{V}$$

Stiff voltage divider

A **stiff voltage-divider** is one in which the loaded voltage nearly the same as the no-load voltage. To accomplish this, the load current must be small compared to the bleeder current (or R_L is large compared to the divider resistors).



Example: If $R_1 = R_2 = 1.0$ kΩ, what value of R_L will make the divider a stiff voltage divider? What fraction of the unloaded voltage is the loaded voltage?

Solution: $R_L > 10\ R_2$; R_L should be 10 kΩ or greater.

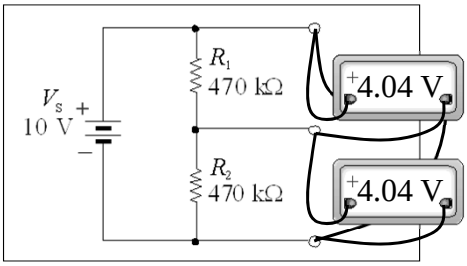
For a 10 kΩ load,

$$V_L = \left(\frac{R_2 \| R_L}{R_1 + R_2 \| R_L}\right) V_S = \left(\frac{0.91\ \text{k}\Omega}{1.0\ \text{k}\Omega + 0.91\ \text{k}\Omega}\right) V_S = (0.476) V_S$$

This is 95% of the unloaded voltage.

Loading Effect of a Voltmeter

Assume V_S = 10 V, but the meter reads only 4.04 V when it is across either R_1 or R_2.



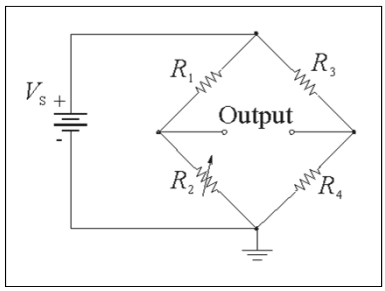
Can you explain what is happening?

All measurements affect the quantity being measured. A voltmeter has internal resistance, which can change the resistance of the circuit under test. In this case, a 1 MΩ internal resistance of the meter accounts for the readings.

Wheatstone bridge

The Wheatstone bridge consists of a DC voltage source and four resistive arms forming two voltage dividers. The output is taken between the dividers.

Frequently, one of the bridge resistors is adjustable.



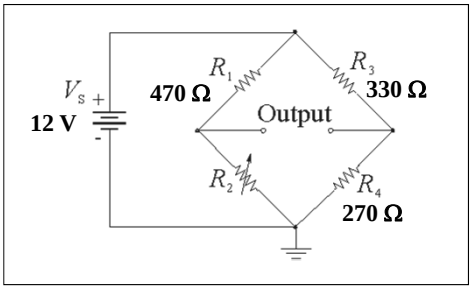
When the bridge is balanced, the output voltage is **zero**,

and the products of resistances in the opposite diagonal arms are **equal**.

Example:

What is the value of R_2 if the bridge is balanced?

$R_2 = 384\ \Omega$



Troubleshooting

The effective troubleshooter must think logically about circuit operation.

Analysis: Understand normal circuit operation and find out the symptoms of the failure.

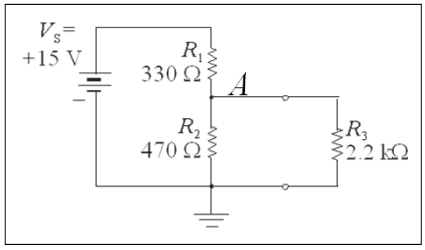
Planning: Decide on a logical set of steps to find the fault.

Measurement: Following the steps in the plan, make measurements to isolate the problem.

Modify the plan if necessary.

Example:

The output of the voltage-divider is 6V. Describe how you would use analysis and planning in finding the fault.



Analysis: From an earlier calculation, V_3 should equal **8.10 V**. A low voltage is most likely caused by a low source voltage or incorrect resistors (possibly R_1 and R_2 reversed). If the circuit is new, incorrect components are possible.

Planning: Decide on a logical set of steps to locate the fault. You could decide to

1) Check the source voltage,

2) Disconnect the load and check the output voltage, and if it is correct,

3) Check the load resistance. If R_3 is correct, check other resistors.