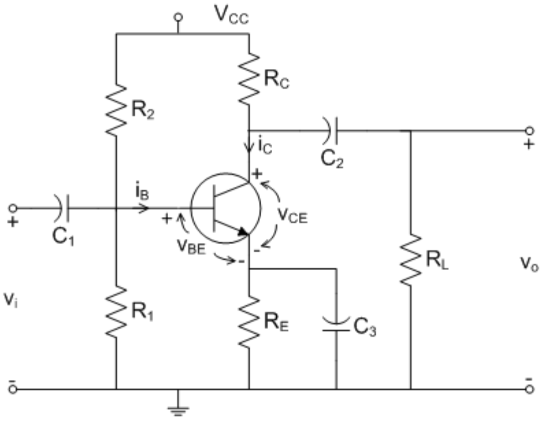
Contents

BJT AC Analysis

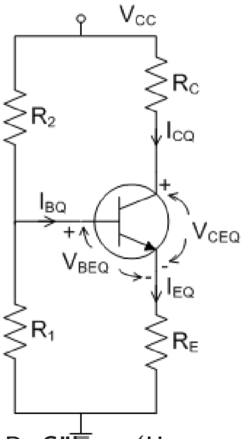
1. Draw the AC equivalent circuit (signal frequency is infinity, i.e., $f = \infty$)
   a) Capacitors are short circuit, i.e., $X_C \to 0$.
   b) Kill the DC power sources (short-circuit DC voltage sources and open-circuit DC current sources).

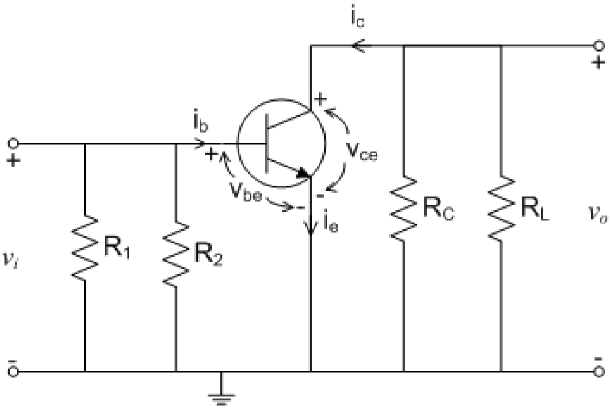
2. Write KVL for the loop which contains CE terminals
   a) Develop AC load-line equation.

3. Draw AC-DC load lines
   a) Find available swings for a given input or find maximum undistorted swings.

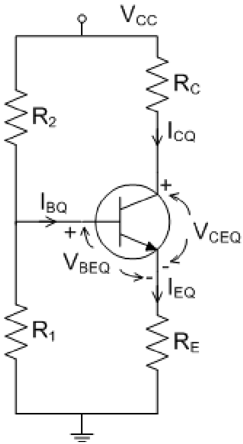


Consider the common-emitter BJT circuit shown above where $v_i = V_m \sin(\omega t)$. Its DC and AC are shown below





DC Load Line



DC equivalent circuit shown above, let us first define the equivalent output-loop (CE-loop) DC resistance R_{DC} and V_{CE} as follows

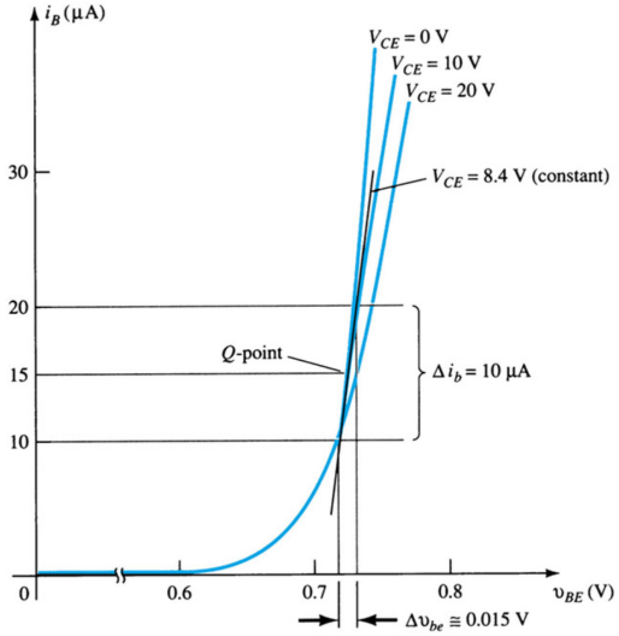
$$R_{DC} = R_C + R_E$$

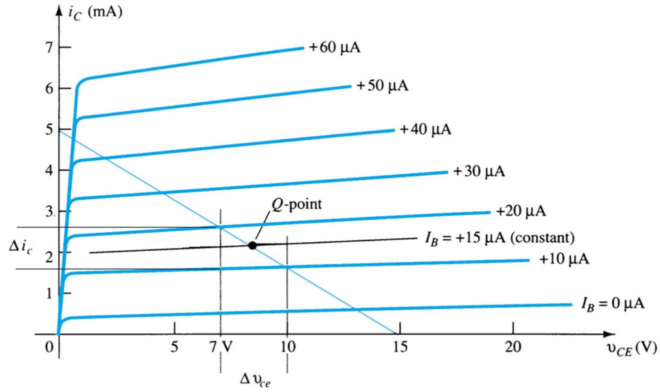
$$V_{CE} = V_{CC} - I_C R_{DC}$$

Thus, the rearranged **DC load line equation** (DC output equation) is given by

$$\boxed{I_C = \frac{-1}{R_{DC}} V_{CE} + \frac{V_{CC}}{R_{DC}}}$$

Note that, AC swings are around the Q-points. Here, input swing $v_{be} = v_i$ on the left below is around the input Q-point (I_{BQ}, V_{BEQ}), and output swing $v_o = v_{ce}$ on the right below is around the output Q-point (I_{CQ}, V_{CEQ}).

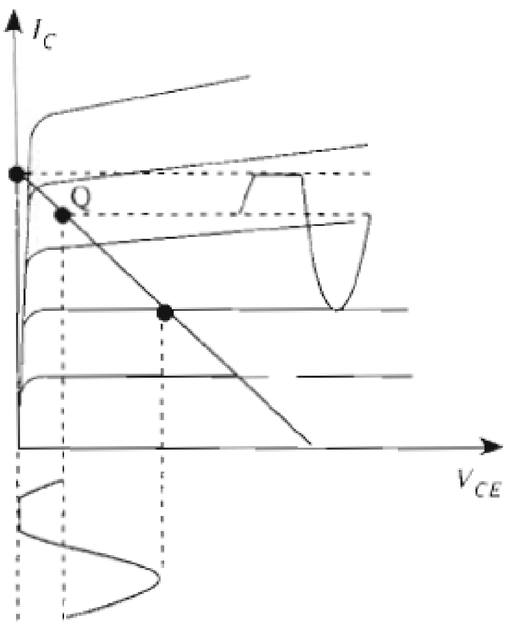


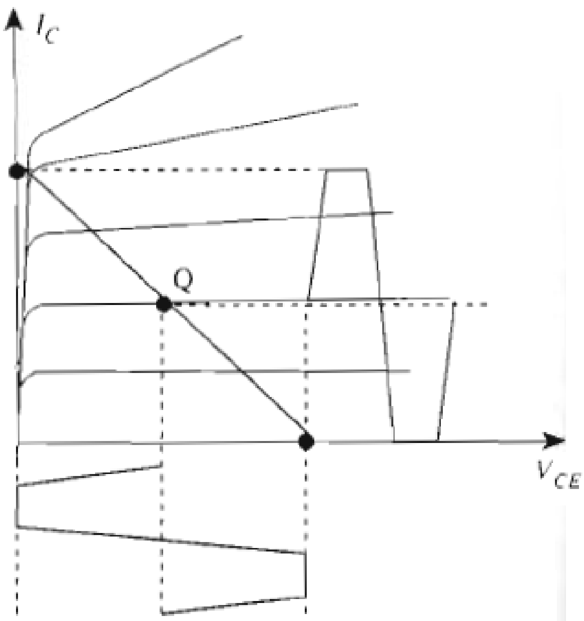


Distortion

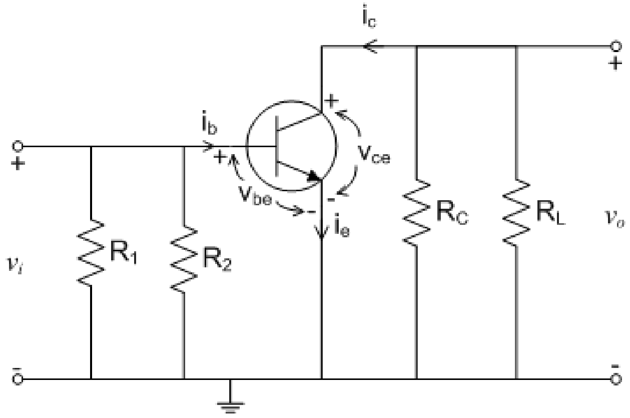
If the Q-point is incorrect as shown on the left below, or if the input is too high as shown on the right below, then the output swings (for a sinusoidal input) as shown in the figures below will be **distorted**, i.e., not the same shape as the input waveform.

NOTE: Load-lines shown in the figures below are the AC load-lines which we will derive in the next slides.





AC Load Line



AC equivalent circuit shown above, let us first define the equivalent output-loop (CE-loop) AC resistance R_{ac} and output v_o as follows

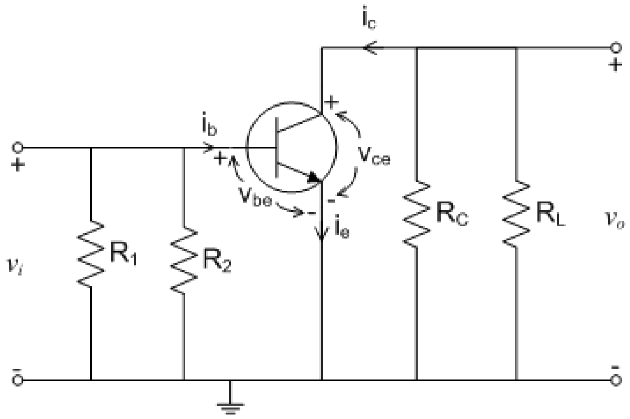
$$R_{ac} = R_C || R_L$$

$$v_o = v_{ce} = -i_c R_{ac}$$

Let us now define the AC+DC output signals i_C and v_{CE} as follows

$$i_C = i_c + I_{CQ}$$

$$v_{CE} = v_{ce} + V_{CEQ}$$



Now let us express the AC output equation $v_{ce} = -i_c R_{ac}$ in terms of v_{CE} and i_C so that we can draw this equation over the output characteristics curve as the AC load line equation.

$$v_{ce} = -i_c R_{ac}$$

$$v_{CE} - V_{CEQ} = -(i_C - I_{CQ}) R_{ac}$$

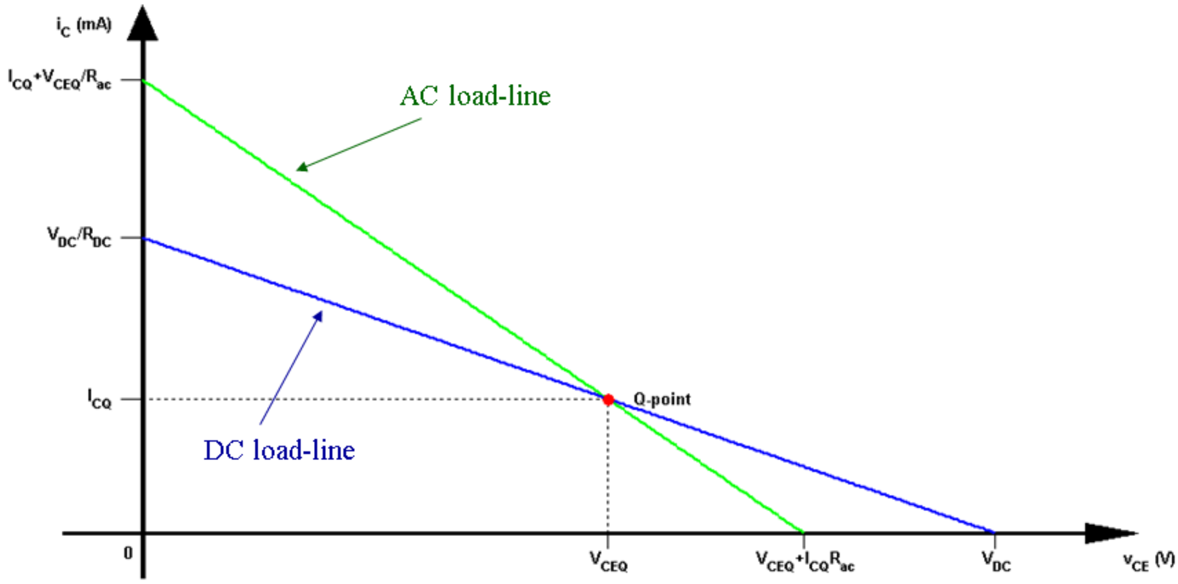
$$v_{CE} = -i_C R_{ac} + V_{CEQ} + I_{CQ} R_{ac}$$

Thus, the rearranged **AC load line equation** (AC output equation) is given by

$$\boxed{i_C = \frac{-1}{R_{ac}} v_{CE} + I_{CQ} + \frac{V_{CEQ}}{R_{ac}}}$$

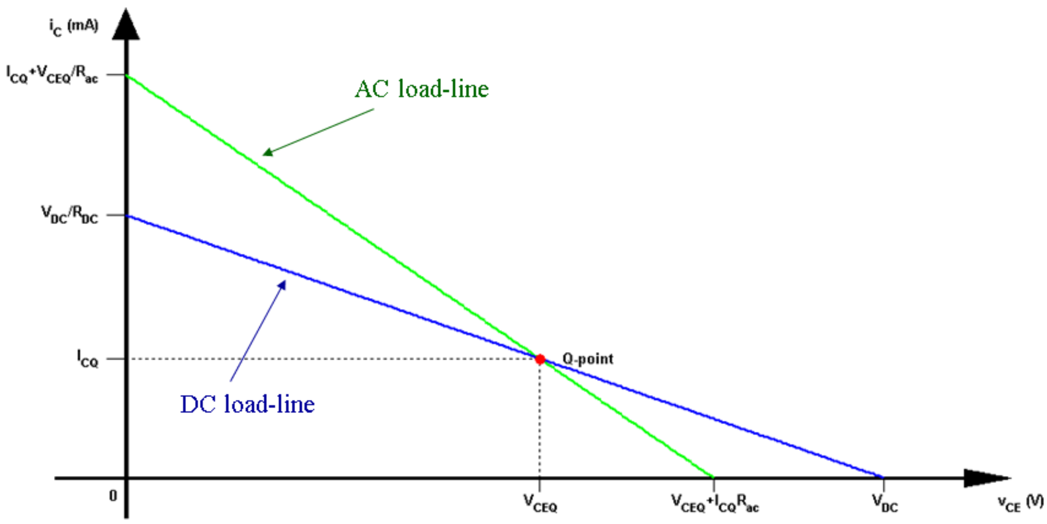
AC-DC Load Lines

Let us draw DC ($V_{CE} = v_{ce} + V_{CEQ}$) and AC ($v_{CE} = -i_C R_{ac} + V_{CEQ} + I_{CQ} R_{ac}$) load lines together as shown below.



Output swings are defined with respect to the ***Q*-point** (I_{CQ}, V_{CEQ}) and the **AC load line end points** on the axes.

Homework 1: Show that AC and DC load lines are the **same** if $R_{DC} = R_{ac}$.



Once the Q-point is known, i.e., the resistor values are given, **peak** values of the **maximum undistorted** voltage and current **swings** $v_{ce(p)(\text{max})}$ and $i_{c(p)(\text{max})}$ are given by

$$\boxed{v_{ce(p)(\text{max})} = \min\left(V_{CEQ}, I_{CQ} R_{ac}\right)}$$

and

$$i_{c(p)(\text{max})} = \min\left(I_{CQ}, \frac{V_{CEQ}}{R_{ac}}\right)$$

Maximum Symmetric Undistorted Swing Design

If we want design our circuit (i.e., select appropriate values for the resistors) in order to obtain the maximum available undistorted swing, i.e., to obtain $\max\left(\min\left(V_{CEQ}, I_{CQ}R_{ac}\right)\right)$, then we obtain the following condition

$$\boxed{V_{CEQ} = I_{CQ}R_{ac}}$$

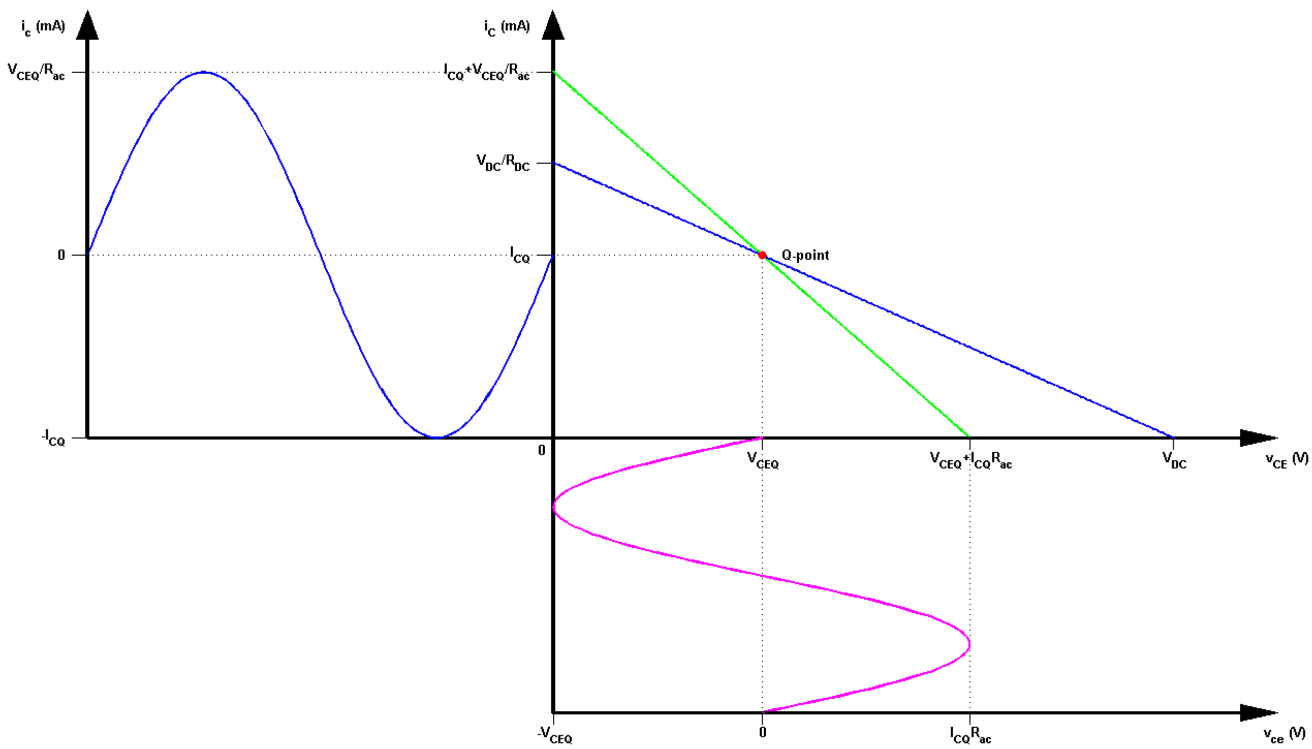
Thus, ***Q*-point** must be in the **middle** of the **AC load line**. In other words, maximum available negative and positive swings are symmetric.

Combining this AC load line requirement with the DC load-line equation $V_{CE} = V_{CC} - I_C R_{DC}$, we find that we have to select the Q-point collector current as

$$\boxed{I_{CQ} = \frac{V_{CC}}{R_{DC} + R_{ac}}}$$

In order to attain this Q-point, we need to select appropriate values for the resistors in the BE loop to obtain $I_{BQ} = \frac{I_{CQ}}{\beta}$.

Once we obtained the desired Q-point in the middle of the AC load line, then the maximum available undistorted output swings will be obtained as shown below.



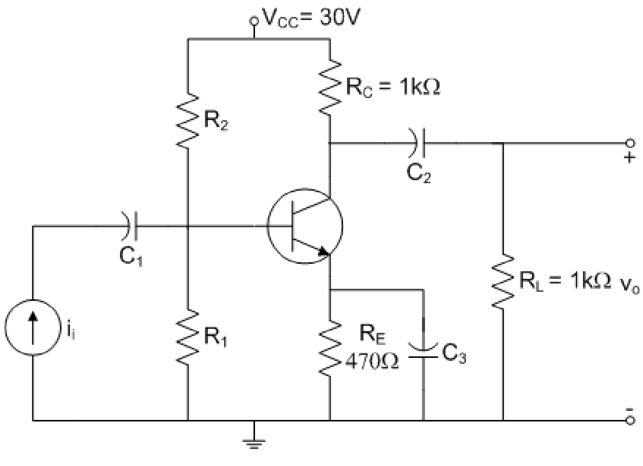
Other Amplifier Configurations

We developed and plotted AC-DC load lines for the common-emitter configuration. Now, let us look at other configurations.

- Common-base (CB) configuration
  1. Obtain R_{ac} from the CB loop.
  2. Obtain R_{DC} from the CE loop.
  3. Draw the AC-DC load lines i_C vs. v_{CE} as before.

  NOTE: You can also draw the AC-DC load lines as i_C vs. v_{CB} by shifting the voltage axis by $V_{BE(ON)}$ volts to the left as $V_{CBQ} = V_{CEQ} - V_{BE(ON)}$. Thus, current axis will be drawn at
  $V_{CB(sat)} = V_{CE(sat)} - V_{BE(ON)} = 0 - V_{BE(ON)} = -V_{BE(ON)}$ volts not at $0\,$V.
- Common-collector (CC) configuration (also known as emitter-follower)
  1. Obtain R_{ac} and R_{DC} from the CE loop as before.
  2. Draw the AC-DC load lines i_E vs. v_{CE}.

  NOTE: As $i_E \cong i_C$, it will be the same as drawing i_C vs. v_{CE}.
- For pnp transistors, we express the currents in the reverse direction (i.e., having positive current values) and reverse the polarity of the terminal voltages (i.e., having positive voltage values), and then draw the AC-DC load lines, e.g., i_C vs. v_{EC}.



Example 1: Consider the circuit above with $I_{BQ} = 50\,\mu$A, $I_{CQ} = 13\,$mA and $\alpha \cong 1$.

a) If $i_i = 50\,\mu\text{A}\sin(\omega t)$, find i_C and v_{CE}.

b) Plot AC and DC load lines together with the output voltage and current swings.

Solution: Here $\beta_{ac} = \beta_{DC} = \beta = \frac{I_{CQ}}{I_{BQ}} = \frac{13m}{50\mu} = 260$,
$R_{DC} = R_C + R_E = 1k + 0.47k = 1.47\,\text{k}\Omega$ and $R_{ac} = R_C || R_L = 1k||1k = 0.5\,\text{k}\Omega$.
So, we can find V_{CEQ} as

$$V_{CEQ} = V_{CC} - I_{CQ}R_{DC} = 30 - (13m)(1.47k) = 10.89\,\text{V}\sin(\omega t)).$$

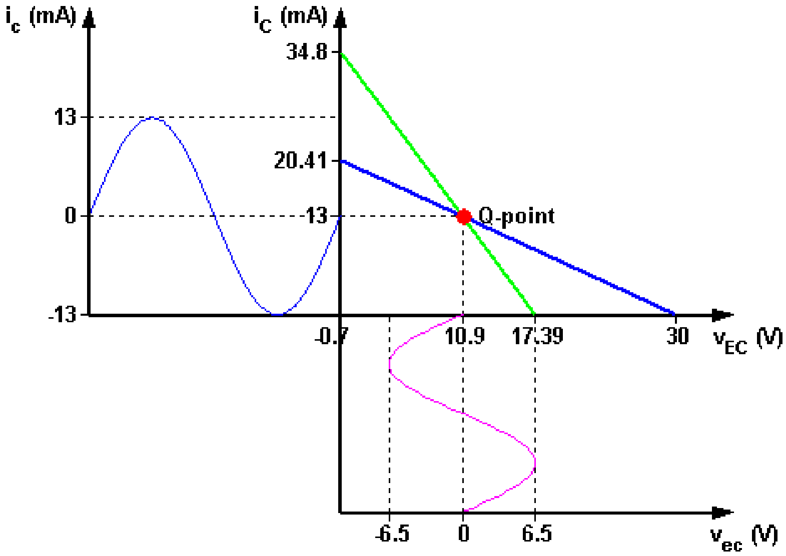
As $i_b \cong i_i$, we can find i_c and v_{ce} as

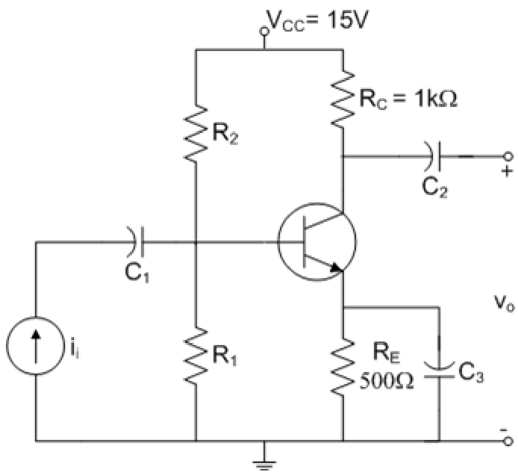
$$i_c = \beta_{ac} i_b \cong \beta i_i = (260)(50\mu) = 13\,\text{mA}\sin(\omega t)$$
$$v_{ce} = -i_c R_{ac} = -(13m)(0.5k) = -6.5\,\text{V}\sin(\omega t)).$$

We find i_C and v_{CE} as

$$i_C = I_{CQ} + i_c = 13\,\text{mA} + 13\,\text{mA}\sin(\omega t)$$
$$v_{CE} = V_{CEQ} + v_{ce} = 10.89\,\text{V} - 6.5\,\text{V}\sin(\omega t)$$

Thus, the AC-DC load-lines are shown below





Example 2: Consider the circuit above with $\alpha \cong 1$.

a) Determine the Q-point in order to obtain maximum undistorted current swing.

b) Draw AC and DC load lines.

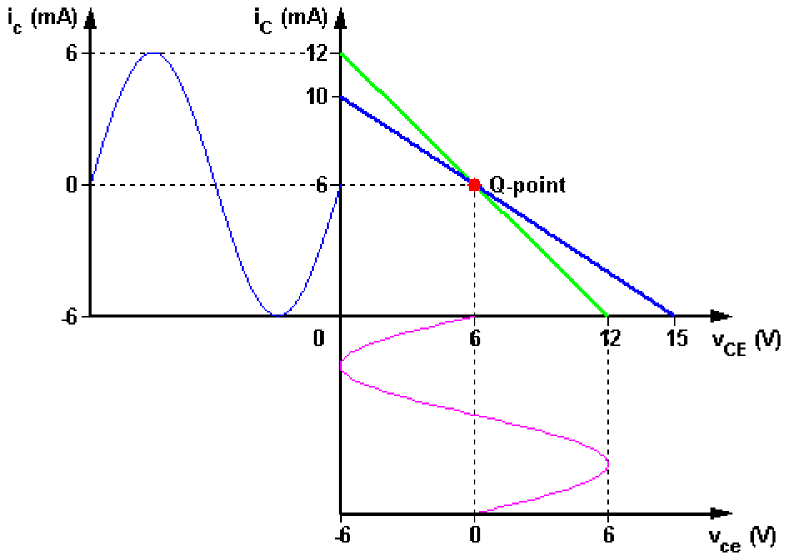
Solution: We can design this circuit to have maximum symmetric undistorted output swing and select R_1 and R_2 values accordingly. So, from the figure $R_{DC} = R_C + R_E = 1k + 0.5k = 1.5\,\text{k}\Omega$ and $R_{ac} = R_C = 1\,\text{k}\Omega$. Thus,

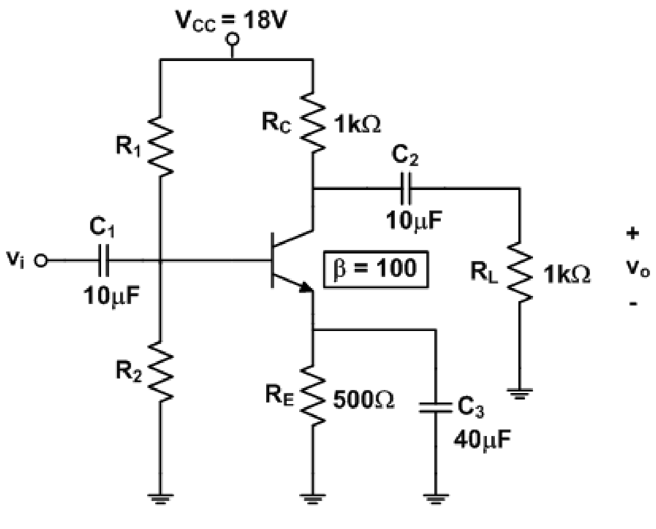
$$I_{CQ} = \frac{V_{CC}}{R_{DC} + R_{ac}} = \frac{15}{1.5k + 1k} = 6\,\text{mA}$$
$$V_{CEQ} = V_{CC} - I_{CQ} R_{DC} = 15 - (6m)(1.5k) = 6\,\text{V}$$

Maximum available swings i_c and v_{ce} are given as

$$i_c = 6\,\text{mA}\sin(\omega t)$$
$$v_{ce} = -6\,\text{V}\sin(\omega t)$$

Consequently, the AC-DC load-lines are shown below





Example 3: (2004-2005 MI) Consider the common-emitter BJT amplifier in the figure above.

a) Explain briefly the effects of the capacitors C_1, C_2 and C_3 on DC biasing and AC operation.

b) Design the DC bias (I_{CQ} and V_{CEQ}) for the **maximum undistorted output swing** and then find the values of R_1 and R_2 which satisfies this condition. Take $\beta R_E \geq 10(R_1||R_2)$, $V_{BE(ON)} = 0.7\,\text{V}$ and $\beta = 100$.

c) Draw the DC and AC load lines for this circuit and show the maximum voltage and current swings on the graph. Also, express these current and voltage swings in written form with their AC and DC components.

Solution: a. Capacitors are open-circuit in DC operation. Thus, C_1 and C_2 are called the coupling capacitors for the protection of the Q-point of the amplifier from the input and output circuitries by preventing the circulation/leakage of DC signals and enabling only AC signals in and out. C_3 is called the emitter bypass capacitor ensuring the stability of the Q-point by enabling the emitter resistor to be in effect in DC operation and increasing the AC gain by bypassing the emitter resistor in AC operation.

b. We can design this circuit to have maximum symmetric undistorted output swing and select R_1 and R_2 values accordingly. So, from the figure
$R_{DC} = R_C + R_E = 1k + 0.5k = 1.5\,\text{k}\Omega$ and $R_{ac} = R_C||R_L = 1k||1k = 0.5\,\text{k}\Omega$. Thus,

$$I_{CQ} = \frac{V_{CC}}{R_{DC} + R_{ac}} = \frac{18}{1.5k + 0.5k} = 9\,\text{mA}$$
$$V_{CEQ} = V_{CC} - I_{CQ}R_{DC} = 18 - (9m)(1.5k) = 4.5\,\text{V}$$

As $I_{EQ} \cong I_{CQ} = 9\,\text{mA}$, base voltage V_{BQ} is given by

$$V_{BQ} = V_{BE(ON)} + I_{EQ}R_E = 0.7 + (9m)(0.5k) = 5.2\,\text{V}.$$

By making the assumption $\beta R_E \geq 10(R_1||R_2)$, we can ignore the base current I_{BQ} and directly apply the voltage divider rule as

$$\frac{R_2}{R_1 + R_2}V_{CC} \cong V_{BQ}$$
$$\frac{R_1 + R_2}{R_2} = \frac{V_{CC}}{V_{BQ}}$$
$$\frac{R_1}{R_2} = \frac{V_{CC}}{V_{BQ}} - 1 = \frac{18}{5.2} - 1 = 2.46.$$

Let us take the highest value of $R_{BB} = R_1||R_2$ in order to reduce the currents through R_1 and R_2 as

$$R_{BB} = R_1||R_2 = \beta R_E/10 = 100 * 0.5/10 = 5\,\text{k}\Omega$$

If we take $a = \frac{R_1}{R_2} = 2.46$, then $R_{BB} = \frac{a}{a+1}R_2$. So, R_2 is given by

$$R_2 = \frac{a+1}{a}R_{BB} = \frac{2.46 + 1}{2.46}5k = 7.03\,\text{k}\Omega$$

Thus, R_1 is given by

$$R_1 = aR_2 = (2.46)(7.03k) = 17.29\,\text{k}\Omega$$

c. AC+DC output current i_C and output voltage v_{CE} are given by

$$i_C = I_{CQ} + i_c = 9\,\text{mA} + 9\,\text{mA}\sin(\omega t)$$
$$v_{CE} = V_{CEQ} + v_{ce} = 4.5\,\text{V} - 4.5\,\text{V}\sin(\omega t)$$

Consequently, the AC-DC load-lines are shown below