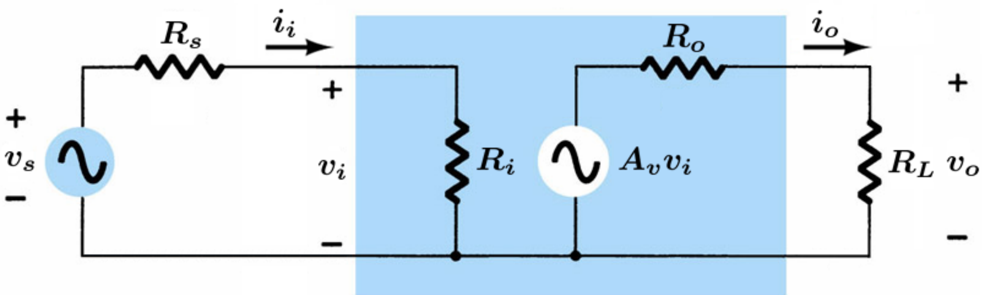
Contents

Purpose of SSAC Analysis

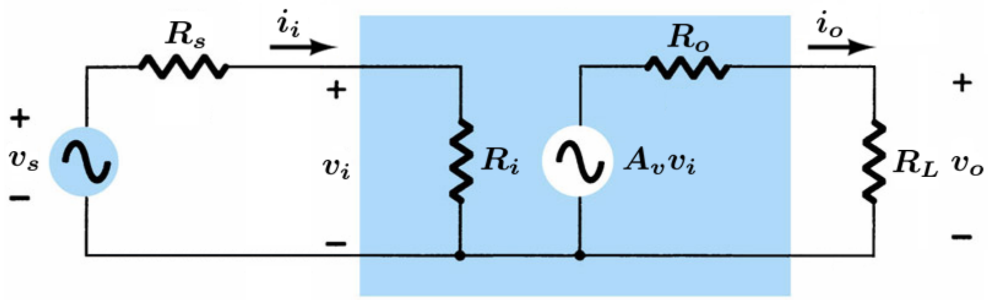
The purpose of small-signal AC (SSAC) analysis to determine the **three** parameters of an amplifier **input resistance**, **output resistance** and **gain**. In this course, we are mostly interested in the two-port voltage-gain amplifier model shown below.



- Input resistance R_i is defined by the no-load input voltage of the amplifier divided by the no-load input current to the amplifier, i.e.,

$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L=\infty}$$

NOTE: Input resistance **cannot** include the source resistance R_s.



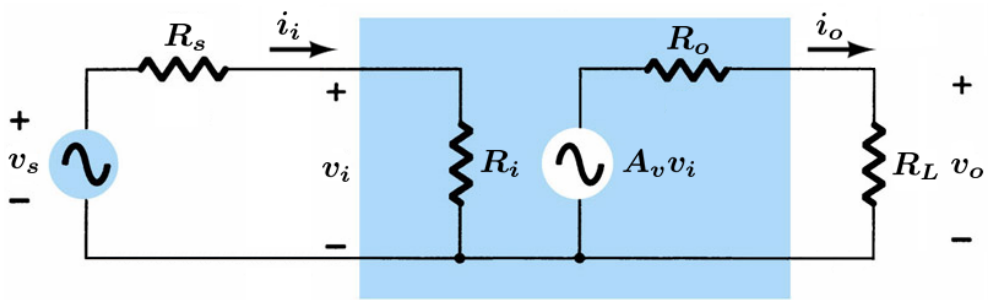
- Output resistance R_o is obtained by the test-voltage method, i.e., by dividing the test voltage value with the measured test current value. In the test-voltage method, load is replaced with a test voltage $v_{\textsf{test}}$ and the independent power sources (v_s or i_s) are killed, i.e., $v_s = 0$ or $i_s = 0$. Thus, output resistance R_o is given by

$$R_o = \left.\frac{v_{\textsf{test}}}{i_{\textsf{test}}}\right|_{v_s=0,\, R_L=v_{\textsf{test}}}$$

NOTE: Output resistance **cannot** include the load resistance R_L.

- No-load voltage gain A_v (or $A_{V_{\textsf{NL}}}$) is defined by

$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$$



- When load is connected, the voltage gain will decrease due to the voltage-divider consisting of R_L and R_o. So, voltage gain with load, A_V, is given by

$$A_V = \frac{v_o}{v_i} = \left(\frac{v_o}{A_v v_i}\right)\left(\frac{A_v v_i}{v_i}\right) = \frac{R_L}{R_o + R_L} A_v$$

- Current gain A_i is defined by the output current versus the input current, i.e.,

$$A_i = \frac{i_o}{i_i} = \frac{v_o / R_L}{v_i / R_i} = \frac{R_i}{R_L} A_V = \frac{R_i}{R_o + R_L} A_v$$

- Finally, overall voltage gain A_{Vs} is given by

$$A_{Vs} = \frac{v_o}{v_s} = \frac{R_L}{R_o + R_L} A_v \frac{R_i}{R_s + R_i}$$

BJT SSAC Analysis Steps

1. Draw the SSAC equivalent circuit
   a) Draw the AC equivalent circuit (signal frequency is infinity, i.e., $f = \infty$)
      i. Capacitors are short circuit, i.e., $X_C \to 0$.
      ii. Kill the DC power sources (i.e., AC value of DC sources is zero).
   b) Replace BJT with its small-signal equivalent model (e.g., hybrid equivalent model or r_e model).

2. Calculate the three amplifier parameters: R_i, R_o and A_v
   a) Calculate no-load input resistance, $R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty}$.
   b) Calculate output resistance, R_o.
   c) Calculate no-load voltage gain, $A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$.

BJT Small-Signal Models

A small-signal model is an equivalent circuit that represents the SSAC characteristics of the transistor. It uses circuit elements that approximate the behavior of the transistor.
Two commonly used models used in SSAC analysis of BJTs are given below:

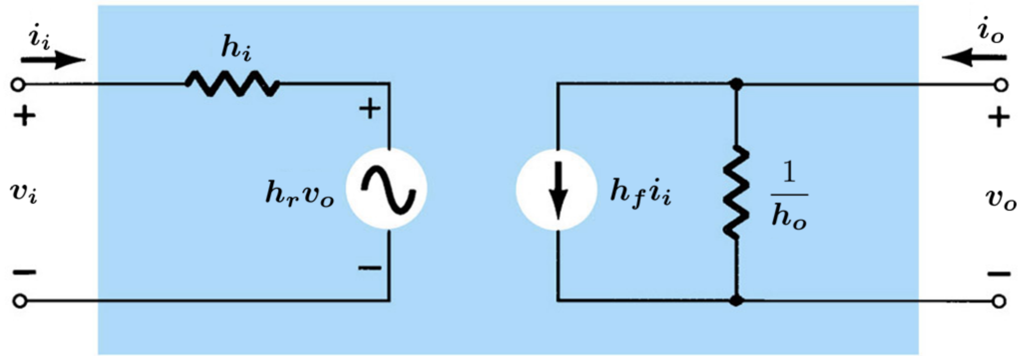
- hybrid equivalent model
- r_e model

Mostly, we are going to use the **hybrid equivalent model**. But, we are going to introduce and provide results for the r_e model as well.

NOTE: Small-signal equivalent model and its analysis are the same for both npn and pnp transistors.

Hybrid Equivalent Model

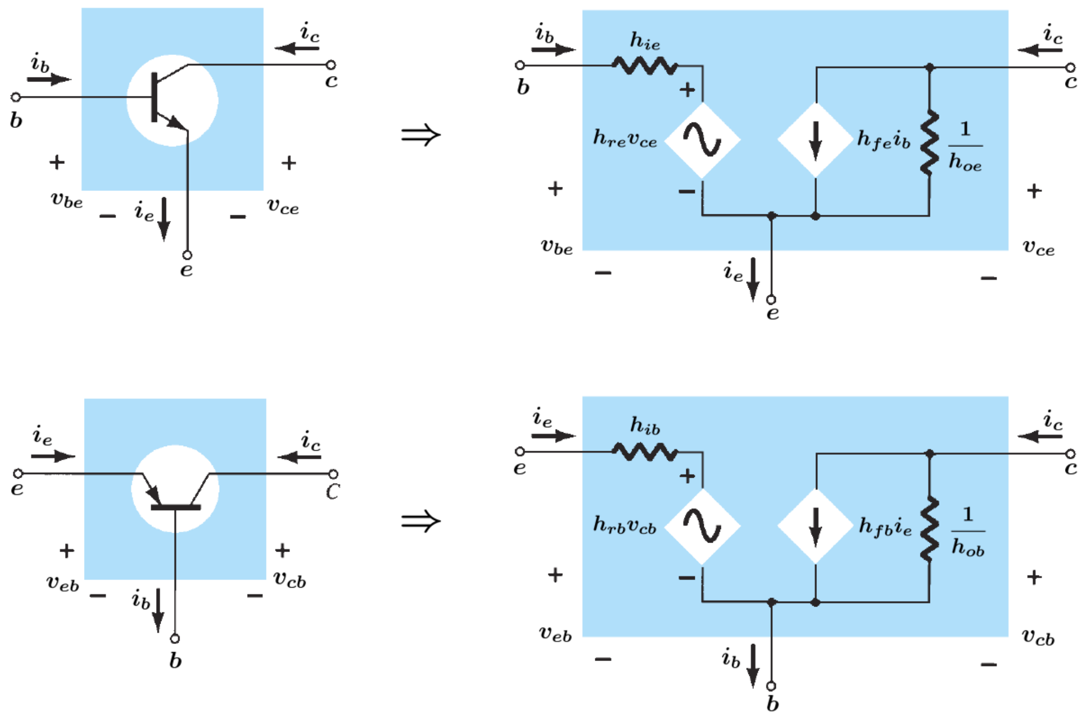
Parameters of the hybrid equivalent circuit provide the entire set on the specification sheet of a BJT and cover all operating conditions. Generalized hybrid equivalent circuit for any transistor configuration is provided below.



Here,

- h_i: input resistance
- h_r: reverse transfer voltage ratio (v_i/v_o)
- h_f: forward transfer current ratio (i_o/i_i)
- h_o: output conductance

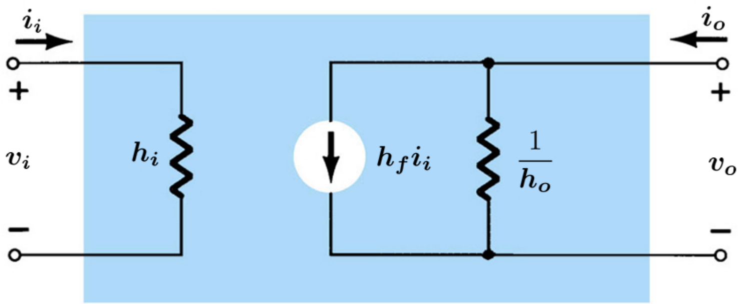
For a specific configuration, the model parameters modified with the label of the common-mode terminal in their subscript. So, common-emitter and common-base configurations and their hybrid equivalent models are shown below, respectively.



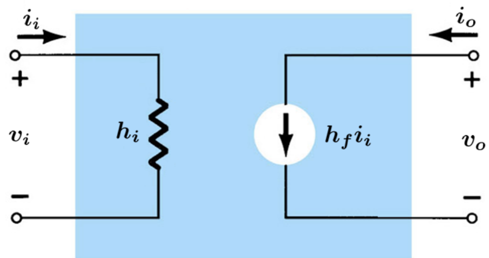
- For the common-collector configuration, we always use the common-emitter hybrid equivalent model.

Simplified Hybrid Equivalent Model

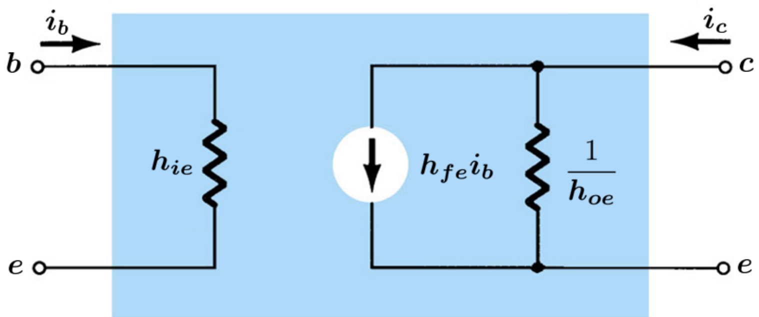
Because h_r is normally a relatively small quantity, its removal is approximated by $h_r \approx 0$ and $h_r v_o = 0$, resulting in the simplified hybrid equivalent circuit shown below. In this course, we are going to use the **simplified hybrid equivalent model**.



This circuit, can be further simplified if a value for the parameter h_o or $1/h_o$ is not provided. In that case, we can safely assume that $h_o = 0$ or $1/h_o = \infty$ resulting in the approximate hybrid equivalent circuit shown below.



Common-Emitter Hybrid Equivalent Model



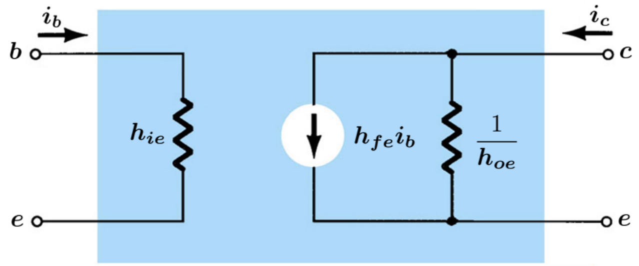
Here, the h-parameters are defined as below

$$h_{ie} = \left.\frac{\partial V_{BE}}{\partial I_B}\right|_{Q\text{-point}} = \frac{\gamma}{I_{BQ}} \quad \text{...see diode dynamic resistance section}$$

$$h_{fe} = \left.\frac{\partial I_C}{\partial I_B}\right|_{Q\text{-point}} = \beta_{ac}$$

$$1/h_{oe} = \left.\frac{\partial V_{CE}}{\partial I_C}\right|_{Q\text{-point}} = \frac{V_A + V_{CEQ}}{I_{CQ}} \quad \text{...} V_A \text{ is the early voltage and } V_A \gg V_{CEQ}$$

Typical values of h_{fe} run from 50 to 200, h_{ie} run from $500\,\Omega$ to $7\,\text{k}\Omega$, and $1/h_{oe}$ run from $40\,\text{k}\Omega$ to $100\,\text{k}\Omega$.

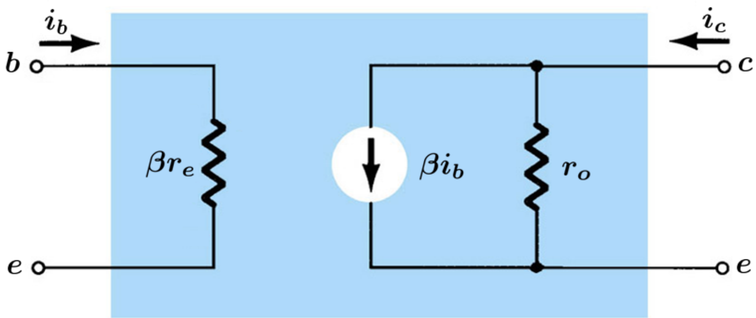


Note that, as $I_{CQ} = \beta I_{BQ}$ and $I_{EQ} = (\beta + 1) I_{BQ}$, we can also express h_{ie} in terms of I_{CQ} or I_{EQ} as follows

$$\begin{aligned} h_{ie} &= \frac{\gamma}{I_{BQ}} \\ &= h_{fe} \frac{\gamma}{I_{CQ}} \\ &= (h_{fe} + 1) \frac{\gamma}{I_{EQ}} \end{aligned}$$

where $\gamma = kT/q$ is the thermal voltage and have fixed values for a given temperature, e.g., $\gamma = 26\,\text{mV}$ at room temperature $T = 300\,\text{K}$.

Common-Emitter r_e Equivalent Model

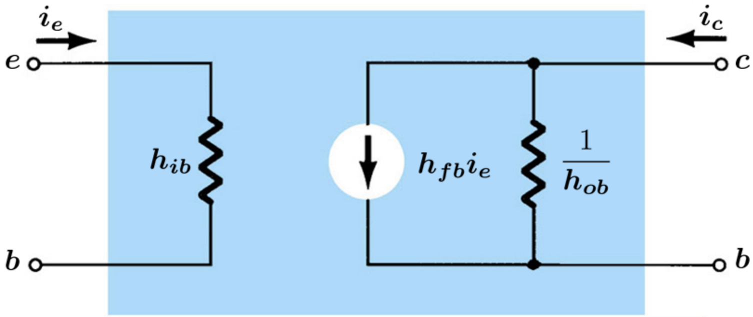


One-to-one correspondence with the h-parameters are given below,

$$\begin{aligned} h_{fe} &= \beta \\ h_{ie} &= (\beta + 1) r_e \cong \beta r_e \\ 1/h_{oe} &= r_o. \end{aligned}$$

Thus, $\beta = h_{fe}$, $\beta r_e = h_{ie}$ and $r_o = 1/h_{oe}$.

Common-Base Hybrid Equivalent Model



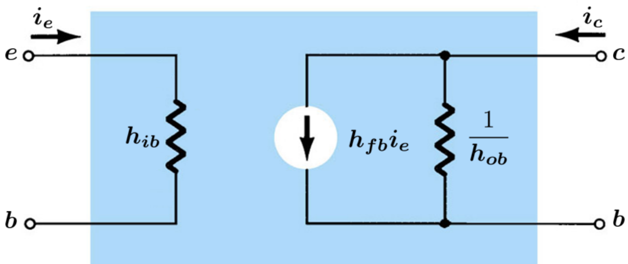
Here, the h-parameters are defined as below,

$$h_{ib} = \left.\frac{\partial V_{BE}}{\partial I_E}\right|_{Q\text{-point}} = \frac{\gamma}{I_{EQ}} \quad \text{...see diode dynamic resistance section}$$

$$h_{fb} = -\left.\frac{\partial I_C}{\partial I_E}\right|_{Q\text{-point}} = -\alpha_{ac} \cong -1$$

$$1/h_{ob} = \left.\frac{\partial V_{CB}}{\partial I_C}\right|_{Q\text{-point}} \approx \infty$$

Typically, $h_{fb} = -1$, and h_{ib} run from $5\,\Omega$ to $50\,\Omega$, and $1/h_{ob}$ is in the megohm range. Thus, $1/h_{ob} \gg 1/h_{oe}$.

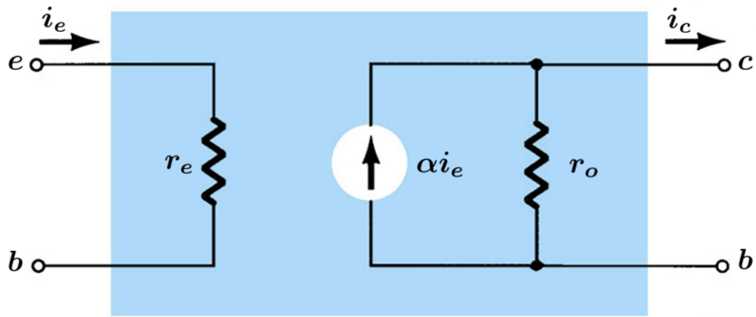


Note that, the relationship between h_{ib} and h_{ie} is given below

$$h_{ie} = \left(h_{fe} + 1\right) h_{ib}$$

or $h_{ib} = \dfrac{h_{ie}}{h_{fe} + 1}$.

Common-Base r_e Equivalent Model



One-to-one correspondence with the h-parameters are given below

$$h_{fb} = -\alpha$$
$$h_{ib} = r_e$$
$$1/h_{ob} = r_o.$$

Thus, $\alpha = -h_{fb} \cong 1$, $r_e = h_{ib}$ and $r_o = 1/h_{ob} \cong \infty$. Note that, minus sign is due to the direction of the current source.

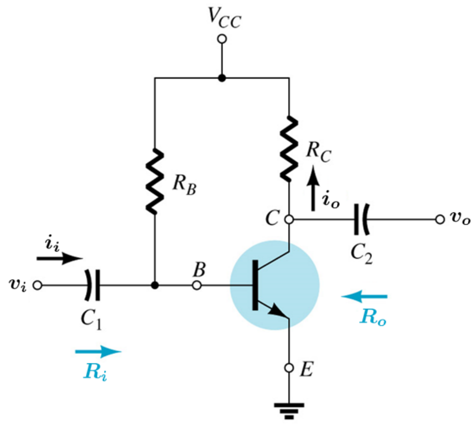
Phase Relationship

The phase relationship between input and output depends on the amplifier configuration circuit as listed below.

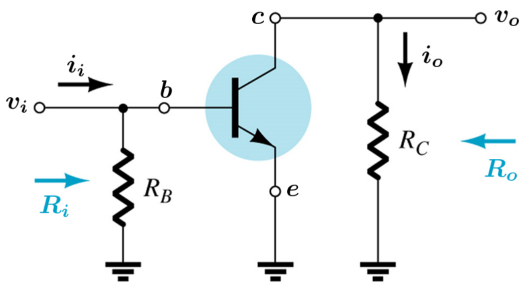
- Common-Emitter: 180 degrees
- Common-Base: 0 degrees
- Common-Collector: 0 degrees (Emitter-Follower)

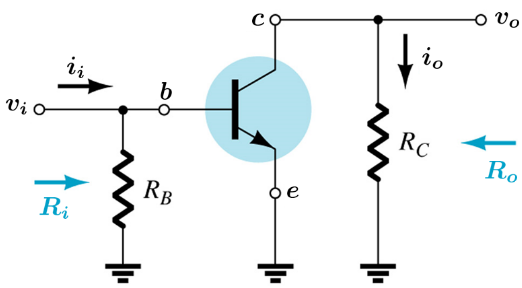
Common-Emitter Fixed-Bias Configuration

Common-emitter fixed-bias configuration is given below

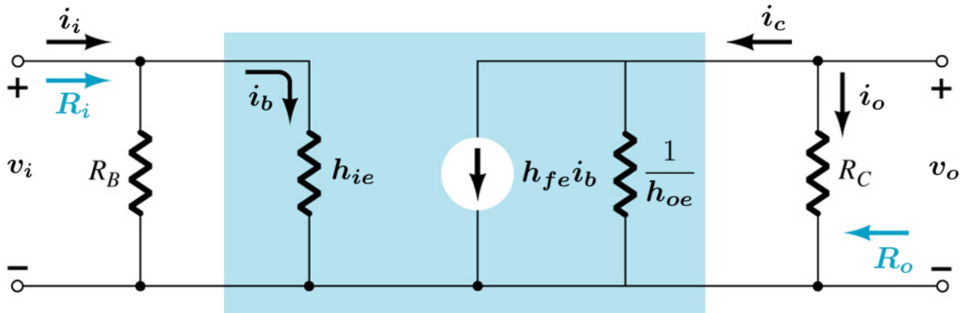


Let us start SSAC analysis by drawing the AC equivalent circuit as shown below





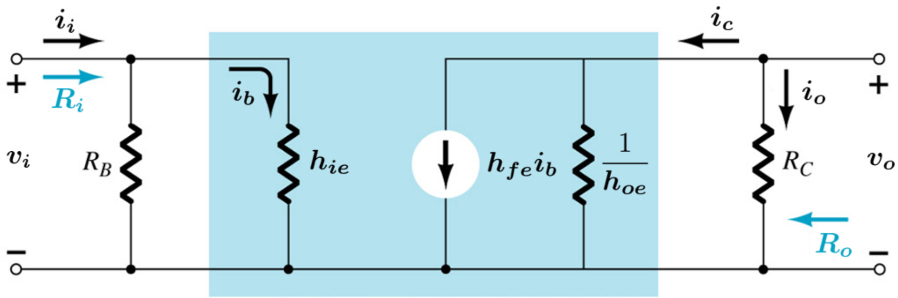
Then, we are going to replace BJT with its common-emitter hybrid equivalent model as shown below



- Obtain h_{fe} and $1/h_{oe}$ from the specification sheet of the transistor or by testing the transistor using a curve tracer. Calculate h_{ie} using the DC analysis values as

$$h_{ie} = \frac{26\,\text{mV}}{I_{BQ}} = h_{fe}\frac{26\,\text{mV}}{I_{CQ}}.$$

Input Resistance



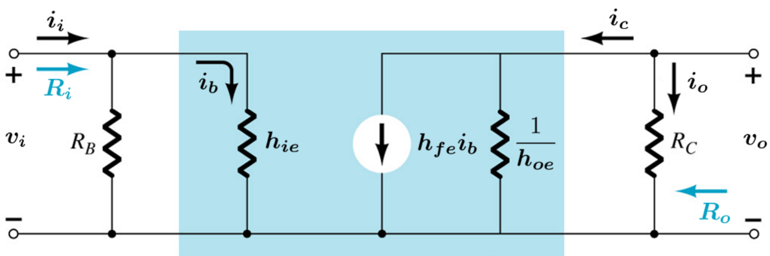
Input resistance R_i is given as

$$R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_B||h_{ie}$$

- If $R_B \geq 10h_{ie}$, then R_i simplifies to $R_i = h_{ie}$.
- Input resistance R_i according to the r_e **model** is given by

$$R_i = R_B||\beta r_e$$

Voltage Gain

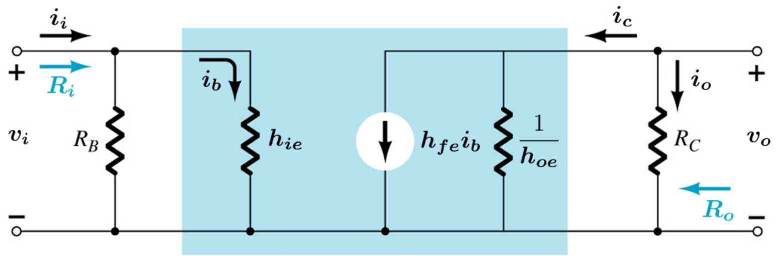


No-load voltage gain A_v is given by

$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \left(\frac{v_o}{h_{fe}i_b}\right)\left(\frac{h_{fe}i_b}{i_b}\right)\left(\frac{i_b}{v_i}\right)$$
$$= (-R_C||1/h_{oe})(h_{fe})\left(\frac{1}{h_{ie}}\right)$$
$$= -\frac{h_{fe}(R_C||1/h_{oe})}{h_{ie}}$$

- No-load voltage gain A_v according to the r_e **model** is given by

$$A_v = -\frac{R_C||r_o}{r_e}$$



- If $1/h_{oe} \geq 10R_C$, no-load voltage gain A_v reduces to

$$A_v = -\frac{h_{fe}R_C}{h_{ie}} \qquad \ldots r_e \text{ model: } A_v = -\frac{R_C}{r_e}$$

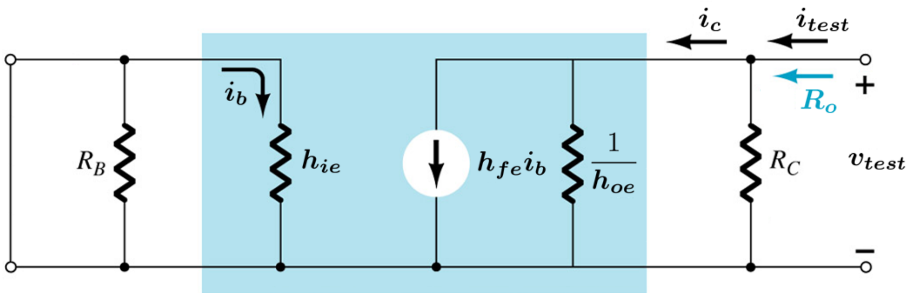
- For the circuit above, we can obtain the current gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_C}{v_i/R_i} = \frac{R_i}{R_C}\frac{v_o}{v_i} = \frac{R_i}{R_C}A_v$$

- If $1/h_{oe} \geq 10R_C$ and $R_B \geq 10h_{ie}$, current gain A_i reduces to

$$A_i = -h_{fe} \qquad \ldots r_e \text{ model: } A_i = -\beta$$

Output Resistance



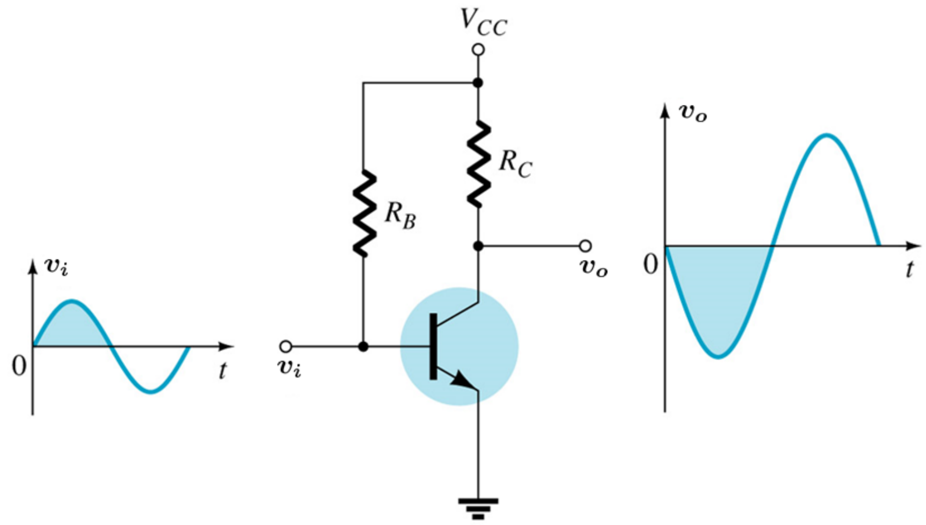
Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above. Note that in the circuit $i_b = 0$, so $h_{fe}i_b = 0$ as well.

$$R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_C || 1/h_{oe}$$

- If $1/h_{oe} \geq 10R_C$, then R_o simplifies to $R_o = R_C$.
- Output resistance R_o according to the r_e **model** is given by

$$R_o = R_C || r_o$$

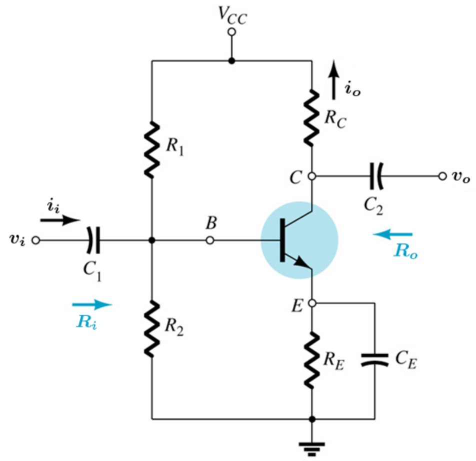
Phase Relationship



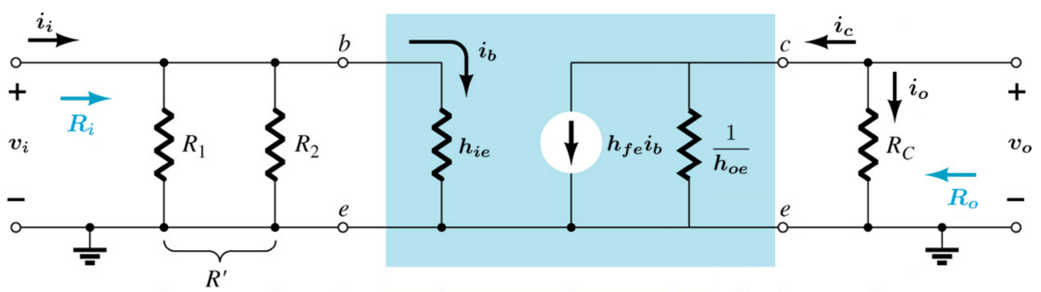
- The phase relationship between input and output is 180 degrees as shown above.
- The negative sign used in the voltage gain formulas indicates the inversion.

CE Voltage-Divider Bias Configuration

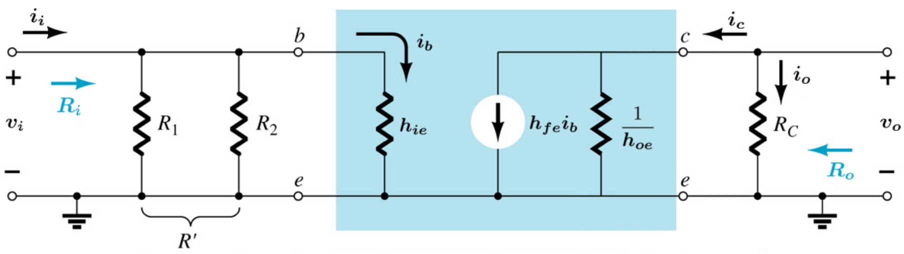
Common-emitter voltage-divider bias configuration is given below



Corresponding SSAC equivalent circuit is shown below



Input Resistance



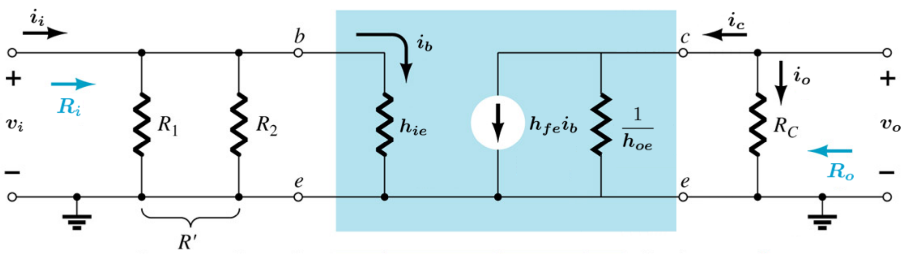
Input resistance R_i is given as

$$R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_1||R_2||h_{ie}$$

- Input resistance R_i according to the r_e **model** is given by

$$R_i = R_1||R_2||\beta r_e$$

Voltage Gain



No-load voltage gain A_v is given by

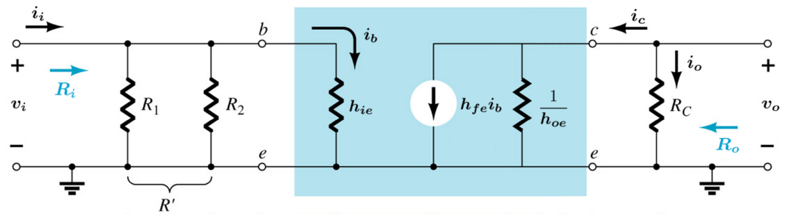
$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \left(\frac{v_o}{h_{fe}i_b}\right)\left(\frac{h_{fe}i_b}{i_b}\right)\left(\frac{i_b}{v_i}\right)$$

$$= (-R_C||1/h_{oe})\,(h_{fe})\left(\frac{1}{h_{ie}}\right)$$

$$= -\frac{h_{fe}\,(R_C||1/h_{oe})}{h_{ie}}$$

- No-load voltage gain A_v according to the r_e **model** is given by

$$A_v = -\frac{R_C||r_o}{r_e}$$



- If $1/h_{oe} \geq 10R_C$, no-load voltage gain A_v reduces to

$$A_v = -\frac{h_{fe}R_C}{h_{ie}} \qquad \ldots r_e \text{ model: } A_v = -\frac{R_C}{r_e}$$

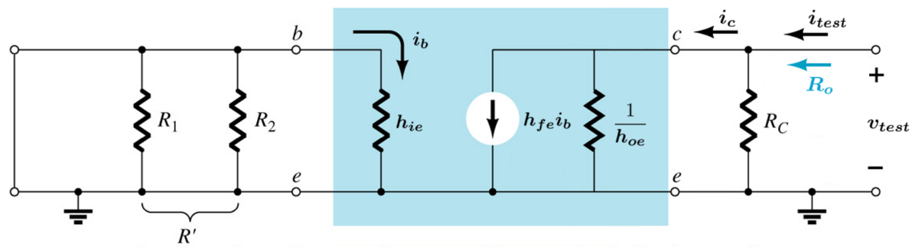
- For the circuit above, we can obtain the current gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_C}{v_i/R_i} = \frac{R_i}{R_C}\frac{v_o}{v_i}$$
$$= \frac{R_i}{R_C}A_v$$

- If $1/h_{oe} \geq 10$, and given $R' = R_1||R_2$, current gain A_i reduces to

$$A_i = -h_{fe}\frac{R'}{R' + h_{ie}} \qquad \ldots r_e \text{ model: } A_i = -\frac{R'}{R'/\beta + r_e}$$

Output Resistance



Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above. Note that in the circuit $i_b = 0$, so $h_{fe}i_b = 0$ as well.

$$R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_C||1/h_{oe}$$

- If $1/h_{oe} \geq 10R_C$, then R_o simplifies to $R_o = R_C$.
- Output resistance R_o according to the r_e **model** is given by

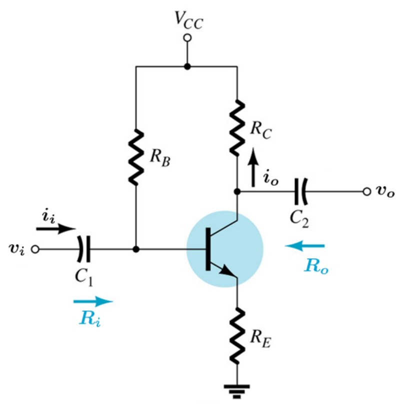
$$R_o = R_C||r_o$$

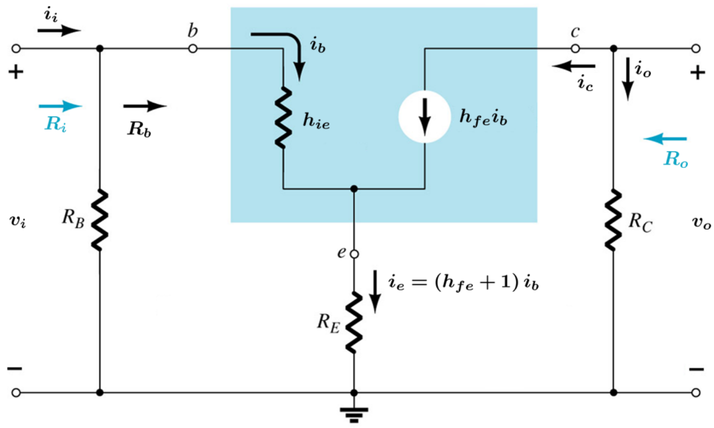
Phase Relationship

- Phase relationship between input and output of a common-emitter amplifier configuration if always 180 degrees. This is independent of the type of the bias-configuration.

CE Unbypassed-Emitter Bias Configuration

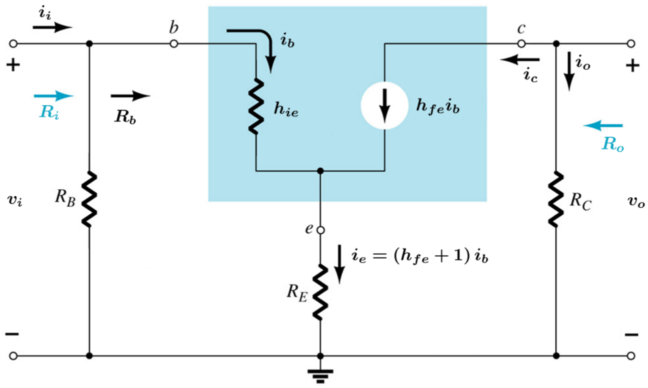
Common-emitter unbypassed-emitter bias configuration and its SSAC equivalent circuit are given on the left and right figures below, respectively.





- When R_E is not bypassed, we normally assume $1/h_{oe} = \infty$ in order to reduce the calculation complexity. Because of the feedback, even $1/h_{oe} \neq \infty$ the results do not really change at all.

Input Resistance



Input resistance R_i is given as

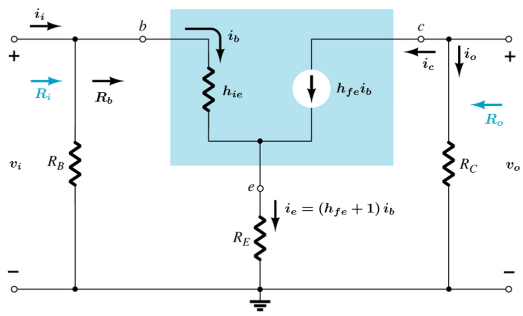
$$R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_B||R_b \qquad \ldots R_b = h_{ie} + (h_{fe}+1)\,R_E$$

$$= R_B||\left[h_{ie} + (h_{fe}+1)\,R_E\right]$$

- Input resistance R_i according to the r_e **model** is given by

$$R_i = R_B||\,(\beta+1)\,(r_e + R_E) \cong R_B||\beta\,(r_e + R_E)$$

Voltage Gain



No-load voltage gain A_v is given by

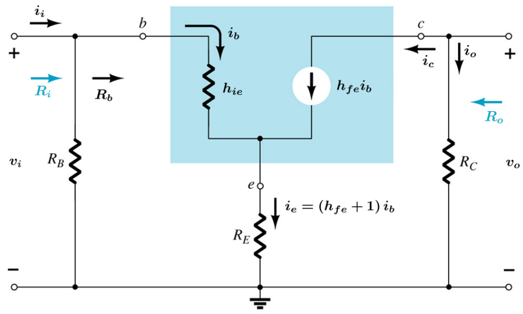
$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \left(\frac{v_o}{h_{fe}i_b}\right)\left(\frac{h_{fe}i_b}{i_b}\right)\left(\frac{i_b}{v_i}\right)$$

$$= (-R_C)\,(h_{fe})\left(\frac{1}{R_b}\right)$$

$$= -\frac{h_{fe}R_C}{h_{ie} + (h_{fe}+1)\,R_E}$$

- No-load voltage gain A_v according to the r_e **model** is given by

$$A_v = -\frac{R_C}{r_e + R_E}$$



- If $(h_{fe}+1)\,R_E \geq 10h_{ie}$, no-load voltage gain A_v reduces to

$$A_v = -\frac{R_C}{R_E} \qquad \ldots r_e \text{ model: } A_v = -\frac{R_C}{R_E}$$

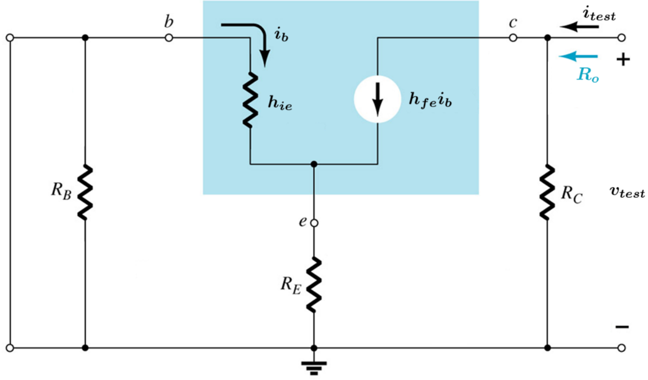
- For the circuit above, we can obtain the current gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_C}{v_i/R_i} = \frac{R_i}{R_C}\frac{v_o}{v_i}$$
$$= \frac{R_i}{R_C}A_v$$

- Resultant current gain A_i is given by

$$A_i = -h_{fe}\frac{R_B}{R_B + R_b} \qquad \ldots r_e \text{ model: } A_i = -\frac{R_B}{R_B/\beta + r_e + R_E}$$

Output Resistance



Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above. Note that in the circuit $i_b = 0$, so $h_{fe}i_b = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_C}$$

- Output resistance R_o according to the r_e **model** is given by

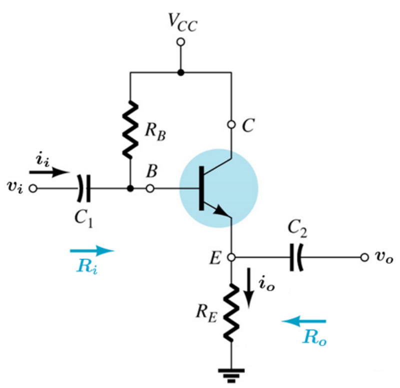
$$R_o = R_C$$

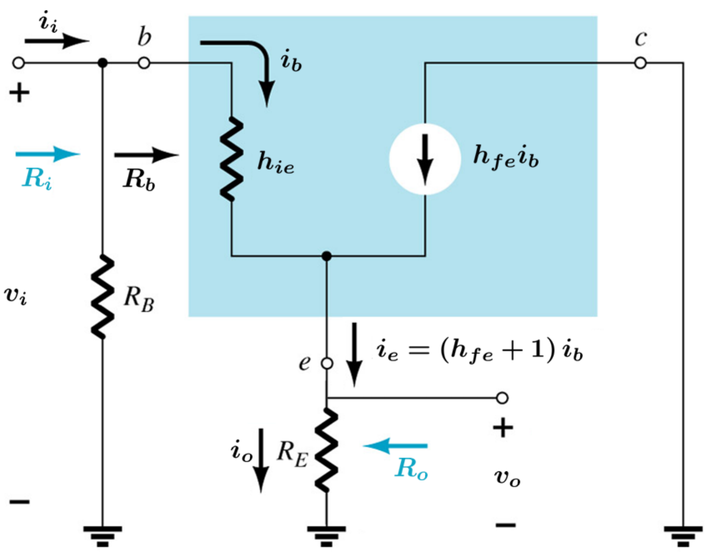
Phase Relationship

- Phase relationship between input and output of a common-emitter amplifier configuration if always 180 degrees. This is independent of the type of the bias-configuration.

Emitter-Follower Configuration

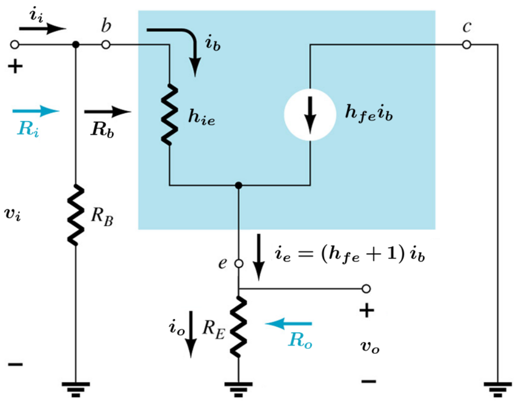
Emitter-follower (common-collector) configuration and its SSAC equivalent circuit are given on the left and right figures below, respectively.





- When R_E is not bypassed, we normally assume $1/h_{oe} = \infty$ in order to reduce the calculation complexity.

Input Resistance



Input resistance R_i is given as

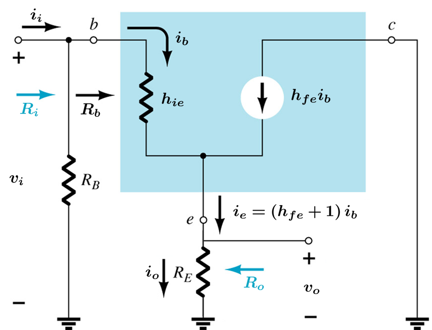
$$R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_B || R_b \qquad \ldots R_b = h_{ie} + (h_{fe} + 1)\, R_E$$

$$= R_B || \left[h_{ie} + (h_{fe} + 1)\, R_E\right]$$

- Input resistance R_i according to the $\boldsymbol{r_e}$ **model** is given by

$$R_i = R_B || (\beta + 1)(r_e + R_E) \cong R_B || \beta (r_e + R_E)$$

Voltage Gain



No-load voltage gain A_v is given by

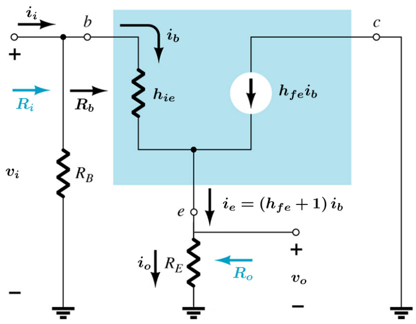
$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \left(\frac{v_o}{i_b}\right)\left(\frac{i_b}{v_i}\right)$$

$$= \left[(h_{fe} + 1)\, R_E\right]\left(\frac{1}{R_b}\right) \qquad \ldots R_b = h_{ie} + (h_{fe} + 1)\, R_E$$

$$= \frac{(h_{fe} + 1)\, R_E}{h_{ie} + (h_{fe} + 1)\, R_E} \cong 1$$

- No-load voltage gain A_v according to the $\boldsymbol{r_e}$ **model** is given by

$$A_v = \frac{R_E}{r_e + R_E} \cong 1$$



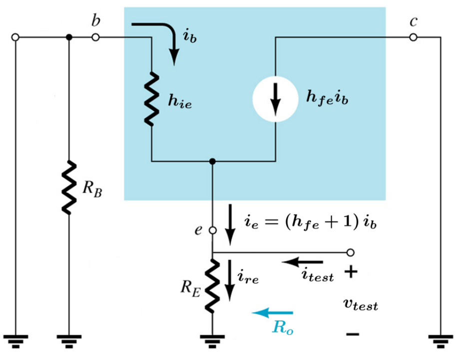
- For the circuit above, we can obtain the current gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_E}{v_i/R_i} = \frac{R_i}{R_E}\frac{v_o}{v_i}$$
$$= \frac{R_i}{R_E}A_v$$

- Resultant current gain A_i is given by,

$$A_i = (h_{fe}+1)\frac{R_B}{R_B+R_b} \qquad \ldots r_e \text{ model: } A_i = \frac{R_B}{R_B/(\beta+1)+r_e+R_E}$$

Output Resistance



Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above.

$$R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_E || \frac{h_{ie}}{h_{fe}+1}$$

- Output resistance R_o according to the r_e **model** is given by

$$R_o = R_E || r_e$$

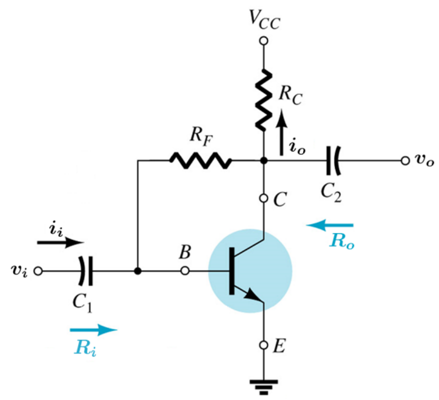
- If $1/h_{oe} \neq \infty$, then replace R_E with $(R_E||1/h_{oe})$ in R_i, A_v and R_o calculations.
- If a voltage source with source resistance R_s is connected to the input, replace h_{ie} with $(h_{ie}+R_B||R_s)$ in R_o calculations.

Phase Relationship

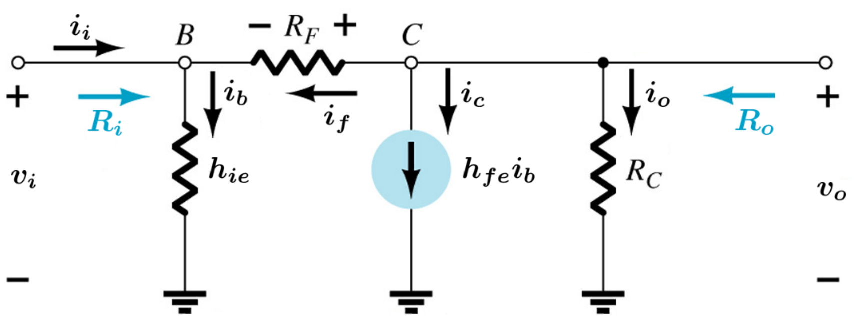
- Emitter-follower (common-collector) configuration has **no phase shift** between input and output.

CE Collector Feedback Configuration

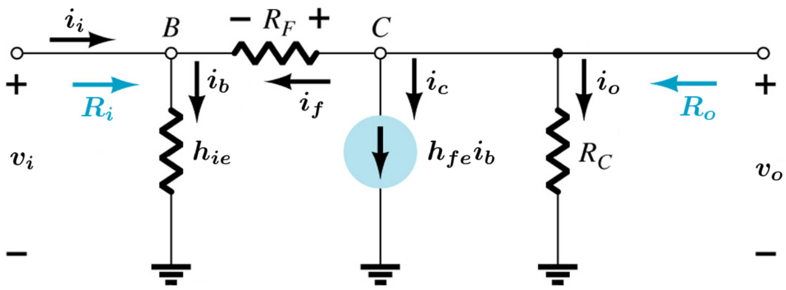
Common-emitter collector feedback bias configuration is given below



Corresponding SSAC equivalent circuit is shown below



Input Resistance



Input resistance R_i is given as

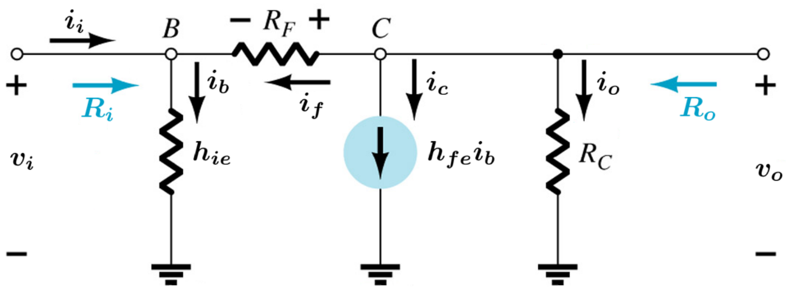
$$R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = \frac{h_{ie}}{1 + \frac{h_{ie}+h_{fe}R_C}{R_F+R_C}} \qquad \ldots i_f = -\frac{h_{ie}+h_{fe}R_C}{R_F+R_C} i_b$$

$$\cong \frac{h_{ie}}{1 + \dfrac{h_{fe}R_C}{R_F+R_C}} \qquad \ldots h_{fe}R_C \gg h_{ie}$$

- Input resistance R_i according to the r_e **model** is given by

$$R_i \cong \frac{\beta r_e}{1 + \dfrac{\beta R_C}{R_F + R_C}}$$

Voltage Gain



No-load voltage gain A_v is given by

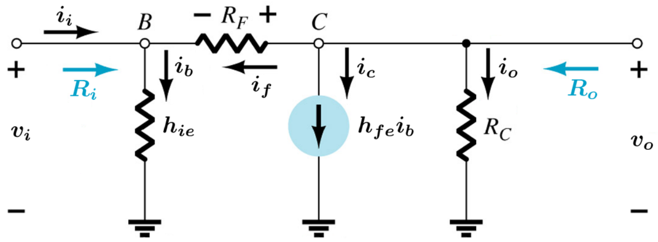
$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \left(\frac{h_{fe}R_F - h_{ie}}{R_F + R_C}\right)\left(\frac{-R_C}{h_{ie}}\right) \qquad \ldots i_f = -\frac{h_{ie}+h_{fe}R_C}{R_F+R_C} i_b$$

$$\cong \left(\frac{h_{fe}R_F}{R_F + R_C}\right)\left(\frac{-R_C}{h_{ie}}\right) \qquad \ldots h_{fe}R_F \gg h_{ie}$$

$$\approx -\frac{h_{fe}R_C}{h_{ie}} \qquad \ldots R_F \gg R_C$$

- No-load voltage gain A_v according to the r_e **model** is given by

$$A_v \approx -\frac{R_C}{r_e}$$



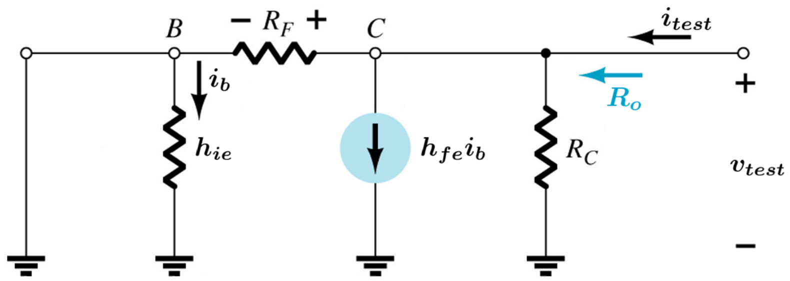
- For the circuit above, we can obtain the current gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_C}{v_i/R_i} = \frac{R_i}{R_C}\frac{v_o}{v_i}$$
$$= \frac{R_i}{R_C}A_v$$

- Resultant current gain A_i is given by,

$$A_i \cong -\frac{h_{fe}\left(R_F + R_C\right)}{R_F + \left(h_{fe}+1\right)R_C} \qquad \ldots r_e \text{ model: } A_i = -\frac{R_F + R_C}{R_F/\beta + R_C}$$

Output Resistance



Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above. Note that in the circuit $i_b = 0$, so $h_{fe}i_b = 0$ as well.

$$R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_C||R_F$$

- Output resistance R_o according to the r_e **model** is given by

$$R_o = R_C||R_F$$

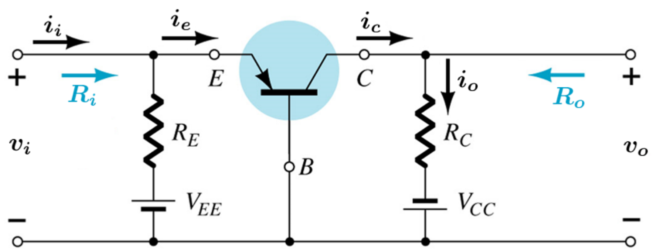
- If $1/h_{oe} \neq \infty$, then replace R_C with $(R_C||1/h_{oe})$ in R_i, A_v and R_o calculations.
- If a voltage source with source resistance R_s is connected to the input, replace R_F with $\left[R_F\left(R_s + h_{ie}\right)/\left(h_{fe}R_s + h_{ie}\right)\right]$ in R_o calculations.

Phase Relationship

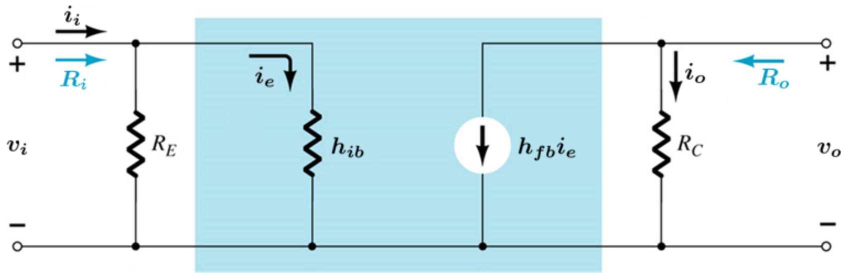
- Phase relationship between input and output of a common-emitter amplifier configuration if always 180 degrees. This is independent of the type of the bias-configuration.

Common-Base Configuration

Common-base configuration is given below

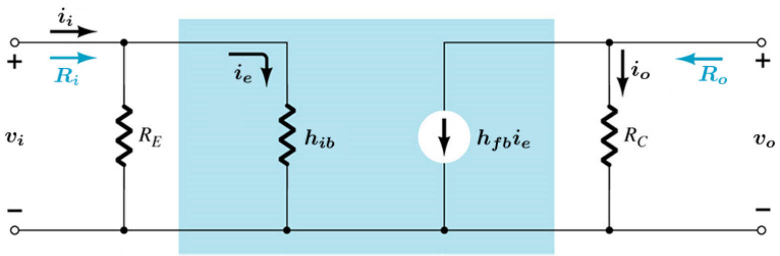


Corresponding SSAC equivalent circuit is shown below



- Here, $h_{ib} = \dfrac{h_{ie}}{h_{fe}+1} = \dfrac{26\,\text{mV}}{I_{EQ}}$ and $h_{fb} = -\alpha_{ac} = -1$.

Input Resistance



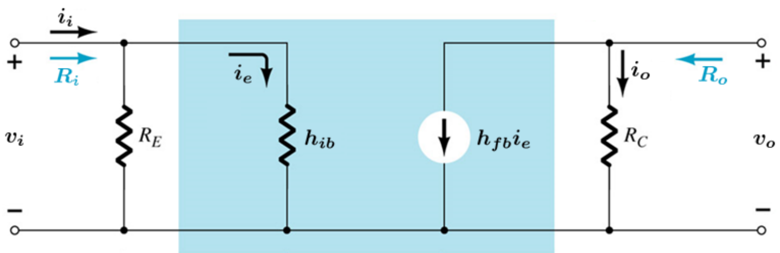
Input resistance R_i is given as

$$R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_E || h_{ib}$$

- If $R_E \geq 10h_{ib}$, then R_i simplifies to $R_i = h_{ib}$.
- Input resistance R_i according to the r_e **model** is given by

$$R_i = R_E || r_e$$

Voltage Gain



No-load voltage gain A_v is given by

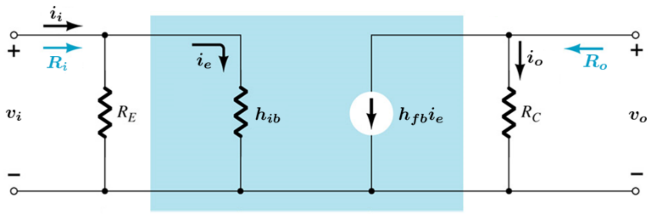
$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \left(\frac{v_o}{h_{fb}i_e}\right)\left(\frac{h_{fb}i_e}{i_e}\right)\left(\frac{i_e}{v_i}\right)$$

$$= (-R_C)(h_{fb})\left(\frac{1}{h_{ib}}\right)$$

$$= \frac{R_C}{h_{ib}} \qquad \ldots h_{fb} = -1$$

- No-load voltage gain A_v according to the r_e **model** is given by

$$A_v = \frac{R_C}{r_e}$$



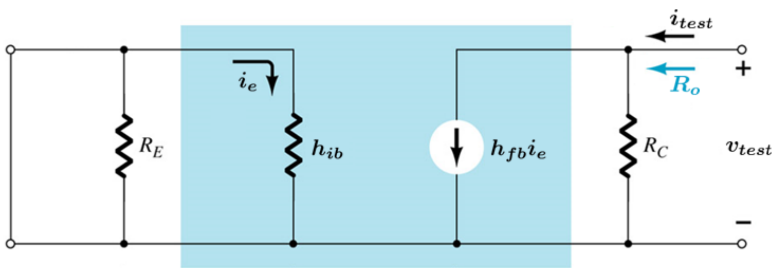
- For the circuit above, we can obtain the current gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_C}{v_i/R_i} = \frac{R_i}{R_C}\frac{v_o}{v_i}$$
$$= \frac{R_i}{R_C}A_v$$

- Resultant current gain A_i is given by,

$$A_i = \frac{R_E||h_{ib}}{h_{ib}} \approx 1 \qquad \ldots r_e \text{ model: } A_i = \frac{R_E||r_e}{r_e} \approx 1$$

Output Resistance



Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above. Note that in the circuit $i_e = 0$, so $h_{fb}i_e = 0$ as well.

$$R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_C$$

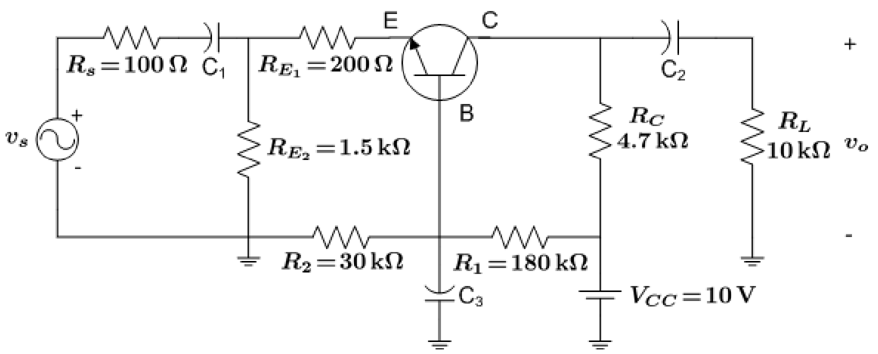
- Output resistance R_o according to the r_e **model** is given by

$$R_o = R_C$$

- If $1/h_{ob} \neq \infty$, then replace R_C with $(R_C||1/h_{ob})$ in R_i, A_v and R_o calculations.

Phase Relationship

- A common-base amplifier configuration has **no phase shift** between input and output

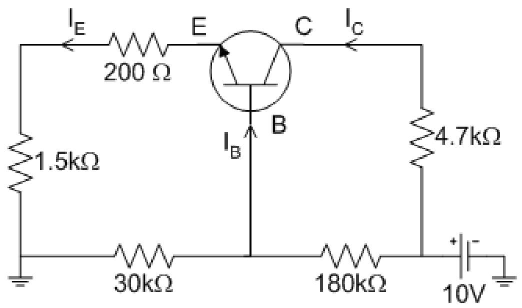


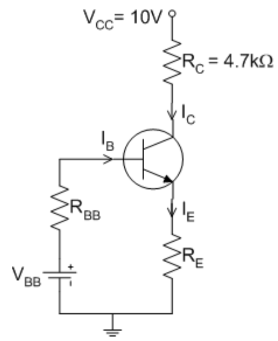
$h_{fe} = h_{FE} = 200$
$V_{BE} = 0.7\,V$
$\gamma = kT/q = 26\,mV$

Example 1: Consider the common-base BJT amplifier in the figure above.

a) Perform DC analysis and find the Q-point.
b) Evaluate the overall voltage gain A_{Vs} and the current gain A_i.
c) Sketch v_o on the AC+DC load line graph when
   i. $v_s = 100 \sin(\omega t)$ mV,
   ii. $v_s = 900 \sin(\omega t)$ mV.

Solution: a) Let us first draw the DC equivalent circuit first as shown below,





Here, $R_E = R_{E_1} + R_{E_2} = 0.2k + 1.5k = 1.7\,\text{k}\Omega$.

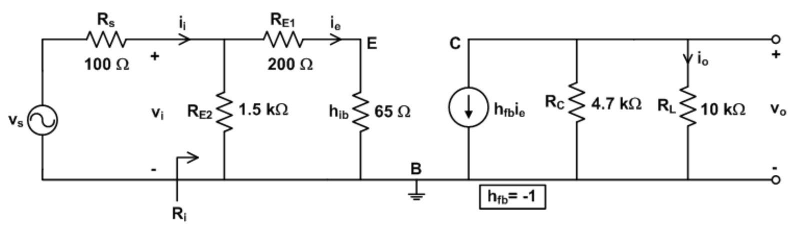
Now, let us calculate V_{BB}, R_{BB}, I_{CQ}, V_{CEQ} and V_{CBQ}

$$V_{BB} = \left(\frac{30k}{30k + 180k}\right)(10) = 1.43\,\text{V},$$
$$R_{BB} = 30k||180k = 25.71\,\text{k}\Omega,$$
$$I_{CQ} \cong I_{EQ} = \frac{1.43 - 0.7}{25.71k/201 + 1.7k} = 0.4\,\text{mA},$$
$$V_{CEQ} = 10 - (0.4m)(4.7k + 1.7k) = 7.44\,\text{V},$$
$$V_{CBQ} = 7.44 - 0.7 = 6.74\,\text{V}.$$

b) In order to calculate the voltage gain, we need to draw the common-base SSAC equivalent circuit. As it is not given $1/h_{ob} = \infty$. Let us now calculate h_{ib} as

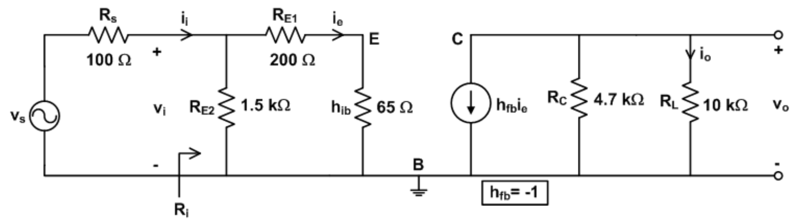
$$h_{ib} = \frac{26m}{0.4m} = 65\,\Omega.$$

So, the small-signal equivalent circuit is given below



Now, let us calculate input resistance R_i and voltage gain with load A_V as follows

$$R_i = R_{E_2}||\,(R_{E1} + h_{ib}) = 1.5k||(200 + 65) \cong 225\,\Omega$$
$$A_V = \frac{v_o}{v_i} = \left(\frac{v_o}{h_{fb}i_e}\right)\left(\frac{h_{fb}i_e}{i_e}\right)\left(\frac{i_e}{v_i}\right)$$
$$= (-R_C||R_L)\,(h_{fb})\left(\frac{1}{R_{E_1} + h_{ib}}\right) = \frac{R_C||R_L}{R_{E_1} + h_{ib}}$$
$$= \frac{4.7k||10k}{200 + 65} = \frac{3.2k}{0.265k} = 12.08.$$



Thus, overall voltage gain A_{Vs} and current gain A_i are given by

$$A_{Vs} = \frac{v_o}{v_s} = \left(\frac{v_o}{v_i}\right)\left(\frac{v_i}{v_s}\right) = A_V \frac{R_i}{R_s + R_i} = (12.08)\left(\frac{225}{100+225}\right)$$
$$= 8.36,$$
$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_L}{v_i/R_i} = A_V \frac{R_i}{R_L} = (12.08)\left(\frac{0.225k}{10k}\right)$$
$$= 0.27.$$

c) Let us write down the AC load line equation for this common-base amplifier, noting that $v_o = v_{cb} = -i_c(R_C||R_L) = -i_c R_{ac}$ and $v_{cb} = v_{ce} - v_{be} = v_{ce} - \frac{h_{ib}}{R_{E_1}+h_{ib}} v_i \approx v_{ce})$

$$v_{CB} = -i_C R_{ac} + V_{CBQ} + I_{CQ} R_{ac} \qquad \ldots V_{CBQ} = V_{CEQ} - V_{BEQ}$$
$$v_{CE} - V_{BEQ} = -i_C R_{ac} + V_{CEQ} - V_{BEQ} + I_{CQ} R_{ac} \qquad \ldots v_{CB} \approx v_{CE} - V_{BEQ}$$
$$v_{CE} = -i_C R_{ac} + V_{CEQ} + I_{CQ} R_{ac}$$

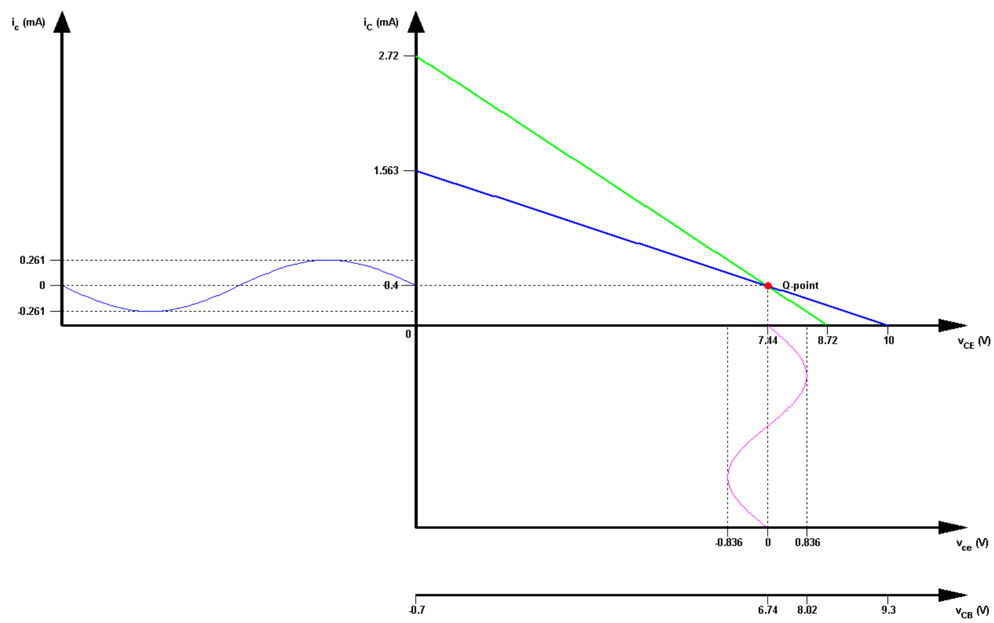
So, $R_{ac} = R_C||R_L = 4.7k||10k = 3.2\,\text{k}\Omega$, and similarly we obtain R_{DC} from the C-E loop as $R_{DC} = R_C + R_E = 4.7k + 1.7k = 6.4\,\text{k}\Omega$.

Note that, maximum available undistorted swing amplitude is

$$\min\left(V_{CEQ}, I_{CQ}R_{ac}\right) = \min(7.44, (0.4m)(3.2k)) = \min(7.44, 1.28) = 1.28\,\text{V}.$$

Thus, as $A_{Vs} = 8.36$, maximum input source amplitude which gives an undistorted output is $\max(v_{s(p)}) = 1.28/8.36 = 153.1\,\text{mV}$. If the input source amplitude exceeds this value, we will observe distortion at the output.

i. For $v_s = 100\sin(\omega t)$ mV, we are going to observe an undistorted sinusoidal output with an amplitude of $0.836\,\text{V}$ around $V_{CBQ} = 6.74\,\text{V}$ as shown below.



ii. For $v_s = 900\sin(\omega t)$ mV, we are going to observe a distorted output as shown below.