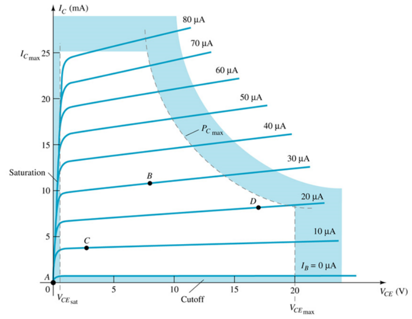
Contents

DC Biasing

Biasing refers to the DC voltages applied to the transistor to put it into **active mode**, so that it can amplify the AC signal.

The DC input establishes an **operating point** or quiescent point called the ***Q*-point**.

Proper DC biasing should try to set the Q-point towards the middle of active region, e.g., Point B in the figure below.



Three States of Operation

Proper DC biasing sets the BJT transistor into the **active state**, so that it can amplify the AC signal. Let us remember the states of the transistor:

- **Active:** Operating state of the amplifier: $I_C = \beta I_B$.
  - Base-Emitter (BE) junction: **forward-biased** (ON).
  - Base-Collector (BC) junction: **reverse-biased** (OFF).
- **Cut-Off:** The amplifier is basically off. There is **no current**, i.e., $I_C = I_B = I_E = 0\,$A.
  - Base-Emitter (BE) junction: **reverse-biased** (OFF).
  - Base-Collector (BC) junction: **reverse-biased** (OFF).
- **Saturation:** The amplifier is saturated. Voltages are fixed, e.g., $V_{CE} = V_{CE(sat)} \cong 0\,$V. **Output** is **distorted**, i.e., not the same shape as the input waveform.
  - Base-Emitter (BE) junction: **forward-biased** (ON).
  - Base-Collector (BC) junction: **forward-biased** (ON).

BJT DC Analysis

1. Draw the DC equivalent circuit (signal frequency is zero, i.e., $f = 0$)
   a) Capacitors are open circuit, i.e., $X_C \to \infty$.
   b) Kill the AC power sources (short-circuit AC voltage sources and open-circuit AC current sources).
   c) Inductors are short circuit or replaced by their DC resistance (winding resistance) if given, i.e., $X_L \to 0$.
2. Write KVL for the loop which contains BE junction
   a) Take $V_{BE} = V_{BE(ON)}$ to ensure the transistor is ON (or not in the cut-off state). Note: For a pnp transistor, $V_{EB} = V_{BE(ON)}$.
   b) Determine the base current I_{BQ} (or emitter current I_{EQ}).
3. Write KVL for the loop which contains CE terminals
   a) Assume the transistor is in the active state and take $I_{CQ} = \beta I_{BQ}$ (or $I_{CQ} = \alpha I_{EQ}$).
   b) Calculate V_{CEQ}.
   c) If $V_{CEQ} \leq V_{CE(sat)}$ then the transistor is in the saturation (SAT) state (i.e., $I_{CQ} \neq \beta I_{BQ}$), so take $V_{CEQ} = V_{CE(sat)}$ and recalculate I_{CQ}.

   NOTE: Normally, a BJT should not be in the saturation state if it is used as an amplifier.

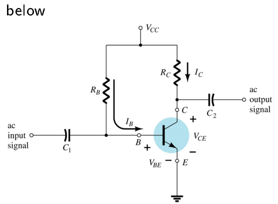
DC Biasing Circuits

Most common four common-emitter biasing circuits are given below

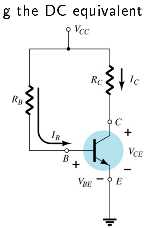
1. Fixed-Bias Circuit
2. Emitter-Stabilized Bias Circuit
3. Voltage Divider Bias Circuit
4. DC Bias with Voltage Feedback

Fixed-Bias Circuit

Fixed-bias circuit is given below

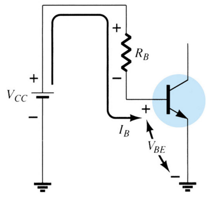


Let us start DC analysis by drawing the DC equivalent circuit as shown below



Base-Emitter Loop

Let us continue with the BE loop shown below



Writing KVL on the BE loop

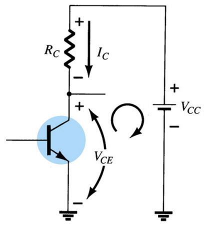
$$V_{CC} - I_B R_B - V_{BE} = 0$$

and given $V_{BE} = V_{BE(ON)}$, we obtain I_{BQ} as

$$\boxed{I_{BQ} = \frac{V_{CC} - V_{BE(ON)}}{R_B}}$$

Collector-Emitter Loop

Let us continue with the CE loop shown below



Writing KVL on the CE loop (i.e., DC load-line equation)

$$V_{CC} - I_C R_C - V_{CE} = 0$$

and given (assuming BJT is in active state)

$$\boxed{I_{CQ} = \beta I_{BQ}}$$

we obtain V_{CEQ} as

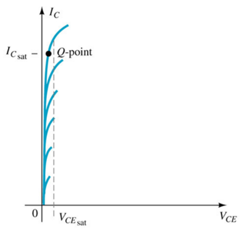
$$\boxed{V_{CEQ} = V_{CC} - I_{CQ} R_C}$$

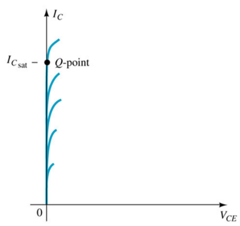
Saturation

The term **saturation** is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of water. For a transistor operating in the saturation region, the **current** is a **maximum** value for the particular design.

Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE(sat)}$. If we approximate the curves of the left figure by those appearing in the right figure, then the saturation voltage $V_{CE(sat)}$ is assumed to be $0\,\mathrm{V}$, i.e,

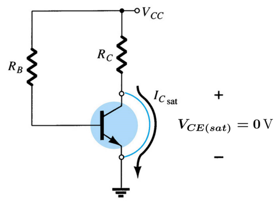
$$\boxed{V_{CE(sat)} \cong 0\,\mathrm{V}}$$

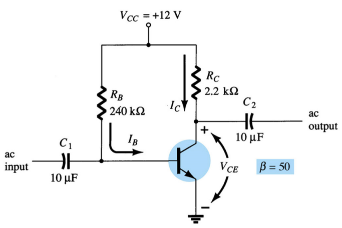




For the fixed-bias configuration shown below, the resulting saturation current (i.e., maximum current) $I_{C(sat)}$ is given by

$$I_{C(sat)} = I_{C(max)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \simeq \frac{V_{CC}}{R_C}$$





Example 1: For the figure above, calculate all DC currents and voltages.

Solution: Let us find I_{BQ}, I_{CQ} and V_{CEQ} as follows

$$I_{BQ} = \frac{V_{CC} - V_{BE(ON)}}{R_B} = \frac{12 - 0.7}{240k} = 47.08\,\mu\mathrm{A},$$

$$I_{CQ} = \beta I_{BQ} = (50)(47.08\mu) = 2.35\,\mathrm{mA},$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 12 - (2.35m)(2.2k) = 6.83\,\mathrm{V}.$$

As $V_{CEQ} > V_{CE(sat)} = 0\,\mathrm{V}$, transistor is in the active state. Let us also prove it by showing $V_{BCQ} < V_{BC(ON)} = 0.7\,\mathrm{V}$ as follows

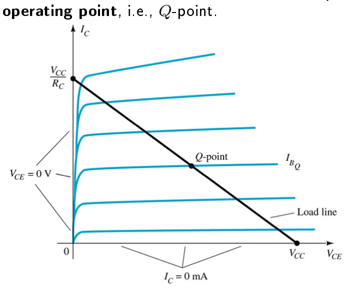
$$V_{BCQ} = V_{BQ} - V_{CQ} = V_{BEQ} - V_{CEQ} = 0.7 - 6.83 = -6.13\,\mathrm{V} < 0.7\,\mathrm{V}.$$

DC Load Line

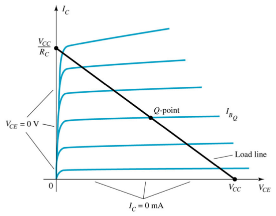
DC load line equation comes from KVL equation in the CE loop (i.e., output loop). For the fixed-bias circuit, DC load line equation is given by

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

Let us draw the load line over output characteristics curve as shown below. The **intersection** of the load-line with the output characteristics curve (determined by the base current I_{BQ}) is the **operating point**, i.e., Q-point.



- The Q-point is the operating point where the value of R_B sets the value of I_{BQ} that controls the values of V_{CEQ} and I_{CQ}.



Fixed-bias load line equation: $V_{CE} = V_{CC} - I_C R_C$

The load line end points are the SATURATION and CUTOFF points, i.e.,

- $I_{C(sat)}$ end point (on the current axis):

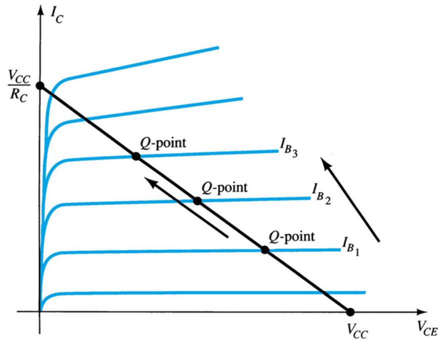
$$I_C = V_{CC}/R_C$$
$$V_{CE} = 0\,\text{V}$$

- $V_{CE(cutoff)}$ end point (on the voltage axis):

$$V_{CE} = V_{CC}$$
$$I_C = 0\,\text{mA}$$

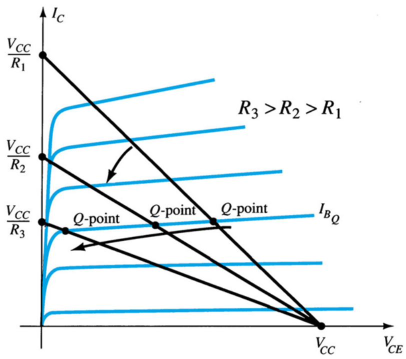
The Effect of I_B on the Q-Point

Movement of the Q-point with increasing level of I_B (or decreasing level of R_B) is shown below.



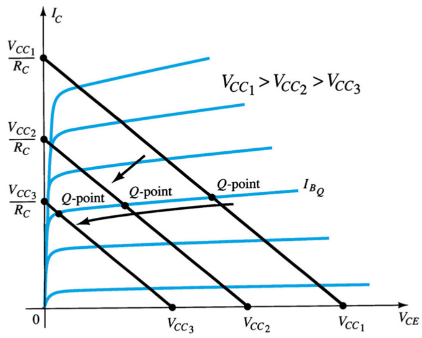
The Effect of R_C on the Q-Point

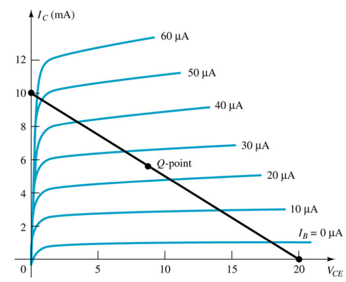
Effect of an increasing level of R_C on the load line (slope decreases with increasing R_C) and the Q-point is shown below.



The Effect of V_{CC} on the Q-Point

Effect of an decreasing level of V_{CC} on the load line (end points gets smaller with decreasing V_{CC}) and the Q-point is shown below.





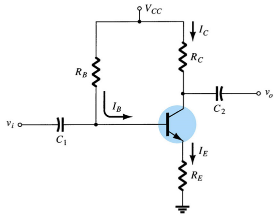
Example 2: For the fixed-bias load line above, calculate V_{CC}, R_C and R_B.

Solution: From the figure, $I_{BQ} = 25\,\mu$A. So, let us find V_{CC}, R_C and R_B as follows

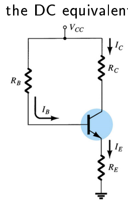
$$V_{CC} = V_{CE(cutoff)} = 20\,\text{V},$$
$$R_C = \frac{V_{CC}}{I_{C(sat)}} = \frac{20}{10m} = 2\,\text{k}\Omega,$$
$$R_B = \frac{V_{CC} - V_{BE(ON)}}{I_{BQ}} = \frac{20 - 0.7}{25\mu} = 772\,\text{k}\Omega.$$

Emitter-Stabilized Bias Circuit

Adding a resistor to the emitter circuit stabilizes the bias circuit, as shown below.

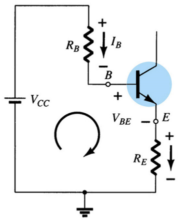


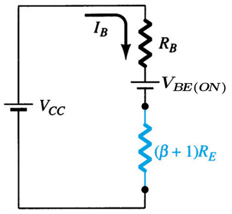
Let us start DC analysis by drawing the DC equivalent circuit as shown below



Base-Emitter Loop

Let us continue with the BE loop shown below





Writing KVL on the BE loop

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

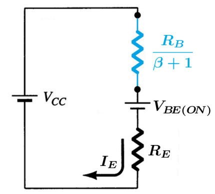
$$V_{CC} - I_B R_B - V_{BE(ON)} - (\beta+1) I_B R_E = 0, \quad \ldots \text{as } V_{BE} = V_{BE(ON)} \text{ and}$$

$$I_E = (\beta+1) I_B \text{ in active mode}$$

we obtain I_{BQ} as

$$\boxed{I_{BQ} = \frac{V_{CC} - V_{BE(ON)}}{R_B + (\beta+1)R_E}}$$

Similarly, we can obtain I_{EQ} directly from the figure below, or dividing the denominator of the I_{BQ} by $(\beta+1)$



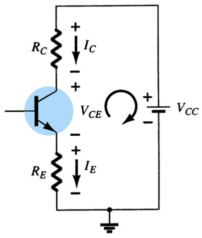
as follows

$$\boxed{I_{EQ} = \frac{V_{CC} - V_{BE(ON)}}{\frac{R_B}{\beta+1} + R_E}}$$

- It is generally better to calculate I_{EQ} directly to reduce the number of calculations, especially when there is an emitter resistor R_E is connected.

Collector-Emitter Loop

Let us continue with the CE loop shown below



Let us write down the KVL equation on the CE loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0 \quad \ldots \text{as } I_C = \alpha I_E \cong I_E \text{ in active mode}$$

$$V_{CC} - I_C (R_C + R_E) - V_{CE} = 0 \quad \ldots \text{DC load line equation}$$

As $I_{CQ} = \beta I_{BQ} \cong I_{EQ}$ in active mode, we obtain V_{CEQ} as

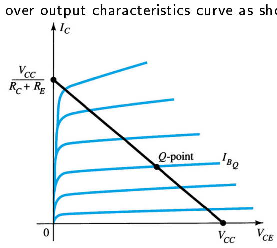
$$\boxed{V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)}$$

DC Load Line

DC load line equation comes from KVL equation in the CE loop (i.e., output loop). For the emitter-stabilized bias circuit, DC load line equation is given by

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$

Let us draw the load line over output characteristics curve as shown below.



Here, $V_{CE(cutoff)} = V_{CC}$ and $I_{C(sat)}$ is given by

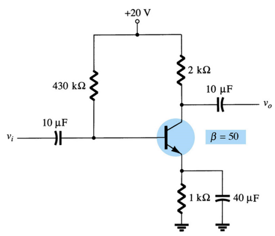
$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E}$$

- The Q-point is the operating point where the value of R_B and R_E sets the value of I_{BQ} that controls the values of V_{CEQ} and I_{CQ}.

Improved Biased Stability

Stability refers to a condition in which the currents and voltages remain fairly constant over a wide range of temperatures and transistor beta (β) values.

- Adding R_E resistor to the emitter improves the stability of a transistor.



Example 3: For the figure above, calculate all DC currents and voltages.

Solution: Let us find I_{BQ}, I_{CQ} and V_{CEQ} as follows

$$I_{BQ} = \frac{V_{CC} - V_{BE(ON)}}{R_B + (\beta+1)R_E} = \frac{20 - 0.7}{430k + (50+1)(1k)} = 40.13\,\mu\text{A},$$

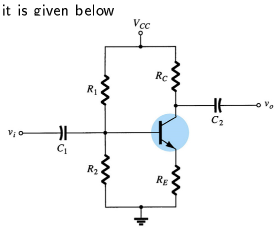
$$I_{CQ} = \beta I_{BQ} = (50)(40.13\mu) = 2.01\,\text{mA},$$

$$V_{CEQ} \cong V_{CC} - I_{CQ}(R_C + R_E) = 20 - (2.01m)(2k + 1k) = 13.97\,\text{V}.$$

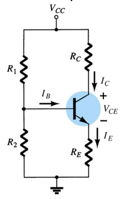
As $V_{CEQ} > 0\,\text{V}$ ($V_{CE(sat)}$), transistor is in the active state.

Voltage Divider Bias Circuit

Voltage divider bias circuit is given below

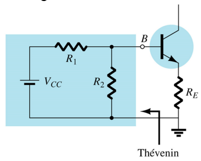


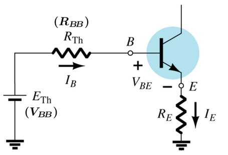
Let us start DC analysis by drawing the DC equivalent circuit as shown below



Base-Emitter Loop (Exact Analysis)

Let us transform the BE loop circuit shown on the left below to the Thévenin simplified circuit on the right below

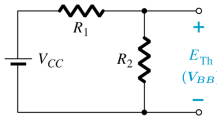


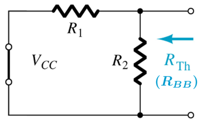


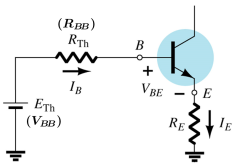
where the Thévenin voltage V_{BB} and Thévenin resistance R_{BB} are calculated as follows

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \quad \text{...from the figure on the left below}$$

$$R_{BB} = R_1 || R_2 \quad \text{...from the figure on the right below}$$







Writing KVL on the Thévenin equivalent BE loop shown above

$$V_{BB} - I_B R_{BB} - V_{BE} - I_E R_E = 0$$

$$V_{BB} - I_B R_{BB} - V_{BE(ON)} - (\beta+1) I_B R_E = 0, \quad \text{...as } V_{BE} = V_{BE(ON)} \text{ and } I_E = (\beta+1) I_B \text{ in active mode}$$

we obtain I_{BQ} as

$$\boxed{I_{BQ} = \frac{V_{BB} - V_{BE(ON)}}{R_{BB} + (\beta+1) R_E}}$$

Similarly, we obtain I_{EQ} as

$$\boxed{I_{EQ} = \frac{V_{BB} - V_{BE(ON)}}{\frac{R_{BB}}{\beta+1} + R_E}}$$

Base-Emitter Loop (Approximate Analysis)

$$I_{EQ} = \frac{V_{BB} - V_{BE(ON)}}{R_{BB}/(\beta+1) + R_E}$$

If we look at the I_{EQ} equation above, we see that if $R_E \gg \frac{R_{BB}}{\beta+1}$, equation simplifies to

$$\boxed{I_{EQ} = \frac{V_{BB} - V_{BE(ON)}}{R_E}}$$

where $V_{BB} = \frac{R_2}{R_1+R_2} V_{CC}$.

- Approximate approach can be used when $(\beta+1) R_E \gg R_{BB}$. Approximate analysis condition can be rewritten as

$$\boxed{(\beta+1) R_E \geq 10 (R_1 || R_2).}$$

Assuming $R_1 > R_2$, we know that $(R_1 || R_2) \leq R_2$. So, the condition above can be further simplified to

$$\boxed{\beta R_E \geq 10 R_2.}$$

- Satisfying this condition means that we can safely ignore the base current I_B in the DC equivalent circuit and apply the voltage divider rule between R_2 and R_1.

Collector-Emitter Loop and DC Load Line

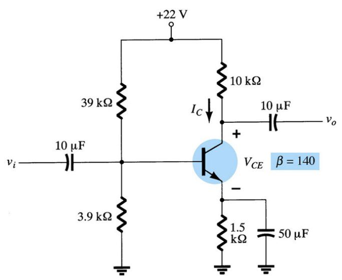
- Analysis on the CE loop (i.e., output loop), is the same as the CE loop analysis of the emitter-stabilized circuit. So, V_{CEQ} is given by

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$$

where $I_{CQ} \cong I_{EQ}$.

- Similarly, DC load line analysis is also the same as the DC load line of the emitter-stabilized circuit. So, DC load line equation is given by

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

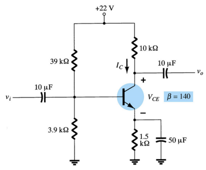


Example 4: For the figure above, calculate all DC currents and voltages using both exact and approximate analysis.

Solution: Let us first find the Thévenin voltage V_{BB} and resistance R_{BB} as follows

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{3.9k}{39k + 3.9k} 22 = 2\,\text{V},$$

$$R_{BB} = R_1 || R_2 = 3.9k || 39k = 3.55\,\text{k}\Omega.$$



Now, let us calculate I_{BQ}, I_{CQ} and V_{CEQ} as follows

$$I_{EQ} = \frac{V_{BB} - V_{BE(ON)}}{R_{BB}/(\beta+1) + R_E} = \frac{2 - 0.7}{3.55k/(140+1) + 1.5k} = 0.85\,\text{mA},$$
$$I_{CQ} \cong I_{EQ} = 0.85\,\text{mA},$$
$$V_{CEQ} \cong V_{CC} - I_{CQ}(R_C + R_E) = 22 - (0.85m)(10k + 1.5k) = 12.23\,\text{V}.$$

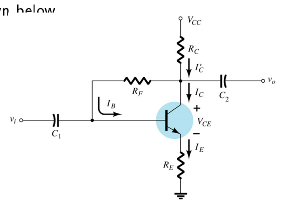
As $\beta R_E \geq 10R_2$ (i.e., $210\,\text{k}\Omega \geq 39\,\text{k}\Omega$), we can use the approximate analysis and ignore I_B and R_{BB} as follows

$$I_{EQ} = \frac{V_{BB} - V_{BE(ON)}}{R_E} = \frac{2 - 0.7}{1.5k} = 0.87\,\text{mA},$$
$$I_{CQ} \cong I_{EQ} = 0.87\,\text{mA},$$
$$V_{CEQ} \cong V_{CC} - I_{CQ}(R_C + R_E) = 22 - (0.87m)(10k + 1.5k) = 12\,\text{V}.$$

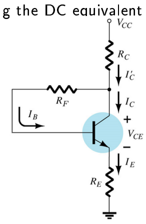
We see that approximate analysis provides close values to the exact analysis. The differences in I_{CQ} and V_{CEQ} are only 0.02 mA and 0.23 V, respectively.

DC Bias with Voltage Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base as shown below

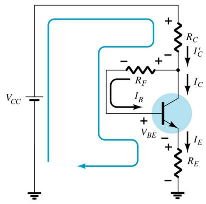


Let us start DC analysis by drawing the DC equivalent circuit as shown below



Base-Emitter Loop

Let us continue with the BE loop shown below



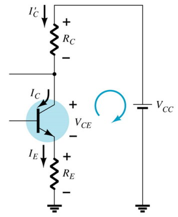
We can write KVL equation on the BE loop noting that $I'_C = I_C + I_B = I_E$

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$
$$V_{CC} - I_E R_C - \frac{I_E}{\beta+1} R_F - V_{BE(ON)} - I_E R_E = 0, \quad \ldots\text{as } V_{BE} = V_{BE(ON)} \text{ and}$$

and we obtain I_{EQ} as
$$\boxed{I_{EQ} = \frac{V_{CC} - V_{BE(ON)}}{\frac{R_F}{\beta+1} + (R_C + R_E)}} \qquad I_B = \frac{I_E}{\beta+1} \text{ in active mode}$$

Collector-Emitter Loop

Let us continue with the CE loop shown below



Let us write down the KVL equation on the CE loop noting that $I'_C = I_C + I_B$

$$V_{CC} - I'_C R_C - V_{CE} - I_E R_E = 0$$
$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0 \quad \ldots\text{as } I_C \cong I_E \text{ and } I_C \cong I'_C \text{in active mode}$$
$$V_{CC} - I_C(R_C + R_E) - V_{CE} = 0 \quad \ldots\text{DC load line equation}$$

As $I_{CQ} \cong I_{EQ}$ in active mode, we obtain V_{CEQ} as

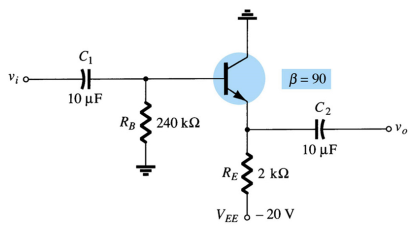
$$\boxed{V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)}$$

DC Load Line

- Note that $I'_C = I_E$, and
$$I_C \cong I_E$$
in active mode (and β is high).

- So, DC load line analysis is the same as the DC load line of the emitter-stabilized circuit. So, DC load line equation is given by
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Various Different Bias Circuits



Example 5: For the figure above, calculate all DC currents and voltages.

Solution: Let us find I_{EQ}, I_{CQ} and V_{CEQ} as follows

$$I_{EQ} = \frac{0 - V_{BE(ON)} - V_{EE}}{R_B/(\beta+1) + R_E} = \frac{20 - 0.7}{240k/(90+1) + 2k} = 4.16\,\text{mA},$$
$$I_{CQ} \cong I_{EQ} = 4.16\,\text{mA},$$
$$V_{CEQ} = 0 - I_{EQ}R_E - V_{EE} = 20 - (4.16m)(2k) = 11.68\,\text{V}.$$

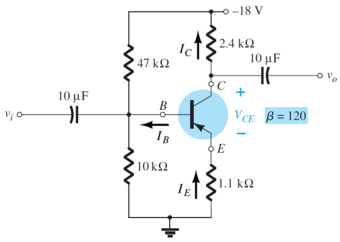
As $V_{CEQ} > V_{CE(sat)} = 0\,\text{V}$, transistor is in the active state.

pnp Transistors

The analysis for pnp bias transistor circuits is the same as that for npn transistor circuits.

The only differences are that

1. Currents are flowing in the opposite direction.
2. Voltages have opposite polarity, e.g., $V_{EB} = V_{BE(ON)} = 0.7\,\text{V}$ in the active mode.



Example 6: For the figure above, calculate all DC currents and voltages.

Solution: As $\beta R_E \geq 10R_2$, i.e., $132\,\text{k}\Omega \geq 100\,\text{k}\Omega$, we can ignore the base current I_B and use the approximate approach. Thus, we can find V_{BB}, I_{EQ}, I_{CQ} and V_{CEQ} as follows

$$V_B \cong \frac{R_2}{R_1+R_2}V_{CC} = \frac{10k}{47k+10k}(-18) = -3.16\,\text{V}$$

$$I_{EQ} \cong \frac{0-V_{EB}-V_B}{R_E} = \frac{0-0.7-(-3.16)}{1.1k} = \frac{2.46}{1.1k} = 2.24\,\text{mA},$$

$$I_{CQ} \cong I_{EQ} = 2.24\,\text{mA},$$

$$V_{ECQ} = 0 - I_{CQ}(R_C+R_E) - V_{CC} = -(2.24m)(2.4k+1.1k) - (-18) = 10.16\,\text{V}.$$

As $V_{ECQ} > V_{CE(sat)} = 0\,\text{V}$, transistor is in the active state.

Bias Stabilization

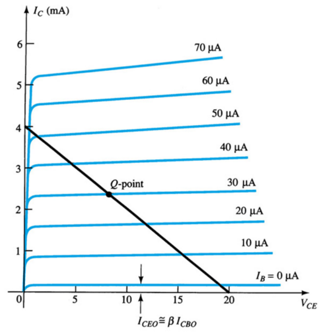
Variation of three BJT (Si) parameters (I_{CO}, β and $V_{BE(ON)}$) with temperature are summarized below

$T\uparrow$	$I_{CO}\uparrow$	$\beta\uparrow$	$V_{BE(ON)}\downarrow$

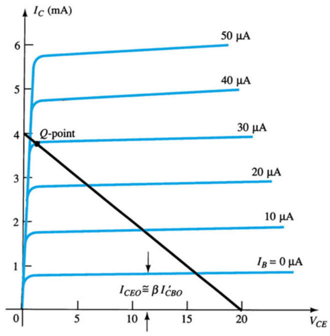
- I_{CO} (reverse saturation current)
  - doubles in value for every $10\,^\circ\text{C}$
- β (transistor current gain)
  - increases with increasing temperature
- $V_{BE(ON)}$ (forward bias potential of the base-emitter junction)
  - decreases about $2.5\,\text{mV}$ per $1\,^\circ\text{C}$ increase in temperature

Variation of the transistor parameters with temperature causes a shift in the operating point (i.e., Q-point).

Figures below (at $25\,^\circ\text{C}$ on the left and at $100\,^\circ\text{C}$ on the right) show the shift of the Q-point (or DC bias point) due to temperature change for a fixed-bias circuit.



at $25\,^\circ\text{C}$



at $100\,^\circ\text{C}$

Stability Factors

Stability of the collector current I_C depends on the stability of several parameters like I_{CO}, β, $V_{BE(ON)}$, V_{CC}, R_B, R_C, etc.

A stability factor S is defined for **each** of the parameters affecting bias stability as follows:

$$S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}} = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{\beta, V_{BE(ON)},\ldots\ \text{constant}}$$

$$S_\beta = \frac{\partial I_C}{\partial \beta} = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO}, V_{BE(ON)},\ldots\ \text{constant}}$$

$$S_{V_{BE(ON)}} = \frac{\partial I_C}{\partial V_{BE(ON)}} = \left.\frac{\Delta I_C}{\Delta V_{BE(ON)}}\right|_{I_{CO},\beta,\ldots\ \text{constant}}$$

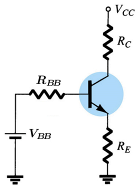
We know that differential dI_C is given by the linear map of parameter differentials as follows

$$dI_C = \frac{\partial I_C}{\partial I_{CO}}dI_{CO} + \frac{\partial I_C}{\partial \beta}d\beta + \frac{\partial I_C}{\partial V_{BE(ON)}}dV_{BE(ON)} + \cdots$$

- Thus, we obtain the collector-current change ΔI_C using the stability factors as follows

$$\boxed{\Delta I_C \cong S_{I_{CO}}\Delta I_{CO} + S_\beta \Delta\beta + S_{V_{BE(ON)}}\Delta V_{BE(ON)}}$$

Derivation of Stability Factors (Voltage-Divider Bias Circuit)



Let us write down the active mode collector current and BE-loop KVL equations for the circuit shown above,

$$I_C = \beta I_B + (\beta+1)I_{CO}$$

$$V_{BB} = I_B R_{BB} + V_{BE(ON)} + (I_B + I_C)R_E$$

Combining the two equations above, we obtain the expression for I_C as

$$\boxed{I_C = \frac{\beta}{R_{BB}+(\beta+1)R_E}\left(V_{BB}-V_{BE(ON)}\right) + \frac{(\beta+1)(R_{BB}+R_E)}{R_{BB}+(\beta+1)R_E}I_{CO}}$$

$$I_C = \frac{\beta}{R_{BB} + (\beta+1)\,R_E}\left(V_{BB} - V_{BE(ON)}\right) + \frac{(\beta+1)\,(R_{BB}+R_E)}{R_{BB} + (\beta+1)\,R_E} I_{CO}$$

1. From the I_C equation above, let us derive $S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}}$ as

$$S_{I_{CO}} = (\beta+1)\,\frac{R_{BB}+R_E}{R_{BB} + (\beta+1)\,R_E}$$

2. From the I_C equation above, let us derive $S_{V_{BE(ON)}} = \frac{\partial I_C}{\partial V_{BE(ON)}}$ as

$$S_{V_{BE(ON)}} = \frac{-\beta}{R_{BB} + (\beta+1)\,R_E}$$

3. In order to derive $S_\beta = \frac{\partial I_C}{\partial \beta}$, let us first simplify I_C equation by letting $I_{CO} \cong 0$

$$I_C \cong \frac{\beta}{R_{BB} + (\beta+1)\,R_E}\left(V_{BB} - V_{BE(ON)}\right)$$

Using the simplified I_C equation we can express I_{C_1} and I_{C_2} as follows

$$I_{C_1} \cong \frac{\beta_1}{R_{BB} + (\beta_1+1)\,R_E}\left(V_{BB} - V_{BE(ON)}\right)$$
$$I_{C_2} \cong \frac{\beta_2}{R_{BB} + (\beta_2+1)\,R_E}\left(V_{BB} - V_{BE(ON)}\right)$$

Thus, using the equations above, let us obrain the ratio $\frac{I_{C_2}-I_{C_1}}{I_{C_1}}$ as

$$\frac{I_{C_2}-I_{C_1}}{I_{C_1}} = \frac{\beta_2-\beta_1}{\beta_1}\,\frac{R_{BB}+R_E}{R_{BB} + (\beta_2+1)\,R_E}$$

From the equation above, we can obtain the ratio $\frac{\Delta I_C}{\Delta\beta}$ by using $\Delta I_C = I_{C_2} - I_{C_1}$ and $\Delta\beta = \beta_2 - \beta_1$ as

$$\frac{\Delta I_C}{\Delta\beta} = \frac{I_{C_1}}{\beta_1}\,\frac{R_{BB}+R_E}{R_{BB} + (\beta_2+1)\,R_E}$$

Thus, as $S_\beta = \frac{\partial I_C}{\partial\beta} \cong \frac{\Delta I_C}{\Delta\beta}$

$$S_\beta = \frac{I_{C_1}}{\beta_1}\,\frac{R_{BB}+R_E}{R_{BB} + (\beta_2+1)\,R_E}$$

Stability Factors for Other Bias Circuits

A. For the **fixed-bias** circuit, i.e., by substituting $R_E = 0$ and $R_{BB} = R_B$, the stability factors are given by

$$S_{I_{CO}} = \beta + 1$$
$$S_{V_{BE(ON)}} = \frac{-\beta}{R_B}$$
$$S_\beta = \frac{I_{C_1}}{\beta_1}$$

B. For the **emitter-stabilized bias** circuit, i.e., $R_{BB} = R_B$ and $R_B \gg R_E$, the stability factors are given by

$$S_{I_{CO}} = (\beta+1)\,\frac{R_B+R_E}{R_B + (\beta+1)\,R_E} \cong \frac{\beta+1}{1+\frac{(\beta+1)\,R_E}{R_B}}$$
$$S_{V_{BE(ON)}} = \frac{-\beta}{R_B + (\beta+1)\,R_E}$$
$$S_\beta = \frac{I_{C_1}}{\beta_1}\,\frac{R_B+R_E}{R_B + (\beta_2+1)\,R_E} \cong \frac{I_{C_1}}{\beta_1}\,\frac{1}{1+\frac{(\beta_2+1)\,R_E}{R_B}}$$

C. For the **voltage-divider bias** circuit with $(\beta+1)R_E \geq 10R_{BB}$, the stability factors are given by

$$S_{I_{CO}} = (\beta+1)\,\frac{R_{BB}+R_E}{R_{BB} + (\beta+1)\,R_E} \cong 1 + \frac{R_{BB}}{R_E}$$
$$S_{V_{BE(ON)}} = \frac{-\beta}{R_{BB} + (\beta+1)\,R_E} \cong \frac{-1}{R_E}$$
$$S_\beta = \frac{I_{C_1}}{\beta_1}\,\frac{R_{BB}+R_E}{R_{BB} + (\beta_2+1)\,R_E} \cong \frac{I_{C_1}}{\beta_1\beta_2}\left(1+\frac{R_{BB}}{R_E}\right)$$

D. For the **voltage-feedback bias** circuit, i.e., $R_{BB} = R_F$, replacing R_E with $R_{CE} = R_C + R_E$ and $R_F \gg R_{CE}$, the stability factors are given by

$$S_{I_{CO}} = (\beta+1)\,\frac{R_F+R_{CE}}{R_F + (\beta+1)\,R_{CE}} \cong \frac{\beta+1}{1+\frac{(\beta+1)\,R_{CE}}{R_F}}$$
$$S_{V_{BE(ON)}} = \frac{-\beta}{R_F + (\beta+1)\,R_{CE}}$$
$$S_\beta = \frac{I_{C_1}}{\beta_1}\,\frac{R_F+R_{CE}}{R_F + (\beta_2+1)\,R_{CE}} \cong \frac{I_{C_1}}{\beta_1}\,\frac{1}{1+\frac{(\beta_2+1)\,R_{CE}}{R_F}}$$

Temperature	I_{CO}	β	$V_{BE(ON)}$
$-65\,°$C	0.02 nA	20	0.85 V
$25\,°$C	0.1 nA	50	0.65 V
$100\,°$C	20 nA	80	0.48 V
$175\,°$C	3.3 μA	120	0.30 V

Example 7: Find and compare the collector current change ΔI_C when the temperature rises from $25\,°$C to $100\,°$C for the transistor defined by the table above for the following bias arrangements.

a. Fixed-bias with $R_B = 240\,\text{k}\Omega$ and $I_{C_1} = 2\,\text{mA}$,
b. Voltage-divider bias with $R_E = 4.7\,\text{k}\Omega$, $R_{BB}/R_E = 2$ and $I_{C_1} = 2\,\text{mA}$.

Solution: From the table above, let us first calculate ΔI_{CO}, $\Delta\beta$ and $\Delta V_{BE(ON)}$

$$\Delta I_{CO} = I_{CO_2} - I_{CO_1} = 20n - 0.1n = 19.9\,\text{nA}$$
$$\Delta\beta = \beta_2 - \beta_1 = 80 - 50 = 30$$
$$\Delta V_{BE(ON)} = V_{BE(ON)_2} - V_{BE(ON)_1} = 0.48 - 0.65 = -0.17\,\text{V}$$

We are goiung to calculate ΔI_C using

$$\Delta I_C \cong S_{I_{CO}}\Delta I_{CO} + S_\beta\Delta\beta + S_{V_{BE(ON)}}\Delta V_{BE(ON)}$$

a. Let us calculate the stability factors for the fixed-bias circuit

$$S_{I_{CO}} = \beta + 1 = 51$$
$$S_\beta = \frac{I_{C_1}}{\beta_1} = \frac{2m}{50} = 0.04\,\text{mA}$$
$$S_{V_{BE(ON)}} = \frac{-\beta}{R_B} = \frac{-50}{240k} = -0.21\,\text{m}\Omega^{-1}$$

Thus, ΔI_C is given by

$$\Delta I_C \cong (51)(19.9n) + (0.04m)(30) + (-0.21m)(-0.17)$$
$$= 1.02\mu + 1.2m + 0.036m$$
$$= 1.236\,\text{mA}$$

That means, for the fixed-bias circuit I_C increases to $3.236\,\text{mA}$ at $100\,°$C from $2\,\text{mA}$.

b. Let us calculate the stability factors for the voltage-divider bias circuit

$$S_{I_{CO}} \cong 1 + \frac{R_{BB}}{R_E} = 1 + 2 = 3$$
$$S_\beta \cong \frac{I_{C_1}}{\beta_1\beta_2}\left(1+\frac{R_{BB}}{R_E}\right) = \frac{2m}{(50)(80)}(1+2) = 1.5\,\mu\text{A}$$
$$S_{V_{BE(ON)}} = \frac{-1}{R_E} = \frac{-1}{4.7k} = -0.21\,\text{m}\Omega^{-1}$$

Thus, ΔI_C is given by

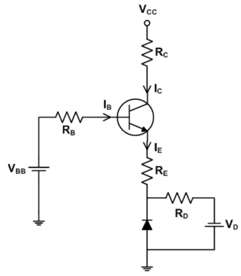
$$\begin{aligned}\Delta I_C &\cong (3)(19.9n) + (1.5\mu)(30) + (-0.21m)(-0.17)\\ &= 0.060\mu + 0.045m + 0.036m\\ &= 0.081\,\text{mA}\end{aligned}$$

That means, for the voltage-divider bias circuit I_C increases to $2.08\,$mA at $100\,°$C from $2\,$mA. Most of the improvement comes from the reduction in S_β.

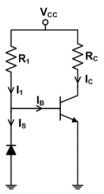
- These two results show that voltage-divider bias circuit is much more stable than the fixed-bias circuit. In other words, adding R_E resistor to the emitter leg of the transistor stabilizes the bias circuit.

Stability of Transistor Circuits with Active Components

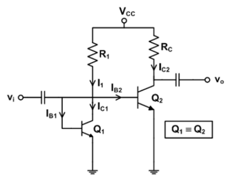
- V_{BE} compensation
  - by using a reverse-biased diode at the emitter



- I_{CO} compensation
  - by replacing R_2 with a reverse-biased diode



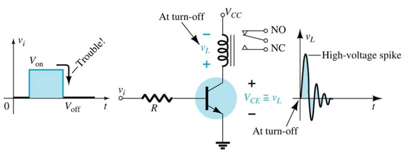
- I_C compensation (without R_E)
  - by using a current mirror



Practical Applications

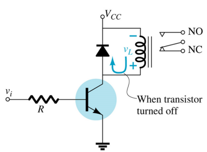
- Relay Driver
- Transistor Switch
- Transistor Switching Networks
- Logic Gates
- Current Mirror
- Voltage Level Indicator

Relay Driver



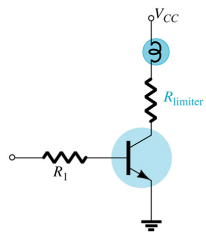
When the transistor turns OFF, a high voltage (given by $v_L = L\,(di_L/dt)$) is induced across the coil as shown above. If its magnitude exceeds the maximum ratings of the transistor, then the semiconductor device will be permanently damaged.

This destructive action can be subdued by placing a diode across the coil as shown below. Now, when the transistor turns off, the voltage across the coil will reverse and will forward-bias the diode, placing the diode in its ON state (hence protecting the transistor).

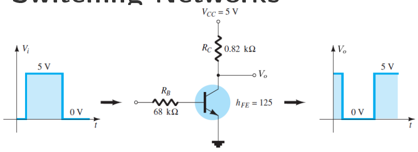


Transistor Switch

A transistor can be used as a switch to control the ON and OFF states of the light-bulb in the collector branch of the circuit as shown below.

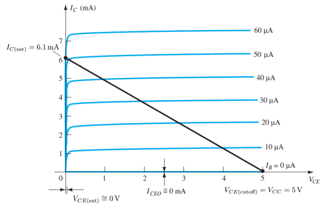


Transistor Switching Networks



Transistors can also be used as switches for computer and control applications. The circuit shown above can be employed an inverter in computer logic circuitry.

Inversion process requires that the Q-point switch from **cutoff** ($V_o = V_{CE(cutoff)} = 5\,\text{V}$) to **saturation** ($V_o = V_{CE(sat)} = 0\,\text{V}$) along the load line depicted below.

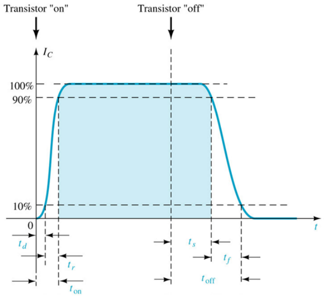


The total time required for the transistor to switch from the OFF to the ON state is designated as t_{on}, and he total time required for a transistor to switch from the ON to the OFF state is referred to as t_{off} as shown below. t_{on} and t_{off} are defined by

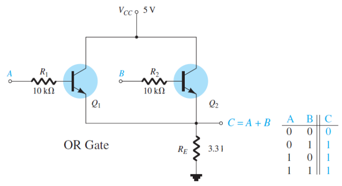
$$t_{on} = t_r + t_d$$

$$t_{off} = t_s + t_f$$

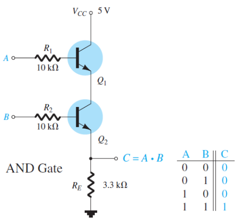
where t_r is the rise time from 10% to 90% of the output, t_d is the delay time between the changing state of the input and the beginning of a response at the output, t_s is the storage time and and t_f the fall time from 90% to 10% of the output.



Logic Gates

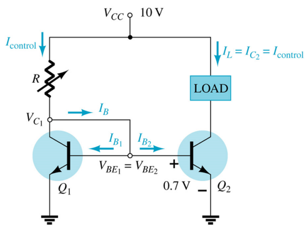


The figure above shows a BJT logic OR gate, and similarly The figure below shows a BJT logic AND gate.



Current Mirror

The **current mirror** shown below is a DC circuit in which the current through a **load** is controlled by a current at another point in the circuit. That is, the current through the load is independent of the load.



Homework 1: For the figure above, show that the load current is equal to the load control current and given by

$$I_L \cong I_{control} = \frac{V_{CC} - V_{BE(ON)}}{R}$$

where the transistors are identical ($Q_1 \equiv Q_2$), i.e., $V_{BE_1(ON)} = V_{BE_2(ON)} = V_{BE(ON)}$ and $\beta_1 = \beta_2 = \beta$, and current gain β is high, e.g., $\beta \geq 100$.

Voltage Level Indicator

The voltage level indicator circuit uses a green LED to indicate when the source voltage is close to its monitoring level of $9\,\text{V}$. The potentiometer is set to establish $5.4\,\text{V}$ at the point indicated below. The result is sufficient voltage to turn on both the $4.7\,\text{V}$ Zener and the transistor and establish a collector current through the LED sufficient in magnitude to turn on the green LED. The LED will immediately turn off, revealing that the supply voltage has dropped below $9\,\text{V}$ or that the power source has been disconnected (i.e., when the voltage set up by the voltage divider circuit drops below $5.4\,\text{V}$).