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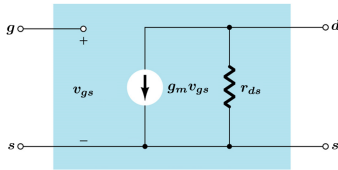
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FET SSAC Analysis Steps

1. Draw the SSAC equivalent circuit
 - a) Draw the AC equivalent circuit (signal frequency is infinity, i.e., $f = \infty$)
 - i. Capacitors are short circuit, i.e., $X_C \rightarrow 0$.
 - ii. Kill the DC power sources (i.e., AC value of DC sources is zero).
 - b) Replace FET with its small-signal equivalent model.
2. Calculate the three amplifier parameters: R_i , R_o and A_v
 - a) Calculate no-load input resistance, $R_i = \left. \frac{v_i}{i_i} \right|_{R_L = \infty}$.
 - b) Calculate output resistance, R_o .
 - c) Calculate no-load voltage gain, $A_v = \left. \frac{v_o}{v_i} \right|_{R_L = \infty}$.

FET Small-Signal Model

Small-signal equivalent model for a FET transistor is provided below. This model and its analysis is the same for all FET types, i.e., JFET, DMOSFET, EMOSFET, n -channel and p -channel.

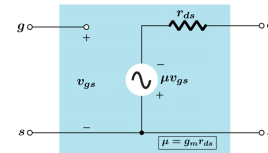


Here,

- $g_m = g_{fs} = y_{fs} = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{Q\text{-point}}$ is the forward transfer conductance,
- $r_{ds} = \frac{1}{g_{os}} = \frac{1}{y_{os}} = \left. \frac{\partial V_{DS}}{\partial I_D} \right|_{Q\text{-point}}$ is the output resistance.

Forward transfer conductance g_m is mostly called as the **transconductance** parameter.

When $r_{ds} \neq \infty$, we can also use the voltage-controlled voltage source model (via Norton-to-Thévenin transformation, a.k.a source transformation) as shown below. We mostly use this model for the common-gate and unbypassed self-bias configurations.



Here $\mu = g_m r_{ds}$ is the forward transfer-voltage gain.

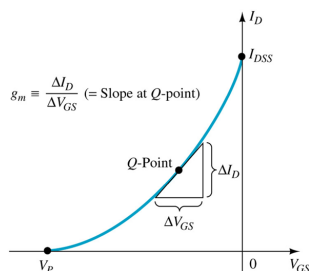
- Typical values of g_m run from 1 mS to 5 mS,
- Typical values of r_{ds} run from 20 kΩ to 100 kΩ,
- Consequently, typical values of μ run from 20 to 500.

Transconductance Parameter (g_m)

Transconductance parameter g_m is given by

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{Q\text{-point}} \cong \left. \frac{\Delta I_D}{\Delta V_{GS}} \right|_{Q\text{-point}}$$

In other words, g_m is the slope of the characteristics at the point of operation as shown below.



- Let us derive g_m for the JFET equation, $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$

$$\begin{aligned} g_m &= \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{Q\text{-point}} = \left. \frac{2I_{DSS}}{|V_P|} \left(1 - \frac{V_{GS}}{V_P}\right) \right|_{Q\text{-point}} \\ &= \frac{2I_{DSS}}{|V_P|} \left(1 - \frac{V_{GSQ}}{V_P}\right) \\ &= \frac{2I_{DSS}}{|V_P|} \sqrt{\frac{I_{DQ}}{I_{DSS}}} \quad \dots I_{DQ} = I_{DSS} \left(1 - \frac{V_{GSQ}}{V_P}\right)^2 \\ &= g_{m0} \sqrt{\frac{I_{DQ}}{I_{DSS}}} \quad \dots g_{m0} = \frac{2I_{DSS}}{|V_P|} \end{aligned}$$

- Let us derive g_m for the MOSFET equation, $I_D = k(V_{GS} - V_{GS(Th)})^2$

$$\begin{aligned} g_m &= \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{Q\text{-point}} = 2k(V_{GS} - V_{GS(Th)}) \Big|_{Q\text{-point}} \\ &= 2k(V_{GSQ} - V_{GS(Th)}) \\ &= 2\sqrt{k} \sqrt{I_{DQ}} \quad \dots I_{DQ} = k(V_{GS} - V_{GS(Th)})^2 \end{aligned}$$

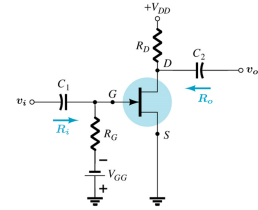
Phase Relationship

The phase relationship between input and output depends on the amplifier configuration circuit as listed below.

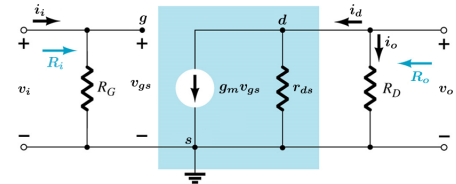
- Common-Source: 180 degrees
- Common-Gate: 0 degrees
- Common-Drain: 0 degrees (Source-Follower)

Common-Source Fixed-Bias Configuration

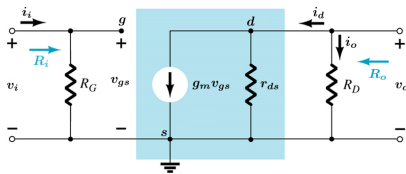
Common-source fixed-bias configuration is given below



Corresponding SSAC equivalent circuit is shown below



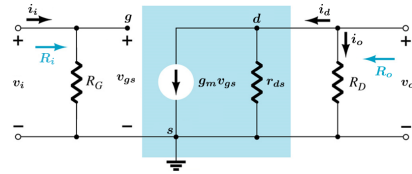
Input Resistance



Input resistance R_i is given as

$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L = \infty} = R_G$$

Voltage Gain

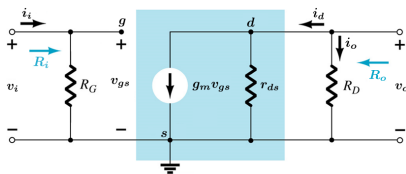


No-load voltage gain A_v is given by

$$A_v = \left. \frac{v_o}{v_i} \right|_{R_L = \infty} = \left(\frac{v_o}{g_m v_{gs}} \right) \left(\frac{g_m v_{gs}}{v_{gs}} \right) \left(v_{gs} \right) = (-R_D || r_{ds}) (g_m) (1) = -g_m (R_D || r_{ds})$$

- If $r_{ds} \geq 10R_D$, voltage gain A_v reduces to

$$A_v = -g_m R_D$$



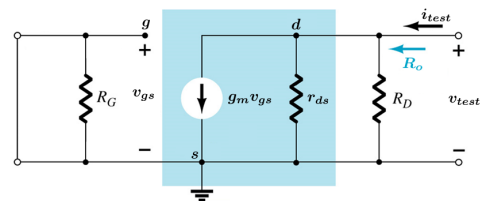
- For the circuit above, we can obtain the current gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i} = \frac{R_i}{R_D} A_v$$

- If $r_{ds} \geq 10R_D$, current gain A_i reduces to

$$A_i = -g_m R_G$$

Output Resistance



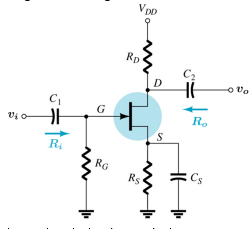
Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$R_o = \left. \frac{v_{test}}{i_{test}} \right|_{v_{gs} = 0, R_L = v_{test}} = R_D || r_{ds}$$

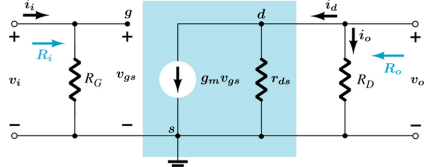
- If $r_{ds} \geq 10R_D$, then R_o simplifies to $R_o = R_D$.

CS Self-Bias Configuration

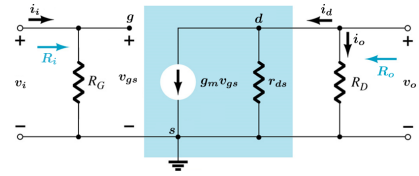
Common-source self-bias configuration is given below



Corresponding SSAC equivalent circuit is shown below



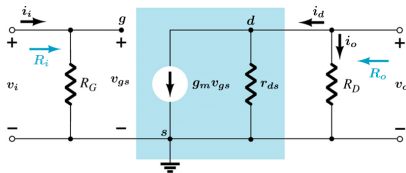
Input Resistance



Input resistance R_i is given as

$$R_i = \frac{v_i}{i_i} \Big|_{R_L = \infty} = R_G$$

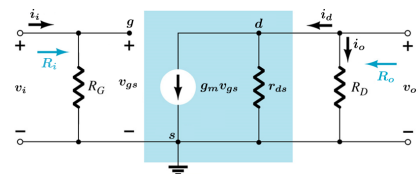
Voltage Gain



No-load voltage gain A_v is given by

$$A_v = \frac{v_o}{v_i} \Big|_{R_L = \infty} = \left(\frac{v_o}{g_m v_{gs}} \right) \left(\frac{g_m v_{gs}}{v_{gs}} \right) \left(v_{gs} \right) = (-R_D || r_{ds}) (g_m) (1) = -g_m (R_D || r_{ds})$$

■ If $r_{ds} \geq 10R_D$, no-load voltage gain A_v reduces to $A_v = -g_m R_D$



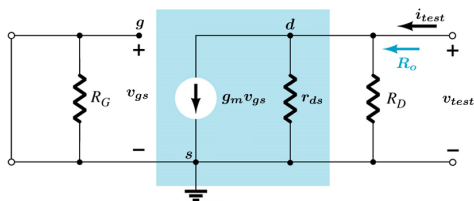
■ For the circuit above, we can obtain the current gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o / R_D}{v_i / R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i} = \frac{R_i}{R_D} A_v$$

■ If $r_{ds} \geq 10R_D$, current gain A_i reduces to

$$A_i = -g_m R_G$$

Output Resistance



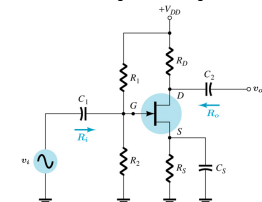
Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$R_o = \frac{v_{test}}{i_{test}} \Big|_{v_{gs}=0, R_L=v_{test}} = R_D || r_{ds}$$

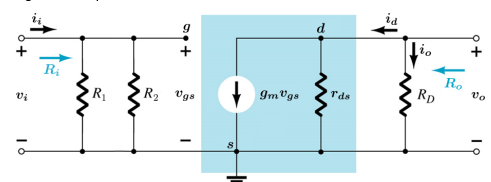
■ If $r_{ds} \geq 10R_D$, then R_o simplifies to $R_o = R_D$.

CS Voltage-Divider Bias Configuration

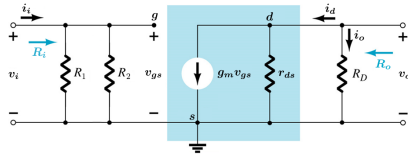
Common-source voltage-divider bias configuration is given below



Corresponding SSAC equivalent circuit is shown below



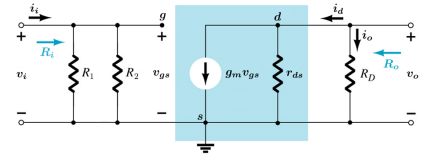
Input Resistance



Input resistance R_i is given as

$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L = \infty} = R_1 || R_2$$

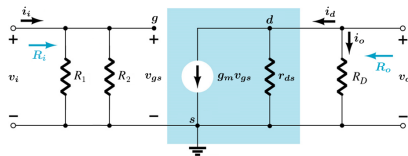
Voltage Gain



No-load voltage gain A_v is given by

$$A_v = \left. \frac{v_o}{v_i} \right|_{R_L = \infty} = \left(\frac{v_o}{g_m v_{gs}} \right) \left(\frac{g_m v_{gs}}{v_{gs}} \right) \left(\frac{v_{gs}}{v_i} \right) = (-R_D || r_{ds}) (g_m) (1) = -g_m (R_D || r_{ds})$$

- If $r_{ds} \geq 10R_D$, no-load voltage gain A_v reduces to $A_v = -g_m R_D$



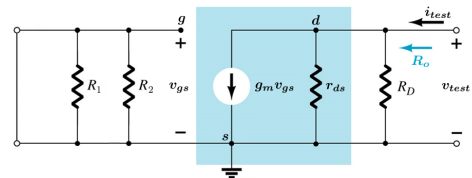
■ For the circuit above, we can obtain the current gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i} = \frac{R_i}{R_D} A_v$$

■ If $r_{ds} \geq 10R_D$, current gain A_i reduces to

$$A_i = -g_m (R_1 || R_2)$$

Output Resistance



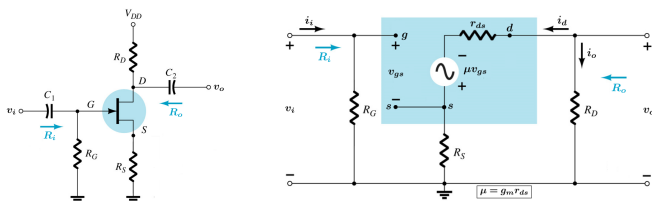
Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$R_o = \left. \frac{v_{test}}{i_{test}} \right|_{v_{gs}=0, R_L=v_{test}} = R_D || r_{ds}$$

- If $r_{ds} \geq 10R_D$, then R_o simplifies to $R_o = R_D$.

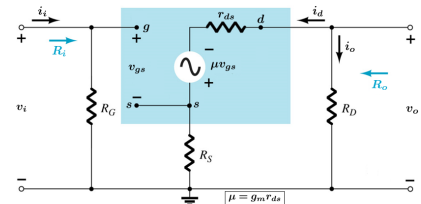
CS Unbypassed Self-Bias Configuration

Common-source unbypassed self-bias configuration and its SSAC equivalent circuit are given on the left and right figures below, respectively.



■ When R_S is not bypassed, we normally use the voltage-controlled voltage source model in the small-signal equivalent circuit as shown above.

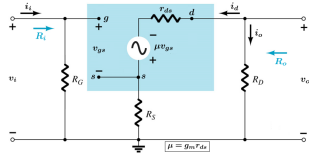
Input Resistance



Input resistance R_i is given as

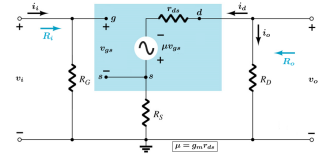
$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L = \infty} = R_G$$

Voltage Gain



No-load voltage gain A_v is given by

$$\begin{aligned}
 A_v &= \left. \frac{v_o}{v_i} \right|_{R_L=\infty} = \left(\frac{v_o}{i_d} \right) \left(\frac{i_d}{v_{gs}} \right) \left(\frac{v_{gs}}{v_i} \right) \\
 &= (-R_D) \left(\frac{\mu}{R_S + R_D + r_{ds}} \right) \left(\frac{v_{gs}}{v_{gs} + i_d R_S} \right) \quad \dots i_d = \frac{\mu v_{gs}}{R_S + R_D + r_{ds}} \\
 &= (-R_D) \left(\frac{\mu}{R_S + R_D + r_{ds}} \right) \left(\frac{1}{1 + \frac{\mu R_S}{R_S + R_D + r_{ds}}} \right) \\
 &= -\frac{\mu R_D}{(\mu + 1) R_S + R_D + r_{ds}} \quad \dots \mu = g_m r_{ds} \\
 &= -\frac{g_m R_D}{1 + g_m R_S + \frac{R_S + R_D}{r_{ds}}}
 \end{aligned}$$



■ If $r_{ds} \geq 10(R_D + R_S)$, no-load voltage gain A_v reduces to

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

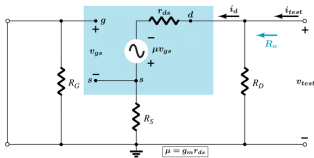
■ If $r_{ds} \geq 10(R_D + R_S)$ and $g_m R_S \gg 1$, no-load voltage gain A_v reduces to

$$A_v \approx -\frac{R_D}{R_S}$$

■ For the circuit above, we can obtain the current gain A_i as follows

$$\begin{aligned}
 A_i &= \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i} \\
 &= \frac{R_i}{R_D} A_v
 \end{aligned}$$

Output Resistance

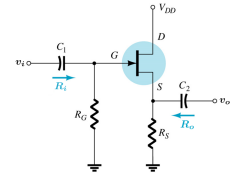


Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above.

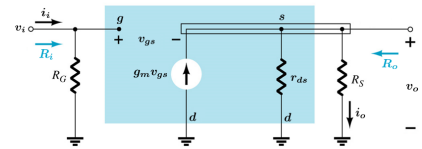
$$\begin{aligned}
 R_o &= \left. \frac{v_{test}}{i_{test}} \right|_{v_s=0, R_L=v_{test}} = \frac{v_{test}}{\frac{v_{test}}{R_D} + i_d} \quad \dots i_{test} = i_{R_D} + i_d \\
 &= \frac{v_{test}}{\frac{v_{test}}{R_D} - \frac{v_{gs}}{R_S}} \quad \dots v_s = -v_{gs}, i_d = \frac{-v_{gs}}{R_S} \\
 &= \frac{v_{test}}{\frac{v_{test}}{R_D} + \frac{v_{test}}{(\mu+1)R_S + r_{ds}}} \quad \dots v_{gs} = -\frac{v_{test}}{(\mu+1) + r_{ds}/R_S} \\
 &= R_D || [(\mu+1)R_S + r_{ds}] \quad \dots \mu = g_m r_{ds} \\
 &= R_D || [(g_m R_S + 1)r_{ds} + R_S] \\
 &\cong R_D
 \end{aligned}$$

Source-Follower Configuration

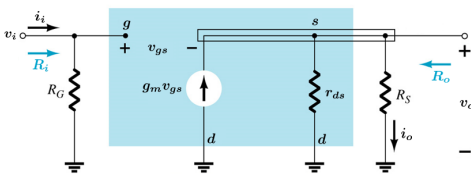
Source-follower (common-drain) configuration is given below



Corresponding SSAC equivalent circuit is shown below



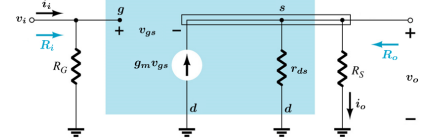
Input Resistance



Input resistance R_i is given as

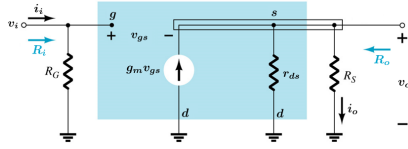
$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L=\infty} = R_G$$

Voltage Gain



No-load voltage gain A_v is given by

$$\begin{aligned}
 A_v &= \left. \frac{v_o}{v_i} \right|_{R_L=\infty} = \left(\frac{v_o}{v_{gs}} \right) \left(\frac{v_{gs}}{v_i} \right) \\
 &= [g_m (R_S || r_{ds})] \left(\frac{1}{1 + g_m (R_S || r_{ds})} \right) \quad \dots v_i = v_{gs} + v_o \\
 &= \frac{g_m (R_S || r_{ds})}{1 + g_m (R_S || r_{ds})} \\
 &\cong 1
 \end{aligned}$$

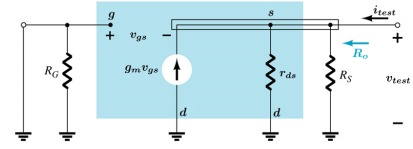


■ For the circuit above, we can obtain the current-gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_S}{v_i/R_i} = \frac{R_i}{R_S} \frac{v_o}{v_i}$$

$$= \frac{R_i}{R_S} A_v$$

Output Resistance



Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above.

$$R_o = \left. \frac{v_{test}}{i_{test}} \right|_{v_s=0, R_L=v_{test}} = \frac{v_{test}}{\frac{v_{test}}{R_S} \parallel r_{ds} - g_m v_{gs}} \quad \dots i_{test} = i_{R_S} \parallel r_{ds} - g_m v_{gs}$$

$$= \frac{v_{test}}{\frac{v_{test}}{R_S} \parallel r_{ds} + g_m v_{test}} \quad \dots v_{test} = -v_{gs}$$

$$= \frac{v_{test}}{\frac{v_{test}}{R_S} \parallel r_{ds} + \frac{v_{test}}{1/g_m}}$$

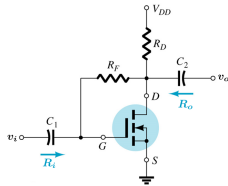
$$= R_S \parallel r_{ds} \parallel \frac{1}{g_m}$$

■ If $(R_S \parallel r_{ds}) \geq 10/g_m$, output resistance R_o reduces to

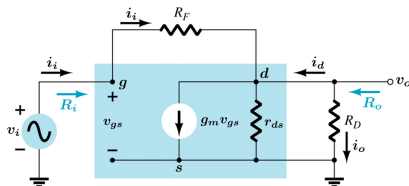
$$R_o \cong \frac{1}{g_m}$$

CS Drain Feedback Configuration

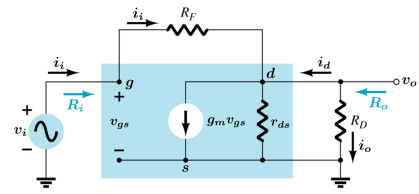
Common-source drain feedback bias configuration is given below



Corresponding SSAC equivalent circuit is shown below



Input Resistance



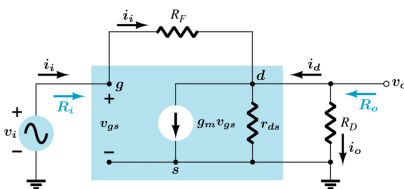
Input resistance R_i is given as

$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L=\infty} = \frac{v_{gs}}{g_m v_{gs} + v_o / (R_D \parallel r_{ds})} \quad \dots v_i = v_{gs}$$

$$= \frac{R_F + R_D \parallel r_{ds}}{1 + g_m (R_D \parallel r_{ds})} \quad \dots v_o = \frac{(1 - g_m R_F) (R_D \parallel r_{ds}) v_{gs}}{R_F + R_D \parallel r_{ds}}$$

$$\cong \frac{R_F}{1 + g_m (R_D \parallel r_{ds})} \quad \dots R_F \gg R_D \parallel r_{ds}$$

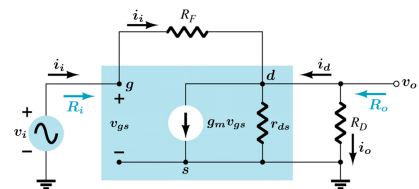
Voltage Gain



No-load voltage gain A_v is given by

$$A_v = \left. \frac{v_o}{v_i} \right|_{R_L=\infty} = \frac{(1 - g_m R_F) (R_D \parallel r_{ds})}{R_F + R_D \parallel r_{ds}} \quad \dots v_i = v_{gs}$$

$$\cong -g_m (R_D \parallel r_{ds}) \parallel R_F \quad \dots g_m R_F \gg 1$$

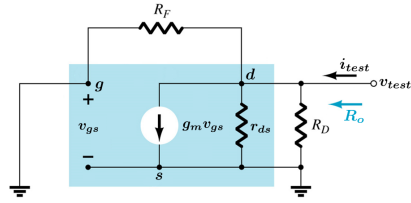


■ For the circuit above, we can obtain the current-gain A_i as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i}$$

$$= \frac{R_i}{R_D} A_v$$

Output Resistance



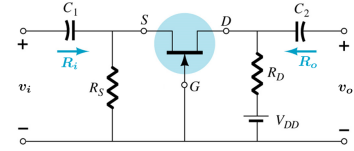
Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$R_o = \left. \frac{v_{test}}{i_{test}} \right|_{v_{gs}=0, R_L=v_{test}} = R_D || r_{ds} || R_F$$

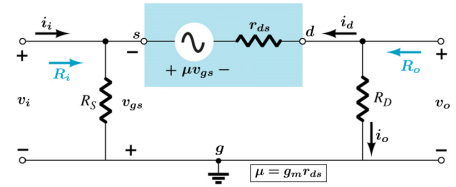
- If a voltage source with source resistance R_s is connected to the input, replace R_F with $[(R_F + R_s) / (1 + g_m R_s)]$ in R_o calculations.

Common-Gate Configuration

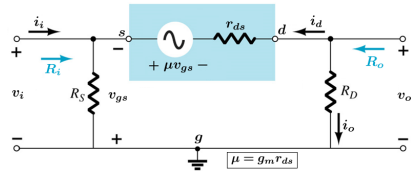
Common-gate configuration is given below



Corresponding SSAC equivalent circuit is shown below



Input Resistance



Input resistance R_i is given as

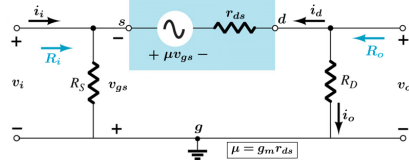
$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L=\infty} = \frac{v_i}{v_i/R_S - i_d} \quad \dots v_i = -v_{gs}$$

$$= \frac{v_i}{v_i/R_S + v_i \left(\frac{R_D + r_{ds}}{\mu + 1} \right)} \quad \dots i_d = \frac{(\mu + 1)v_{gs}}{R_D + r_{ds}}$$

$$= R_S || \frac{R_D + r_{ds}}{1 + g_m r_{ds}} \quad \dots \mu = g_m r_{ds}$$

$$\cong R_S || \frac{1}{g_m} \quad \dots r_{ds} \geq 10R_D \text{ and } g_m r_{ds} \gg 1$$

Voltage Gain



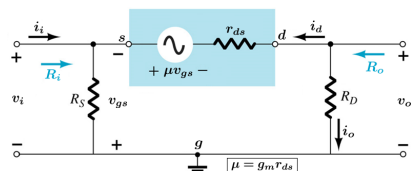
No-load voltage gain A_v is given by

$$A_v = \left. \frac{v_o}{v_i} \right|_{R_L=\infty} = \frac{-i_d R_D}{-v_{gs}} \quad \dots v_i = -v_{gs}$$

$$= \frac{(\mu + 1) R_D}{R_D + r_{ds}} \quad \dots i_d = \frac{(\mu + 1)v_{gs}}{R_D + r_{ds}}$$

$$= \frac{(g_m r_{ds} + 1) R_D}{R_D + r_{ds}} \quad \dots \mu = g_m r_{ds}$$

$$\cong g_m R_D \quad \dots r_{ds} \geq 10R_D \text{ and } g_m r_{ds} \gg 1$$



- For the circuit above, we can obtain the current-gain A_i as follows

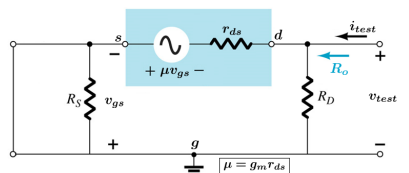
$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i}$$

$$= \frac{R_i}{R_D} A_v$$

- If $r_{ds} \geq 10R_D$ and $g_m r_{ds} \gg 1$, current-gain A_i reduces to

$$A_i = g_m \left(R_S || \frac{1}{g_m} \right) \approx 1$$

Output Resistance



Output resistance, i.e., Thévenin equivalent resistance, R_o is calculated using the test voltage circuit above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$R_o = \left. \frac{v_{test}}{i_{test}} \right|_{v_{gs}=0, R_L=v_{test}} = R_D || r_{ds}$$

- If $r_{ds} \geq 10R_D$, then R_o simplifies to $R_o = R_D$.
- If a voltage source with source resistance R_s is connected to the input, replace r_{ds} with $([1 + g_m (R_s || R_G)] r_{ds} + R_s || R_G)$ in R_o calculations. We can say that $R_o \approx R_D$ in most cases.