FET Small-Signal Analysis

FET SSA C Analysis Steps

1. Draw the SSA C equivalent circuit
   a) Draw the AC equivalent circuit (signal frequency is infinity, i.e., \( f = \infty \))
      i. Capacitors are short circuit, i.e., \( X_C \rightarrow 0 \).
      ii. Kill the DC power sources (i.e., AC value of DC sources is zero).
   b) Replace FET with its small-signal equivalent model.

2. Calculate the three amplifier parameters: \( R_i \), \( R_o \) and \( A_v \)
   a) Calculate no-load input resistance, \( R_i = \left. \frac{v_o}{v_i} \right|_{R_L=\infty} \).
   b) Calculate output resistance, \( R_o \).
   c) Calculate no-load voltage gain, \( A_v = \left. \frac{v_o}{v_i} \right|_{R_L=\infty} \).
FET Small-Signal Model

Small-signal equivalent model for a FET transistor is provided below. This model and its analysis is the same for all FET types, i.e., JFET, DMOSFET, EMOSFET, n-channel and p-channel.

Here,

- \( g_m = g_f = y_f = \frac{\partial I_D}{\partial V_{GS}} \bigg|_{Q}\text{ is the forward transfer conductance,} \)
- \( r_{ds} = \frac{1}{g_{os}} = \frac{1}{y_{os}} = \frac{\partial V_{DS}}{\partial I_D} \bigg|_{Q}\text{ is the output resistance.} \)

Forward transfer conductance \( g_m \) is mostly called as the transconductance parameter.

When \( r_{ds} \neq \infty \), we can also use the voltage-controlled voltage source model (via Norton-to-Thévenin transformation) as shown below. We mostly use this model for the common-gate and unbypassed self-bias configurations.

Here \( \mu = g_m r_{ds} \) is the forward transfer-voltage gain.

- Typical values of \( g_m \) run from 1 mS to 5 mS,
- Typical values of \( r_{ds} \) run from 20 k\( \Omega \) to 100 k\( \Omega \),
- Consequently, typical values of \( \mu \) run from 20 to 500.
Transconductance Parameter \((g_m)\)

Transconductance parameter \(g_m\) is given by

\[
g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{Q\text{-point}} \approx \left. \frac{\Delta I_D}{\Delta V_{GS}} \right|_{Q\text{-point}}
\]

In other words, \(g_m\) is the slope of the characteristics at the point of operation as shown below.

\[
g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad (= \text{Slope at } Q\text{-point})
\]

Let us derive \(g_m\) for the JFET equation, \(I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2\)

\[
g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{Q\text{-point}} = \left. \frac{2I_{DSS}}{|V_P|} \left(1 - \frac{V_{GS}}{V_P}\right) \right|_{Q\text{-point}}
\]

\[
= 2I_{DSS} \sqrt{\frac{I_{DQ}}{I_{DSS}}} \quad \ldots I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2
\]

\[
= g_{m0} \sqrt{\frac{I_{DQ}}{I_{DSS}}} \quad \ldots g_{m0} = \frac{2I_{DSS}}{|V_P|}
\]

Let us derive \(g_m\) for the MOSFET equation, \(I_D = k \left(V_{GS} - V_{GS(Th)}\right)^2\)

\[
g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{Q\text{-point}} = 2k \left(V_{GS} - V_{GS(Th)}\right) \left|_{Q\text{-point}} \right.
\]

\[
= 2k \left(V_{GS} - V_{GS(Th)}\right)
\]

\[
= 2\sqrt{k} \sqrt{I_{DQ}} \quad \ldots I_{DQ} = k \left(V_{GS} - V_{GS(Th)}\right)^2
\]
Phase Relationship

The phase relationship between input and output depends on the amplifier configuration circuit as listed below.

- Common-Source: 180 degrees
- Common-Gate: 0 degrees
- Common-Drain: 0 degrees (Source-Follower)

Common-Source Fixed-Bias Configuration

Common-source fixed-bias configuration is given below

Corresponding SSAC equivalent circuit is shown below
### Input Resistance

Input resistance $R_i$ is given as

$$R_i = \frac{v_i}{i_i} \bigg|_{R_L=\infty} = R_G$$

### Voltage Gain

No-load voltage gain $A_v$ is given by

$$A_v = \frac{v_o}{v_i} \bigg|_{R_L=\infty} = \left(\frac{v_o}{g_m v_{gs}} \right) \left(\frac{g_m v_{gs}}{v_{gs}} \right) \left(\frac{v_{gs}}{v_i} \right)$$

$$= (-R_D||r_{ds}) \left(g_m\right)$$

$$= -g_m \left(R_D||r_{ds}\right)$$

- If $r_{ds} \geq 10R_D$, voltage gain $A_v$ reduces to

$$A_v = -g_m R_D$$
FET Small-Signal Analysis Common-Source Fixed-Bias Configuration

For the circuit above, we can obtain the current gain $A_i$ as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i} = \frac{R_i}{R_D} A_v$$

If $r_{ds} \geq 10R_D$, current gain $A_i$ reduces to

$$A_i = -g_m R_G$$

Output Resistance

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$R_o = \left. \frac{v_{test}}{i_{test}} \right|_{v_{gs}=0, R_L=v_{test}} = R_D || r_{ds}$$

If $r_{ds} \geq 10R_D$, then $R_o$ simplifies to $R_o = R_D$. 
CS Self-Bias Configuration

Common-source self-bias configuration is given below.

Corresponding SSAC equivalent circuit is shown below.

Input Resistance

Input resistance $R_i$ is given as

$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L = \infty} = R_G$$
Voltage Gain

No-load voltage gain $A_v$ is given by

$$A_v = \left| \frac{v_o}{v_i} \right|_{R_L=\infty} = \left( \frac{v_o}{g_m v_{gs}} \right) \left( \frac{g_m v_{gs}}{v_{gs}} \right) \left( \frac{v_{gs}}{v_i} \right)$$

$$= (-R_D||r_{ds}) \left( g_m \right) (1)$$

$$= -g_m \left( R_D||r_{ds} \right)$$

- If $r_{ds} \geq 10R_D$, no-load voltage gain $A_v$ reduces to

$$A_v = -g_m R_D$$

For the circuit above, we can obtain the current gain $A_i$ as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i}$$

$$= \frac{R_i}{R_D} A_v$$

- If $r_{ds} \geq 10R_D$, current gain $A_i$ reduces to

$$A_i = -g_m R_G$$
Output Resistance

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$R_o = \frac{v_{test}}{i_{test}} \bigg|_{v_{gs}=0,R_L=v_{test}} = R_D || r_{ds}$$

- If $r_{ds} \geq 10R_D$, then $R_o$ simplifies to $R_o = R_D$.

CS Voltage-Divider Bias Configuration

Common-source voltage-divider bias configuration is given below.

Corresponding SSAC equivalent circuit is shown below.
**Input Resistance**

Input resistance $R_i$ is given as

$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L=\infty} = R_1 || R_2$$

**Voltage Gain**

No-load voltage gain $A_v$ is given by

$$A_v = \left. \frac{v_o}{v_i} \right|_{R_L=\infty} = \left( \frac{v_o}{g_m v_{gs}} \right) \left( g_m v_{gs} \right) \left( \frac{v_{gs}}{v_i} \right)$$

$$= (-R_D || r_{ds}) (g_m) (1)$$

$$= -g_m (R_D || r_{ds})$$

- If $r_{ds} \geq 10R_D$, no-load voltage gain $A_v$ reduces to

$$A_v = -g_m R_D$$
For the circuit above, we can obtain the current gain $A_i$ as follows:

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i}$$

$$= \frac{R_i}{R_D} A_v$$

If $r_{ds} \geq 10R_D$, current gain $A_i$ reduces to

$$A_i = -g_m (R_1 || R_2)$$

Output Resistance

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$R_o = \frac{v_{test}}{i_{test}} \bigg|_{v_{gs}=0,R_L=v_{test}} = R_D || r_{ds}$$

If $r_{ds} \geq 10R_D$, then $R_o$ simplifies to $R_o = R_D$. 
CS Unbypassed Self-Bias Configuration

Common-source unbypassed self-bias configuration and its SSAC equivalent circuit are given on the left and right figures below, respectively.

- When $R_S$ is not bypassed, we normally use the voltage-controlled voltage source model in the small-signal equivalent circuit as shown above.

Input Resistance

Input resistance $R_i$ is given as

$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L=\infty} = R_G$$
Voltage Gain

No-load voltage gain $A_v$ is given by

$$A_v = \frac{v_o}{v_i} \bigg|_{R_L=\infty} = \left( \frac{v_o}{i_d} \right) \left( \frac{i_d}{v_{gs}} \right) \left( \frac{v_{gs}}{v_i} \right)$$

$$= (-R_D) \left( \frac{\mu}{R_S + R_D + r_{ds}} \right) \left( \frac{v_{gs}}{v_i + i_d R_S} \right)$$

$$\Rightarrow i_d = \frac{\mu v_{gs}}{R_S + R_D + r_{ds}}$$

$$\Rightarrow \mu = g_m r_{ds}$$

- If $r_{ds} \geq 10(R_D + R_S)$, no-load voltage gain $A_v$ reduces to

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

- If $r_{ds} \geq 10(R_D + R_S)$ and $g_m R_S \gg 1$, no-load voltage gain $A_v$ reduces to

$$A_v \approx -\frac{R_D}{R_S}$$

- For the circuit above, we can obtain the current gain $A_i$ as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i}$$

$$\quad = \frac{R_i}{R_D} A_v$$
Output Resistance

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit above.

$$R_o = \frac{v_{test}}{i_{test}} \bigg|_{v_s=0, R_L=v_{test}}$$

$$= \frac{v_{test}}{R_D} + i_d$$

$$= \frac{v_{test}}{R_D} - \frac{v_{gs}}{R_S}$$

$$\ldots v_s = -v_{gs}, i_d = -\frac{v_{gs}}{R_S}$$

$$= \frac{v_{test}}{R_D} + \frac{v_{test}}{(\mu + 1) R_S + r_{ds}}$$

$$\ldots v_{gs} = -\frac{v_{test}}{(\mu + 1) + r_{ds}/R_S}$$

$$= R_D \| [(\mu + 1) R_S + r_{ds}]$$

$$\ldots \mu = g_m r_{ds}$$

$$= R_D \| [(g_m R_S + 1) r_{ds} + R_S]$$

$$\cong R_D$$

Source-Follower Configuration

Source-follower (common-drain) configuration is given below

Corresponding SSAC equivalent circuit is shown below
Input Resistance

Input resistance $R_i$ is given as

$$R_i = \left. \frac{v_i}{i_i} \right|_{R_L=\infty} = R_G$$

Voltage Gain

No-load voltage gain $A_v$ is given by

$$A_v = \left. \frac{v_o}{v_i} \right|_{R_L=\infty} = \left( \frac{v_o}{v_{gs}} \right) \left( \frac{v_{gs}}{v_i} \right)$$

$$= \frac{g_m (R_S||r_{ds})}{1 + g_m (R_S||r_{ds})}$$

$$\approx 1$$
FET Small-Signal Analysis Source-Follower Configuration

For the circuit above, we can obtain the current-gain $A_i$ as follows:

$$A_i = \frac{i_o}{i_i} = \frac{v_o}{R_S} \frac{R_i}{v_i} = \frac{R_i}{R_S} A_v$$

Output Resistance

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit above.

$$R_o = \left. \frac{v_{test}}{i_{test}} \right|_{v_S=0, R_L=v_{test}} = \frac{v_{test}}{R_S || r_{ds}} - g_m v_{gs}$$

$$= \frac{v_{test}}{R_S || r_{ds}} + g_m v_{test} \quad \cdots v_{test} = -v_{gs}$$

$$= \frac{v_{test}}{R_S || r_{ds}} + \frac{v_{test}}{1/g_m}$$

$$= R_S || r_{ds} \left[ \frac{1}{g_m} \right]$$

If $(R_S || r_{ds}) \geq 10/g_m$, output resistance $R_o$ reduces to

$$R_o \approx \frac{1}{g_m}$$
CS Drain Feedback Configuration

Common-source drain feedback bias configuration is given below

\[ \text{Corresponding SSAC equivalent circuit is shown below} \]

\[ \text{Input Resistance} \]

Input resistance \( R_i \) is given as

\[ R_i = \left. \frac{v_i}{i_i} \right|_{R_L=\infty} = \frac{v_{gs}}{g_m v_{gs} + v_o / (R_D || r_{ds})} \quad \ldots v_i = v_{gs} \]

\[ = \frac{R_F + R_D || r_{ds}}{1 + g_m (R_D || r_{ds})} \quad \ldots v_o = \frac{(1 - g_m R_F) (R_D || r_{ds}) v_{gs}}{R_F + R_D || r_{ds}} \]

\[ \approx \frac{R_F}{1 + g_m (R_D || r_{ds})} \quad \ldots R_F \gg R_D || r_{ds} \]
Voltage Gain

No-load voltage gain $A_v$ is given by

$$A_v = \left. \frac{v_o}{v_i} \right|_{R_L=\infty} = \frac{(1 - g_m R_F) (R_D || r_{ds})}{R_F + R_D || r_{ds}}$$

\[\approx -g_m (R_D || r_{ds} || R_F)\]

... $v_i = v_{gs}$

... $g_m R_F \gg 1$

- For the circuit above, we can obtain the current-gain $A_i$ as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o}{R_D} = \frac{R_i}{R_D} \frac{v_o}{v_i}$$

$$= \frac{R_i}{R_D} A_v$$
Output Resistance

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$R_o = \frac{v_{test}}{i_{test}} \bigg|_{v_{gs}=0, R_L=v_{test}} = R_D || r_{ds} || R_F$$

- If a voltage source with source resistance $R_s$ is connected to the input, replace $R_F$ with $[(R_F + R_s) / (1 + g_m R_s)]$ in $R_o$ calculations.

Common-Gate Configuration

Common-gate configuration is given below

Corresponding SSAC equivalent circuit is shown below
### Input Resistance

**Input resistance** $R_i$ is given as

$$R_i = \frac{v_i}{i} \bigg|_{R_L=\infty} = \frac{v_i}{v_i/R_S - i_d}$$  

\[\ldots v_i = -v_{gs}\]

$$= \frac{v_i}{v_i/R_S + v_i/(R_D + r_{ds})}$$  

\[\ldots i_d = \frac{(\mu + 1)v_{gs}}{R_D + r_{ds}}\]

$$= R_S \left| \frac{R_D + r_{ds}}{1 + g_m r_{ds}} \right|$$  

\[\ldots \mu = g_m r_{ds}\]

$$\approx R_S \left| \frac{1}{g_m} \right| \geq 10R_D \text{ and } g_m r_{ds} \gg 1$$

### Voltage Gain

**No-load voltage gain** $A_v$ is given by

$$A_v = \frac{v_o}{v_i} \bigg|_{R_L=\infty} = -\frac{i_d R_D}{-v_{gs}}$$  

\[\ldots v_i = -v_{gs}\]

$$= \frac{(\mu + 1)R_D}{R_D + r_{ds}}$$  

\[\ldots i_d = \frac{(\mu + 1)v_{gs}}{R_D + r_{ds}}\]

$$= \frac{(g_m r_{ds} + 1)R_D}{R_D + r_{ds}}$$  

\[\ldots \mu = g_m r_{ds}\]

$$\approx g_m R_D$$  

\[\ldots r_{ds} \geq 10R_D \text{ and } g_m r_{ds} \gg 1\]
For the circuit above, we can obtain the current-gain $A_i$ as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D} \frac{v_o}{v_i}$$

$$= \frac{R_i}{R_D} A_v$$

- If $r_{ds} \geq 10R_D$ and $g_m r_{ds} \gg 1$, current-gain $A_i$ reduces to

$$A_i = g_m \left( R_S \parallel \frac{1}{g_m} \right) \approx 1$$

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$R_o = \left. \frac{v_{test}}{i_{test}} \right|_{v_s=0,R_L=v_{test}} = R_D \parallel r_{ds}$$

- If $r_{ds} \geq 10R_D$, then $R_o$ simplifies to $R_o = R_D$.

- If a voltage source with source resistance $R_s$ is connected to the input, replace $r_{ds}$ with $\left( [1 + g_m (R_s || R_G)] r_{ds} + R_s || R_G \right)$ in $R_o$ calculations. We can say that $R_o \approx R_D$ in most cases.