# ELE 230 Electronics I

Hacettepe University

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27 May 2018

1. These lecture notes are complete and regularly updated at the address below: http://www.ee.hacettepe.edu.tr/∼usezen/ele230/.

2. These lecture notes use material from several other sources like Prof. Selçuk Geçim's lecture notes, "Electronic Devices and Circuit Theory, 11th ed." by Boylestad and Nashelsky and and its instructor materials.

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# Textbook

Textbooks:

1. Boylestad and Nashelsky, ***Electronic Devices and Circuit Theory***, Prentice Hall, 11th ed, 2012.

2. Sedra and Smith, ***Microelectronic Circuits***, Oxford Press, 2009 (6th ed.)

Supplementary books:

1. Millman and Halkias, ***Integrated Electronics***, McGraw-Hill.

2. Horowitz and Hill, ***The Art of Electronics***, Cambridge, 3rd ed.

# Chapter 1

# Semiconductor Diodes

## 1.1 Circuit Symbol

Diode is a nonlinear two-terminal device whose circuit symbol is like an arrowhead shown in Figure 1.1 below.

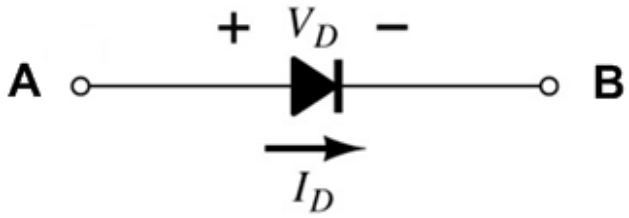



Figure 1.1: Diode circuit symbol.

- Voltage across the diode, $V_D$, is normally defined as the voltage difference between back end of the arrowhead and front end of the arrowhead (voltage difference between terminal $A$ and terminal $B$), i.e.,

$$\boxed{V_D = V_A - V_B} \tag{1.1.1}$$

.

- Current through the diode, $I_D$, is defined in the direction of the arrowhead (flowing from terminal $A$ to terminal $B$), i.e.,

$$\boxed{I_D = I_{AB}} \tag{1.1.2}$$

.

- Diode is called **forward biased** (FB) when $V_A \geq V_B$, i.e., $V_D \geq 0$, and called **reverse biased** (RB) when $V_A < V_B$, i.e., $V_D < 0$.

## 1.2 Ideal Diode Model

Ideally diode conducts current in only one direction and blocks current in the opposite direction. Thus,

- Ideal diode is **short circuit** (i.e., ON) when it is **forward biased**.

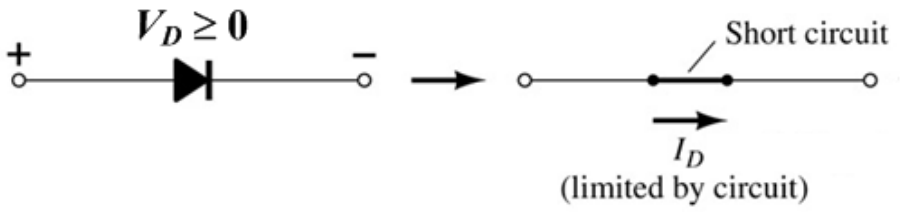



Figure 1.2: Ideal diode is short circuit when it is forward biased.

and **open circuit** (i.e., OFF) when it is **reverse biased**.

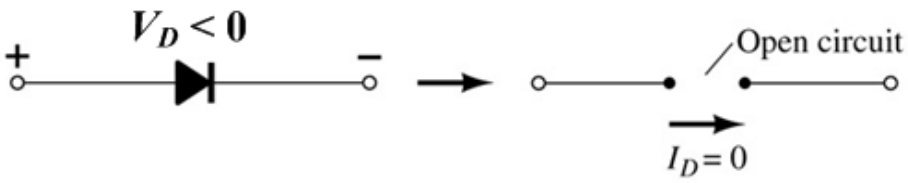



Figure 1.3: Ideal diode is open circuit when it is reverse biased.

Consequently, characteristics curve of the ideal diode is given by

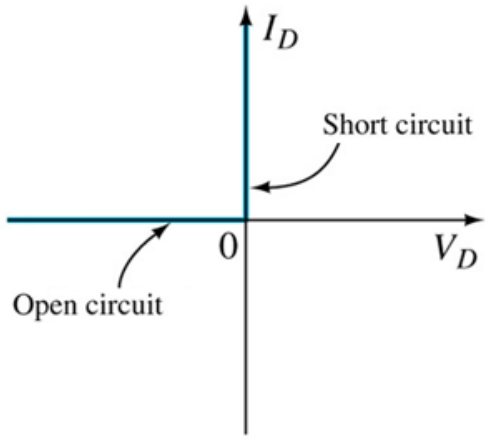



Figure 1.4: Characteristics curve of the ideal diode.

We can summarize the ideal diode with its state and circuit behaviour with

$$\text{Ideal diode state} = \begin{cases} ON, & \text{if } V_D \geq 0 \\ OFF, & \text{if } V_D < 0 \end{cases} \tag{1.2.3}$$

and

| **Ideal Diode Model** | | |
|---|---|---|
| **State** | **Circuit Behaviour** | **Test Condition** |
| ON | $V_D = 0$ | $I_D \geq 0$ |
| OFF | $I_D = 0$ | $V_D < 0$ |

If you make a **wrong assumption** about the state of the diode, then you will find that the **test condition will fail** (once you calculate the circuit voltage and currents).

- For example, if you have assumed the diode to be ON while it should be OFF, then you will find $I_D < 0$, failing the test condition.
- Similarly, if you have assumed the diode to be OFF while it should be ON, then you will find $V_D \geq 0$, failing the test condition.

### 1.2.1 Determining State of an Ideal Diode

Using circuit behaviour and the test condition for the OFF state, let us devise a method to determine the state of the ideal diode.

**Determining State of an Ideal Diode**

1. Obtain the expression for $V_D$ in terms of the diode current $I_D$ from the electronic circuit.
2. Insert $I_D = 0$ in to this expression
3. Then, the diode state is given by

$$\text{Ideal diode state} = \begin{cases} ON, & \text{if } V_D|_{I_D=0} \geq 0 \\ OFF, & \text{if } V_D|_{I_D=0} < 0 \end{cases} \tag{1.2.4}$$

**Example 1.1:** Consider the circuit below and find $I_D$ and $V_D$. Assume the diode is **ideal**.

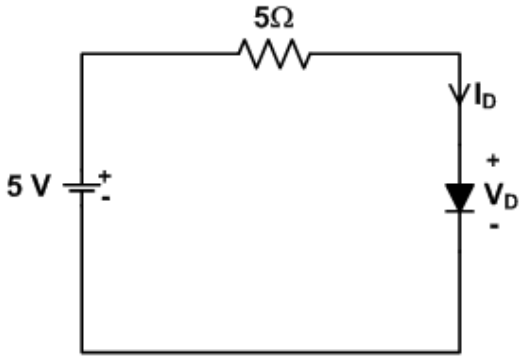



Figure 1.5: Diode circuit for Example 1.1.

**Solution:** First we need to determine the state of the ideal diode (i.e., ON or OFF). So, let us write down the KVL equation and obtain $V_D$

$$V_D = 5 - 5\, I_D$$

From the equation above, $V_D|_{I_D=0} = 5 \geq 0$. So, the diode is ON. Thus,

$$V_D = 0\,\text{V} \qquad \ldots \text{from circuit behaviour}$$
$$I_D = \frac{5 - V_D}{5} = \frac{5 - 0}{5} = 1\,\text{A}.$$

## 1.3 $p$-$n$ Junction Diodes

In an ***n*-type** semiconductor, **majority carriers** are **electrons** and **minority carriers** are **holes**.

Similarly, in a ***p*-type** semiconductor, **majority carriers** are **holes** and **minority carriers** are **electrons**.

When we join $n$-type and $p$-type semiconductors (Silicon or Germanium) together, we obtain a $p$-$n$ junction as shown in Figure 1.6 below.

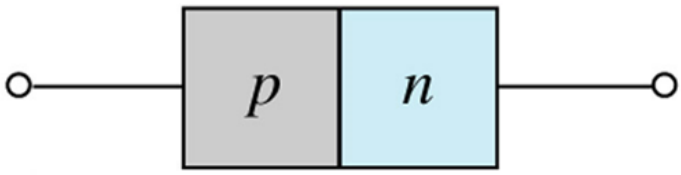



Figure 1.6: A $p$-$n$ junction.

Current formed due to the movement of majority carriers across the junction is called the **majority carrier current**, $I_{\text{majority}}$.

Similarly, current formed due to the movement of minority carriers across the junction is called the **minority carrier current**, $I_s$. Note that, minority carrier and majority carrier currents flow in **opposite** directions.

When the materials are joined, the negatively charged atoms of the $n$-type side are attracted to the positively charged atoms of the $p$-type side.

Electrons in the $n$-type material migrate across the junction to the $p$-type material (electron flow).

Or, you could also say that holes in the $p$-type material migrate across the junction to the $n$-type material (conventional current flow).

The result is the formation of a **depletion layer** around the junction intersection, as shown in Figure 1.7 below.

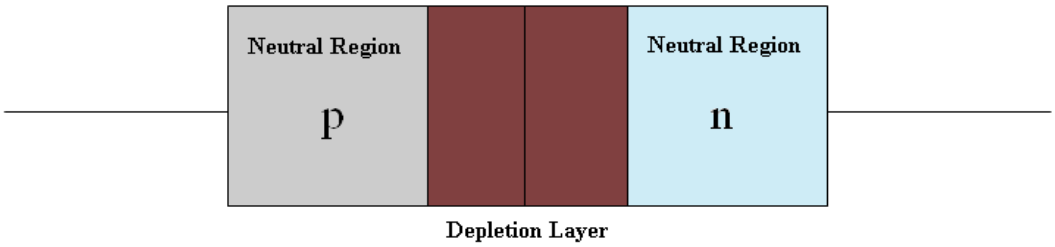



Figure 1.7: Depletion layer in a $p$-$n$ junction.

Normally, depletion layer is not symmetric around the intersection as the doping levels of $n$-side and $p$-side are usually not the same.

**Operating Conditions**

- **No Bias:** No voltage is applied and no current is flowing.
- **Reverse Bias:** Negative voltage (i.e., opposite polarity with the $p$-$n$ junction) is applied.
- **Forward Bias:** Positive voltage (i.e., same polarity with the $p$-$n$ junction) is applied.

### 1.3.1 No Bias Condition

- No external voltage is applied to the $p$-$n$ junction as shown in Figure 1.8 below. So, $V_D = 0\,\text{V}$ and no current is flowing $I_D = 0\,\text{A}$. Under no bias, only a modest depletion layer exists as seen in Figure 1.8 below.

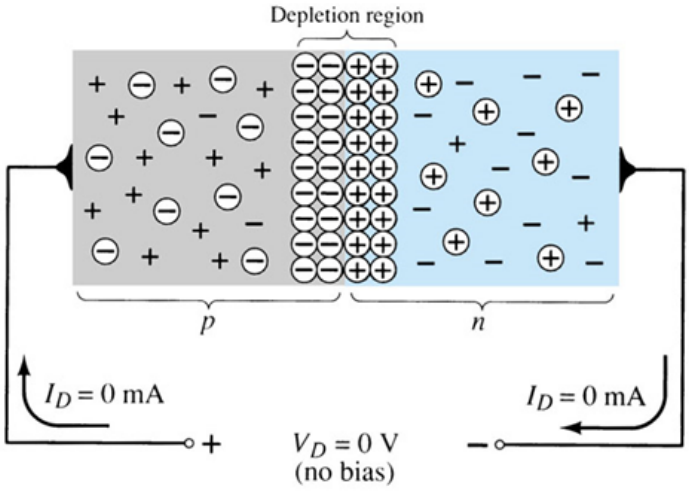



Figure 1.8: $p$-$n$ junction under no bias.

- No bias circuit behaviour is also shown in Figure 1.9 below

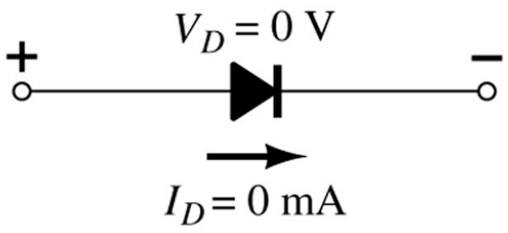



Figure 1.9: Diode behaviour under no bias.

### 1.3.2 Reverse Bias Condition

- External voltage is applied across the $p$-$n$ junction in the opposite polarity of the $p$- and $n$-type materials, as shown in Figure 1.10 below.
- This causes the depletion layer to widen as shown below, as electrons in the $n$-type material are attracted towards the positive terminal and holes in the $p$-type material are attracted towards the negative terminal. Thus, the majority carrier current is zero, i.e., $I_{\text{majority}} = 0$.
- However, minority carriers move along the electric field across the junction forming the **minority carrier current**, $I_s$. Sometimes, this current is also called as the **reverse saturation current**.

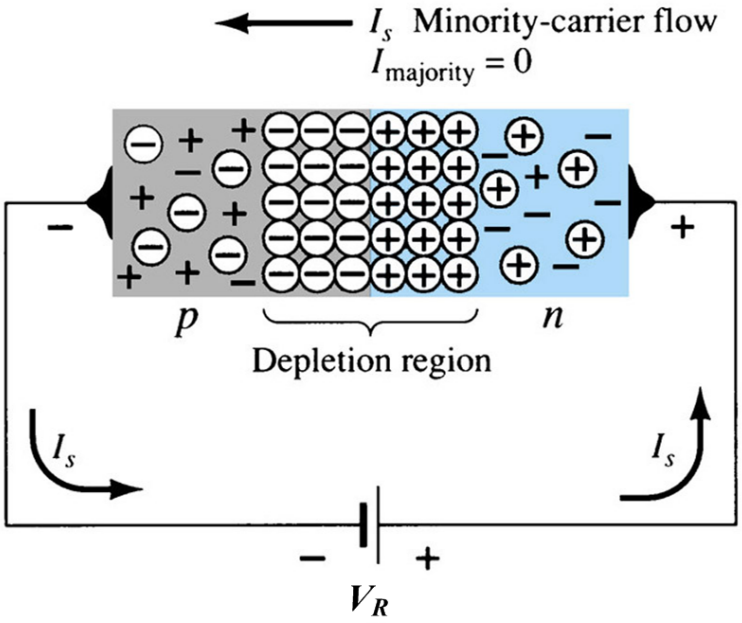



Figure 1.10: $p$-$n$ junction under reverse bias.

- Reverse bias circuit behaviour is also shown in Figure 1.11 below

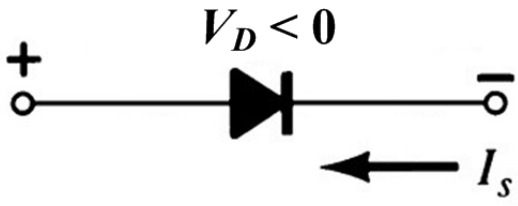



Figure 1.11: Diode behaviour under reverse bias.

- Thus, diode current $I_D$ under reverse bias is given by

$$I_D = I_{\text{majority}} - I_s = 0 - I_s = -I_s. \tag{1.3.5}$$

### 1.3.3 Forward Bias Condition

- External voltage is applied across the $p$-$n$ junction in the same polarity of the $p$- and $n$-type materials, as shown in Figure 1.12 below.
- The depletion layer is narrow. So, electrons from the $n$-type material and holes from the $p$-type material have sufficient energy to cross the junction forming the **majority carrier current**, $I_{\text{majority}}$
- Minority carrier current $I_s$ is still present in the opposite direction

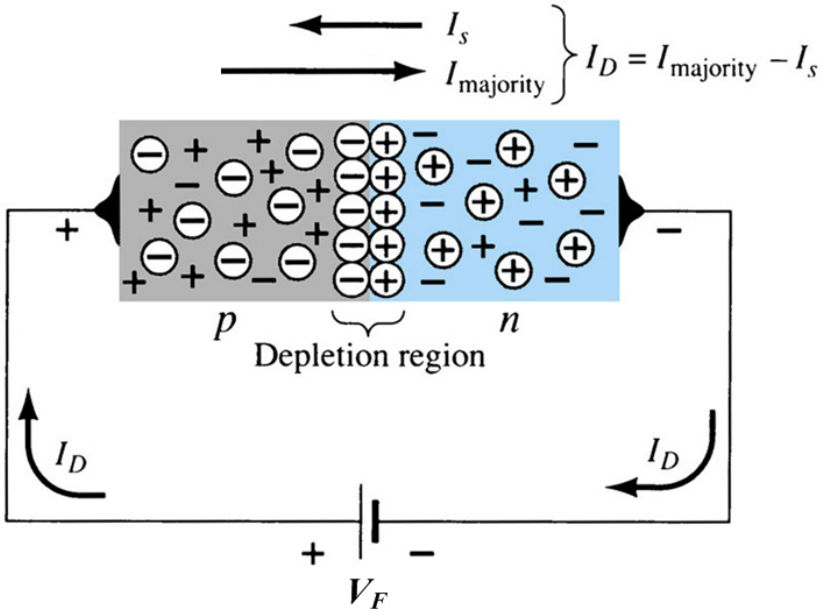



Figure 1.12: $p$-$n$ junction under forward bias.

- Forward bias circuit behaviour is also shown in Figure 1.13 below

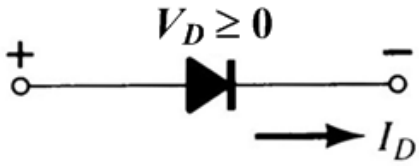



Figure 1.13: Diode behaviour under forward bias.

- Thus, diode current $I_D$ under forward bias is given by

$$I_D = I_{\text{majority}} - I_s. \tag{1.3.6}$$

- Normally $I_{\text{majority}} \gg I_s$, so diode current $I_D$ under forward bias is approximately equal to the majority carrier current, i.e.,

$$I_D \approx I_{majority}. \tag{1.3.7}$$

### 1.3.4 Diode Characteristic Equation

Empirically obtained diode **characteristics curve** covering all three operating conditions is shown in Figure 1.14 below

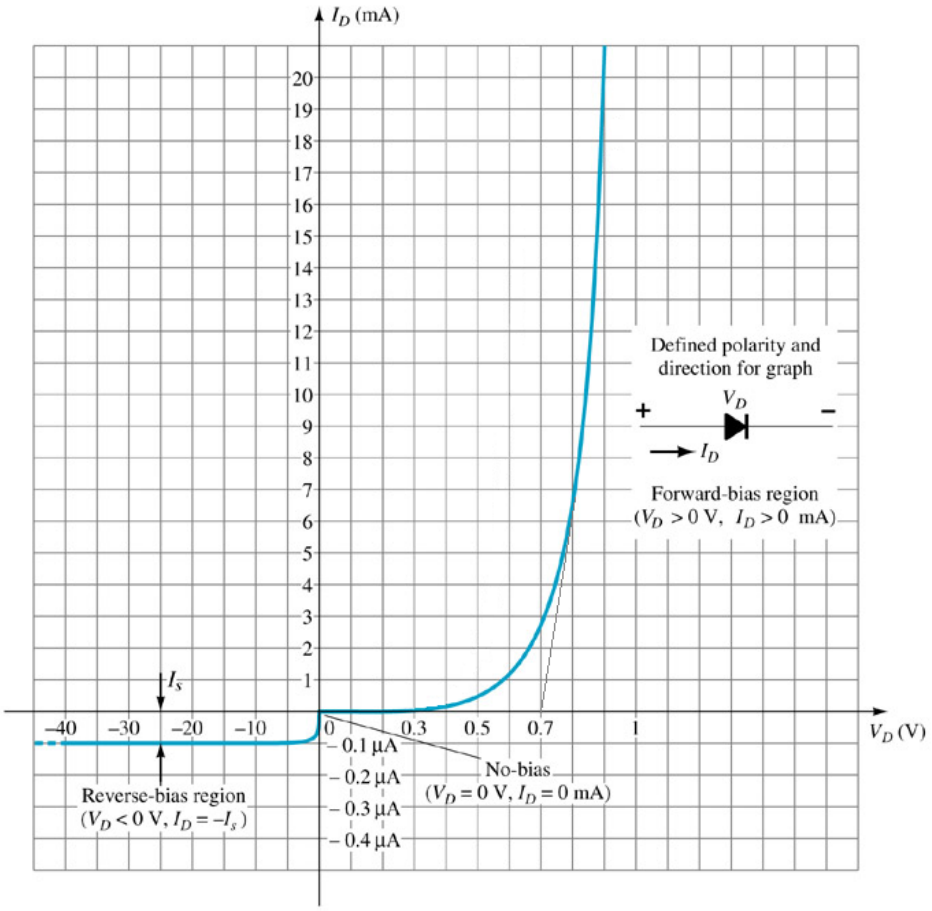



Figure 1.14: Diode characteristics curve

- Diode characteristic equation (also known as the Shockley diode equation) describing the diode characteristics curve is given below

$$\boxed{I_D = I_s \left(e^{V_D/\gamma} - 1\right)} \tag{1.3.8}$$

where $\gamma$, sometimes expressed as $V_T$, is the **thermal voltage** given by

$$\gamma = \frac{kT}{q} \tag{1.3.9}$$

with $k$, $q$ and $T$ being the Boltzman constant, the charge of an electron and temperature in Kelvins, respectively. Note that, $\frac{k}{q}$ is constant given by

$$\frac{k}{q} = \eta\, 8.6173 \times 10^{-5}\,\mathrm{V/K} \tag{1.3.10}$$

where $\eta = 1$ for Ge and $\eta = 2$ for Si for relatively low levels of diode current (at or below the knee of the curve) and $\eta = 1$ for Ge and Si for higher levels of diode current (in the rapidly increasing section of the curve). We can safely assume $\eta = 1$ for most cases.

- Under forward bias, diode characteristic equation simplifies (as $e^{V_D/\gamma} \gg 1$) to the **simplified forward bias diode equation** below

$$I_D \approx I_s e^{V_D/\gamma} \tag{1.3.11}$$

- Under reverse bias, diode characteristic equation simplifies (as $e^{V_D/\gamma} \ll 1$) to the following

$$I_D \approx -I_s \tag{1.3.12}$$

- Note that, $\gamma$ only depends on the temperature (expressed in Kelvin units).

  So, thermal voltage $\gamma$ at room temperature $T = 300\,\mathrm{K}$ (i.e., $T = 27\,^\circ\mathrm{C}$) is given by

$$\boxed{\gamma = \gamma\,|_{T=300\,\mathrm{K}} = 26\,\mathrm{mV}.} \tag{1.3.13}$$

  If we take the room temperature as $T = 25\,^\circ\mathrm{C}$, then thermal voltage becomes

$$\gamma\,|_{T=298\,\mathrm{K}} = 25\,\mathrm{mV}. \tag{1.3.14}$$

  NOTE: Temperature in Kelvin ($T$) is obtained from the temperature in Celsius ($T_C$) as follows

$$T = T_C + 273 \tag{1.3.15}$$

### 1.3.5 Zener Region (or Avalanche Breakdown Region)

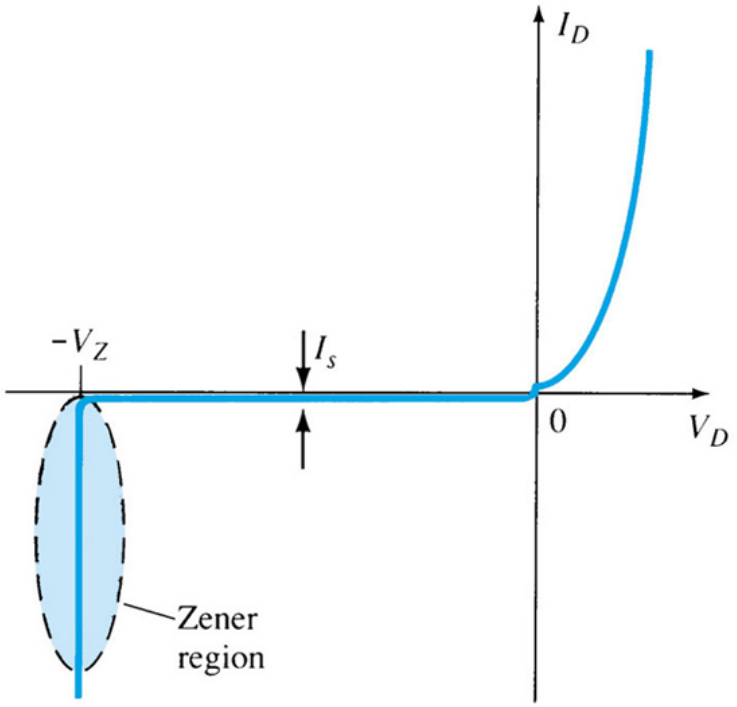



Figure 1.15: Zener region (or avalanche breakdown region)

Even though the scale of Figure 1.14 is in tens of volts in the negative region, there is a point where the application of too negative a voltage will result in a sharp change in the characteristics, as shown in Figure 1.15. The current increases at a very rapid rate in a direction opposite to that of the positive voltage region. The reverse-bias potential that results in this dramatic change in characteristics is called the Zener potential and is given the symbol $V_Z$.

As the voltage across the diode increases in the reverse-bias region, the velocity of the minority carriers responsible for the reverse saturation current $I_s$ will also increase. Eventually, their velocity and associated kinetic energy will be sufficient to release additional carriers (i.e., avalanche effect) through collisions with otherwise stable atomic structures. That is, an ionization process will result whereby valence electrons absorb sufficient energy to leave the parent atom. These additional carriers can then aid the ionization process to the point where a high avalanche current is established and the **avalanche breakdown** region determined.

The avalanche region ($V_Z$) can be brought closer to the vertical axis by increasing the doping levels in the $p$- and $n$-type materials. However, as $V_Z$ decreases to very low levels, such as 5 V, another mechanism, called **Zener breakdown**, will contribute to the sharp change in the characteristic.

It occurs because there is a strong electric field in the region of the junction that can disrupt the bonding forces within the atom and generate carriers generally **via tunnelling** (sometimes called as tunnelling breakdown) of the majority carriers under reverse-bias electric field when the valence band of the highly doped $p$-region is aligned with the conduction band of the highly doped $n$-region.

Although the Zener breakdown mechanism is a significant contributor only at lower levels of $V_Z$, this sharp change in the characteristic at any level is called the Zener region and diodes employing this unique portion of the characteristic of a $p$-$n$ junction are called **Zener diodes**.

### 1.3.6 Peak Inverse Voltage (PIV) Rating

Avalanche breakdown region of the semiconductor diode must be avoided if the diode is supposed to work as an ON and OFF device.

The maximum reverse-bias potential that can be applied before entering the avalanche breakdown region is called the **peak inverse voltage** (referred to simply as the **PIV rating** ) or the **peak reverse voltage** (denoted by **PRV rating**).

If an application requires a PIV rating greater than that of a single unit, a number of diodes of the same characteristics can be connected in series.

Similarly, diodes can be also connected in parallel to increase the current-carrying capacity.

### 1.3.7 Forward Bias Turn-On Voltage ($V_{D(ON)}$)

The point at which the diode changes from No Bias condition to Forward Bias condition happens when the electron and holes are given sufficient energy to cross the $p$-$n$ junction. This energy comes from the external voltage applied across the diode.

This voltage (can be deduced from the diode characteristics curve) is called the **turn-on voltage** or the **threshold voltage**, and denoted by $V_{D(ON)}$ ($V_T$ or $V_0$ notations are also used).

The forward bias voltage required to turn on the diode for a

- Silicon diode: $V_{D(ON)} = 0.7\,\mathrm{V}$
- Germanium diode: $V_{D(ON)} = 0.3\,\mathrm{V}$

### 1.3.8 Temperature Effects

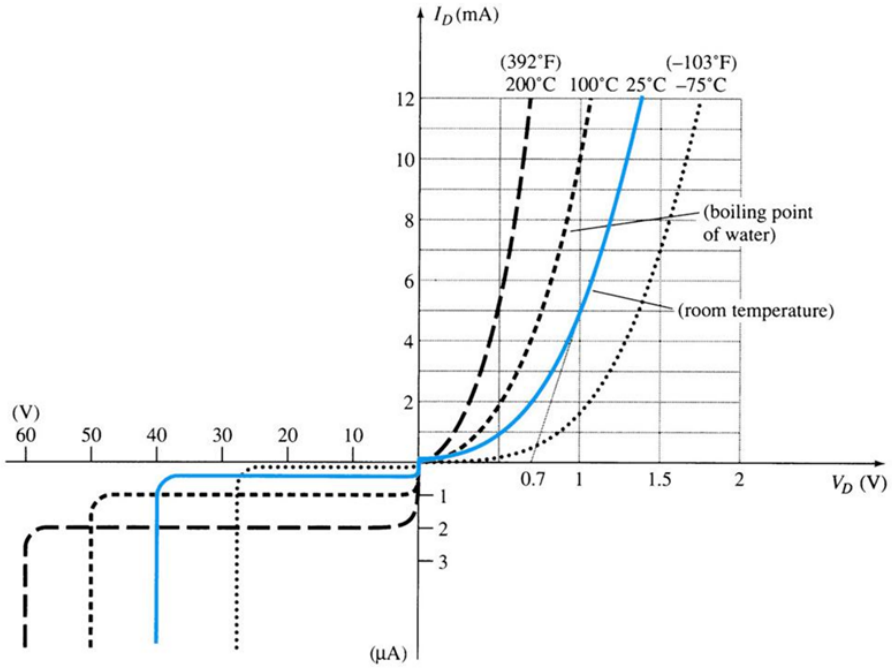
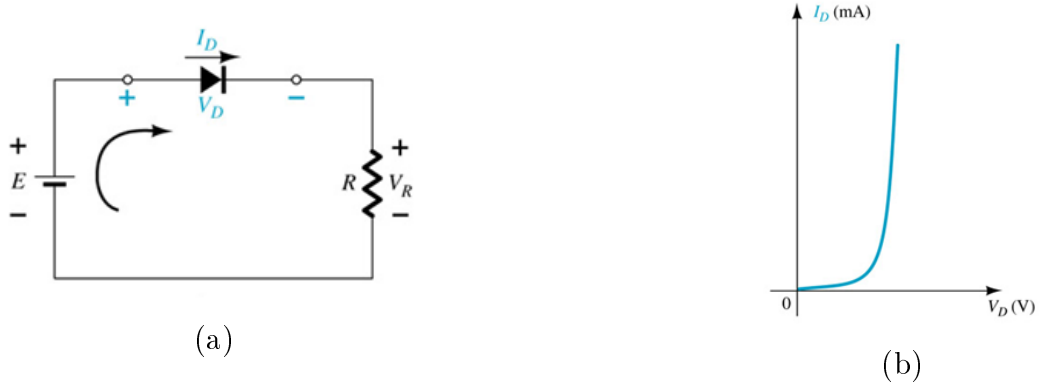



Figure 1.16: Change of diode characteristics with temperature

- As temperature increases it adds energy to the diode. From Figure 1.16 above, as temperature increases
  - It **reduces** the required **turn-on voltage** ($V_{D(ON)}$) in forward bias condition,
  - It **increases** the amount of **reverse saturation current** ($I_s$) in reverse bias condition,
  - It **increases** the **avalanche breakdown voltage** in reverse bias condition.
- Germanium diodes are more sensitive to temperature variations than Silicon diodes.

### 1.3.9 Load Line and Operating Point ($Q$-point)




(a) (b)

Figure 1.17: Series diode configuration: (a) circuit, (b) diode characteristics curve.

From Figure 1.17(a) above, we obtain

$$V_D = E - I_D R \tag{1.3.16}$$

- We can rearrange the circuit equation (1.3.16) above to get $I_D$ on the left-hand side of the equation, i.e.,

$$\boxed{I_D = \frac{-1}{R} V_D + \frac{E}{R}} \tag{1.3.17}$$

- This equation obtained from the diode circuit is called the **load line equation**.

  The **load line** equation gives us all the possible current ($I_D$) values for all the possible voltage ($V_D$) values obtained across the diode in a given circuit.

- Once we draw the load line over the diode characteristics curve given in Figure 1.17(b), and the intersection point will give us the solution $(I_{DQ}, V_{DQ})$ of the diode current and diode voltages $I_D$ and $V_D$ for the given circuit, respectively. The result is shown in Figure 1.18 below.

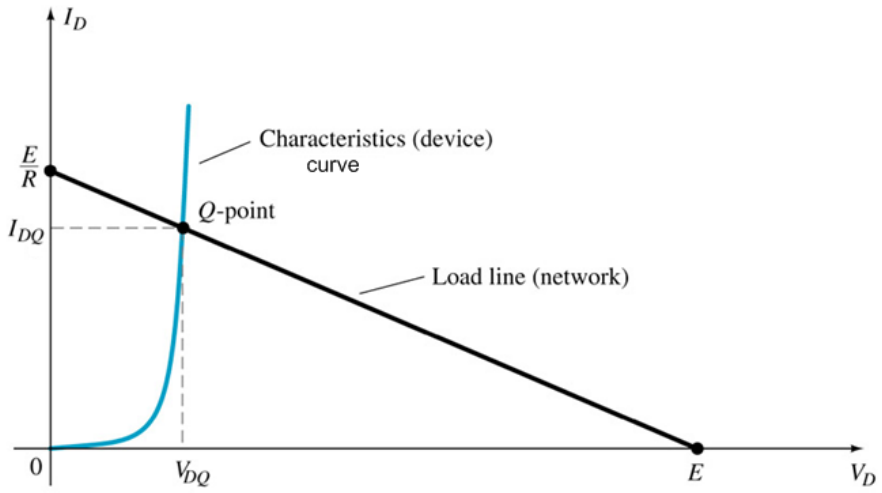



Figure 1.18: Drawing the load line and finding the point of operation.

- This plot is called the **load line plot**. Also, the intersection point of the load line and the diode characteristics curve is called the **operating point** or the ***Q*-point** specified by the $(I_{DQ}, V_{DQ})$ pair. Note that $Q$ stands for quiescent (i.e., still).

- For some examples, see Examples 2.1, 2.2 and 2.3 in the Boylestad and Nashelsky textbook (8th ed.).

A load line plot like Figure 1.18 is actually the graphical way of solving the diode characteristics equation

$$I_D = I_S \left(e^{V_D/\gamma} - 1\right)$$

and the electrical circuit equation, i.e., load line equation

$$I_D = -\frac{V_D}{R} + \frac{E}{R}$$

simultaneously. Load line plots are very practical and more efficient than solving these two equations analytically.

### 1.3.10 DC Resistance (Static Resistance)

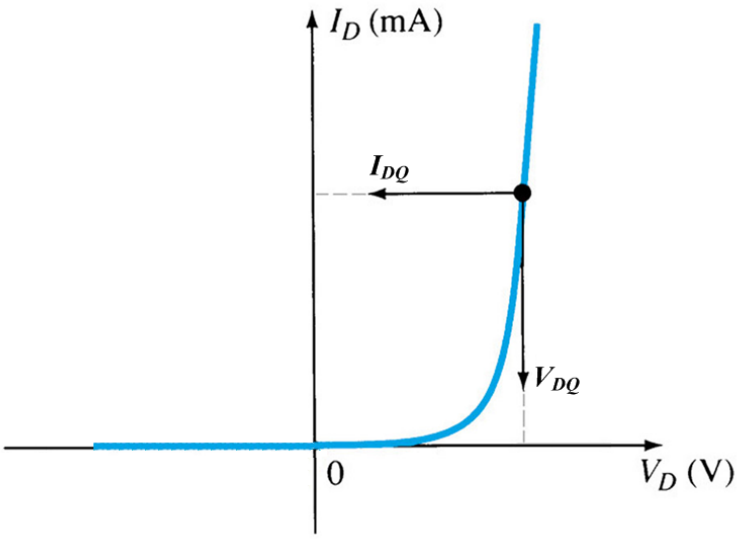



Figure 1.19: Determining the DC resistance of a diode at a particular operating point.

- For a specific applied DC voltage $V_{DQ}$, the diode will have a specific current $I_{DQ}$, and consequently a specific resistance $R_{DQ}$. The amount of resistance $R_{DQ}$, depends on the applied DC voltage and current.

- For a given operating point as shown in Figure 1.19 above, we can find the DC resistance as follows

$$\boxed{\begin{aligned} R_{DQ} &= \left.\frac{V_D}{I_D}\right|_{Q\text{-point}} \\ &= \frac{V_{DQ}}{I_{DQ}} \end{aligned}} \tag{1.3.18}$$

### 1.3.11 AC Resistance (Dynamic Resistance)

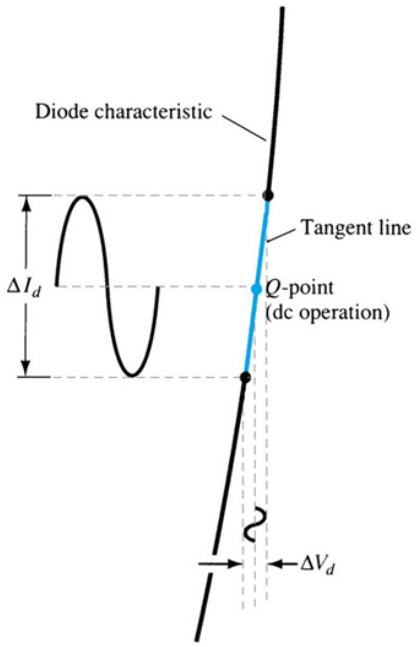



Figure 1.20: Defining the dynamic or AC resistance around an operating point

- Dynamic resistance $r_d$ is determined around a $Q$-point (see Figure 1.20 above) as the ratio of given very small voltage variation $\Delta V_d$ to the current variation $\Delta I_d$ obtained, i.e.,

$$r_d \cong \left.\frac{\Delta V_d}{\Delta I_d}\right|_{Q\text{-point}}.$$

- As the magnitude of these small voltage and current variations go to zero this equation for the dynamic resistance $r_d$ approaches to the following partial derivative

$$\boxed{r_d = \left.\frac{\partial V_D}{\partial I_D}\right|_{Q\text{-point}}} \tag{1.3.19}$$

- In the **forward bias region**, we can use the simplified forward bias diode equation

$$I_D \approx I_s e^{V_D/\gamma}$$

as given in (1.3.11)

Then, the forward bias dynamic resistance is obtained as

$$r_d = \left.\frac{\partial V_D}{\partial I_D}\right|_{Q\text{-point}} = \left.\frac{1}{\frac{\partial I_D}{\partial V_D}}\right|_{Q\text{-point}} \approx \frac{1}{\frac{1}{\gamma}\underbrace{I_s\, e^{V_{DQ}/\gamma}}_{I_{DQ}}}$$

$$= \frac{\gamma}{I_{DQ}}$$

The forward bias dynamic resistance depends on the $Q$-point current $I_{DQ}$ and the temperature, i.e.,

$$\boxed{r_d = \frac{\gamma}{I_{DQ}}} \tag{1.3.20}$$

We know that $\gamma = 26\,\text{mV}$ at room temperature ($300\,\text{K}$), so the diode dynamic resistance can be calculated as

$$r_d = \frac{26\,\text{mV}}{I_{DQ}} \tag{1.3.21}$$

- In the **reverse bias region**, diode current is approximately constant

$$I_D \approx -I_s$$

as given in (1.3.12)

So, the reverse bias dynamic resistance is essentially infinite, i.e.,

$$r_d = \infty. \tag{1.3.22}$$

### 1.3.12 DC and Small-Signal AC (SSAC) Analysis

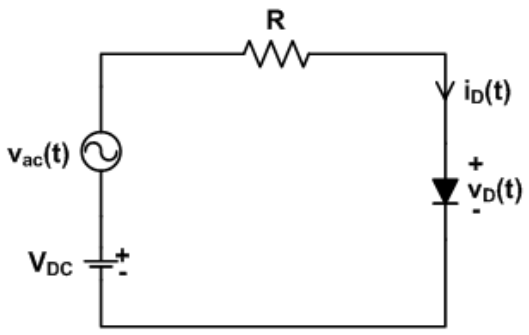



Figure 1.21: Diode circuit with AC and DC sources.

- Here, it is given that $V_{DC} - \text{peak}(v_{ac}(t)) > V_{D(ON)}$ and $V_{DC} >> \text{peak}(v_{ac}(t))$.

  First condition ensures that the diode state do not change for any value of the AC signal (i.e., diode is always ON) and the second condition ensures that diode behaviour is approximately linear around the $Q$-point.

  The two conditions together provide **linearity** (approximately), so that we can employ the **superposition theorem**. Remember that, superposition theorem can only be employed in linear systems.

- Then, we can apply the **superposition theorem** and express the diode current and voltages as follows

$$i_D(t) = I_{DQ} + i_d(t) \tag{1.3.23}$$
$$v_D(t) = V_{DQ} + v_d(t). \tag{1.3.24}$$

- Diode is always ON and magnitude of the AC signal is very small compared to the DC signal (e.g., 10 mV vs. 10 V). So, we can apply the **law of superposition** and perform DC analysis and small-signal AC (SSAC) analysis **separately**, that is, we obtain $I_{DQ}$ and $i_d(t)$ independently using different circuits.

- We obtain **DC equivalent circuit** by killing the AC sources as shown in Figure 1.22 below

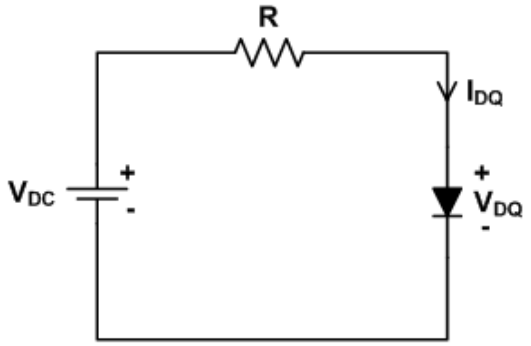



Figure 1.22: DC equivalent circuit of the circuit in Figure 1.21.

In DC analysis, $I_{DQ}$ and $V_{DQ}$ are found using the **load-line analysis**, i.e., by solving the diode characteristic equation and load-line equation simultaneously.

- We obtain **SSAC equivalent circuit** by killing the DC sources and replacing the diode with **its SSAC model ($r_d$)** where

$$r_d = \frac{26\,\text{mV}}{I_{DQ}}$$

as shown in Figure 1.23 below

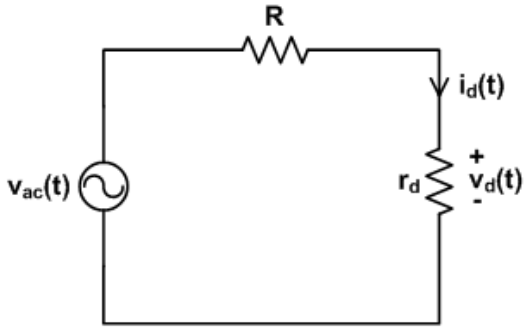



Figure 1.23: SSAC equivalent circuit of the circuit in Figure 1.21.

- In SSAC analysis, diode is replaced by its dynamic resistance $r_d$ and we can finally find $i_d(t)$ and $v_d(t)$ as follows

$$i_d(t) = \frac{v_{ac}(t)}{R + r_d} \tag{1.3.25}$$

$$v_d(t) = \frac{r_d}{R + r_d}\, v_{ac}(t). \tag{1.3.26}$$

### 1.3.13 Average AC Resistance

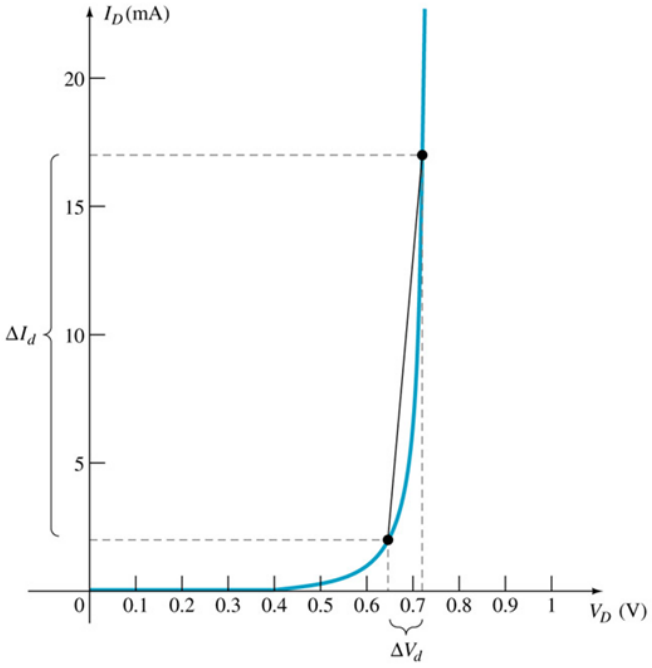



Figure 1.24: Determining the average AC resistance between indicated limits.

- Average AC resistance can be determined by picking two points on the characteristic curve developed for a particular circuit where the voltage and current variations (i.e., $\Delta V_d$ and $\Delta I_d$) are large, as shown in Figure 1.24 above. It is used to develop the piecewise-linear diode model.
- Thus, the average AC resistance $r_{\text{av}}$ is calculated as

$$r_{\text{av}} = \frac{\Delta V_D}{\Delta I_D} \quad \text{(point-to-point)} \tag{1.3.27}$$

## 1.4 Piecewise-Linear Diode Model

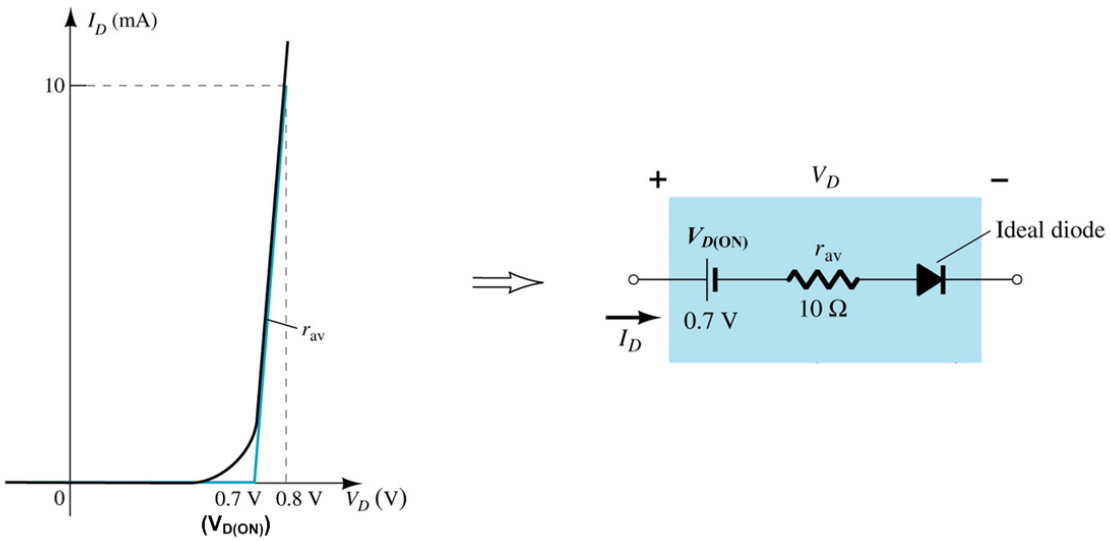



Figure 1.25: Piecewise-linear characteristics curve (blue line on the left) and piecewise-linear equivalent circuit (on the right) of the diode.

- Piecewise-linear approximation of the diode characteristics curve is obtained and depicted as the blue lines on the left of Figure 1.25 above.
- Similarly, obtained piecewise-linear equivalent circuit is shown on the right of Figure 1.25 above.
- Here, $r_{\text{av}}$ is the forward bias average AC resistance (i.e., **internal resistance**) of the diode.

## 1.5 Simplified Diode Model

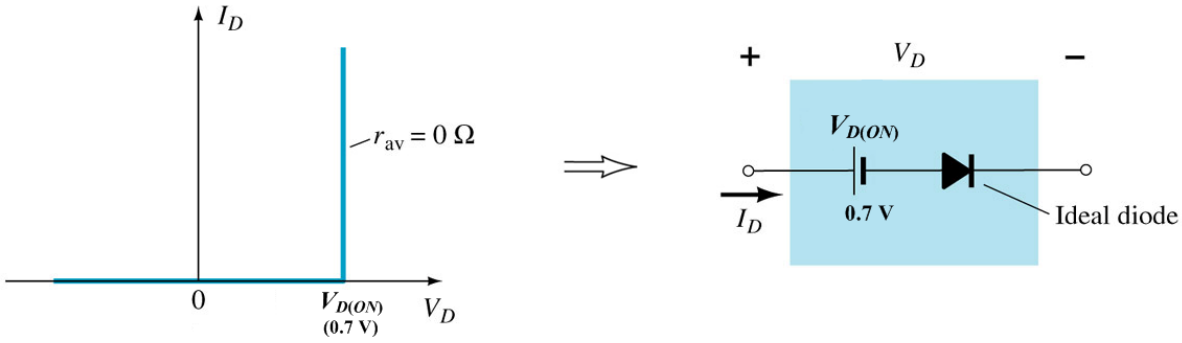



Figure 1.26: Simplified characteristics curve (on the left) and simplified equivalent circuit (on the right) of the diode.

- Simplified diode characteristics curve is obtained and shown on the left of Figure 1.26 above.
- Similarly, obtained simplified equivalent circuit is shown on the right of Figure 1.26 above.

We can summarize the simplified diode model with its state and circuit behaviour with

$$\text{Diode state} = \begin{cases} ON, & \text{if } V_D \geq V_{D(ON)} \\ OFF, & \text{if } V_D < V_{D(ON)} \end{cases} \tag{1.5.28}$$

and

| **Simplified Diode Model** | | |
|---|---|---|
| **State** | **Circuit Behaviour** | **Test Condition** |
| ON | $V_D = V_{D(ON)}$ | $I_D \geq 0$ |
| OFF | $I_D = 0$ | $V_D < V_{D(ON)}$ |

- For the ideal diode model, the turn-on voltage is zero, i.e., $V_{D(ON)} = 0\,\text{V}$.

**In this course, we will mostly use the simplified diode model unless otherwise stated.**

### 1.5.1 Determining State of a Diode

- Using circuit behaviour and the test condition for the OFF state, let us devise a method to determine the state of a diode under simplified diode model.

**Determining State of a Diode**

1. Obtain the expression for $V_D$ in terms of the diode current $I_D$ from the electronic circuit.
2. Insert $I_D = 0$ in to this expression
3. Then, the diode state is given by

$$\text{Ideal diode state} = \begin{cases} ON, & \text{if } V_D|_{I_D=0} \geq V_{D(ON)} \\ OFF, & \text{if } V_D|_{I_D=0} < V_{D(ON)} \end{cases} \tag{1.5.29}$$

**Example 1.2:** Consider the circuit below and find $I_D$ and $V_D$ with $V_{D(ON)} = 0.7\,\text{V}$ and $E > 0.7\,\text{V}$.

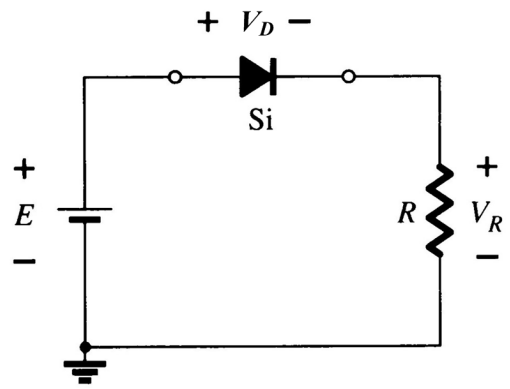



Figure 1.27: Diode circuit for Example 1.2.

**Solution:** First we need to determine the state of the diode (i.e., ON or OFF). So, let us write down the KVL equation and obtain $V_D$

$$V_D = E - I_D\, R$$

From the equation above, $V_D|_{I_D=0} = E \geq V_{D(ON)}$. So, the diode is ON. Thus,

$$\begin{aligned} V_D &= V_{D(ON)} = 0.7\,\text{V} && \ldots \text{from circuit behaviour} \\ I_D &= \frac{E - V_D}{R} = \frac{E - 0.7}{R} \\ V_R &= E - V_D = E - 0.7 \end{aligned}$$

Thus, our diode circuitin Figure 1.27 is simplified to the circuit shown in Figure 1.28 below

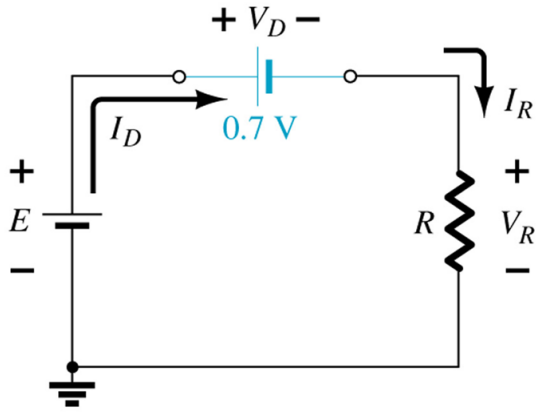



Figure 1.28: Simplified circuit for the diode circuit in Figure 1.27.

Note that $I_R = I_D$.

**Example 1.3:** Consider the circuit below and find $I_D$ and $V_D$ with $V_{D(ON)} = 0.7\,\text{V}$ and $E > 0.7\,\text{V}$.

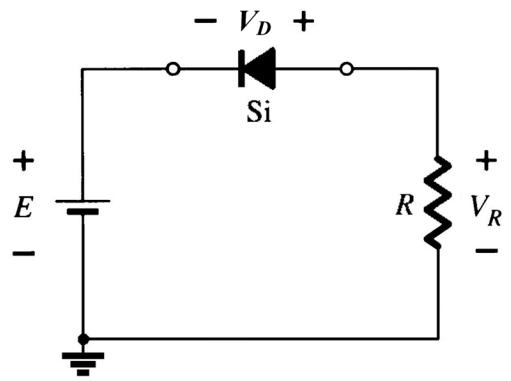



Figure 1.29: Diode circuit for Example 1.3.

**Solution:** First we need to determine the state of the diode (i.e., ON or OFF). So, let us write down the KVL equation and obtain $V_D$

$$V_D = -E - I_D\,R$$

From the equation above, $V_D|_{I_D=0} = -E < V_{D(ON)}$. So, the diode is OFF. Thus,

$$\begin{aligned} I_D &= 0\,\text{A} && \ldots\text{from circuit behaviour} \\ V_D &= -E - I_D\,R = -E \\ V_R &= -I_D R = 0\,\text{V} \end{aligned}$$

Thus, our diode circuitin Figure 1.29 is simplified to the circuit shown in Figure 1.30 below

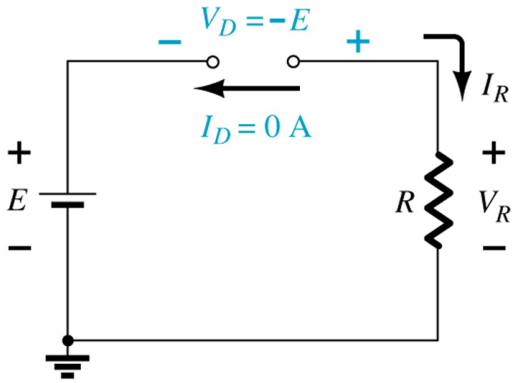



Figure 1.30: Simplified circuit for the diode circuit in Figure 1.29.

Note that $I_R = -I_D = 0\,\text{A}$.

**Example 1.4:** Consider the circuit below and find $I_1$, $V_o$, $I_{D_1}$ and $I_{D_2}$ with $V_{D(ON)} = 0.7\,\text{V}$ and $D_1 \equiv D_2$.

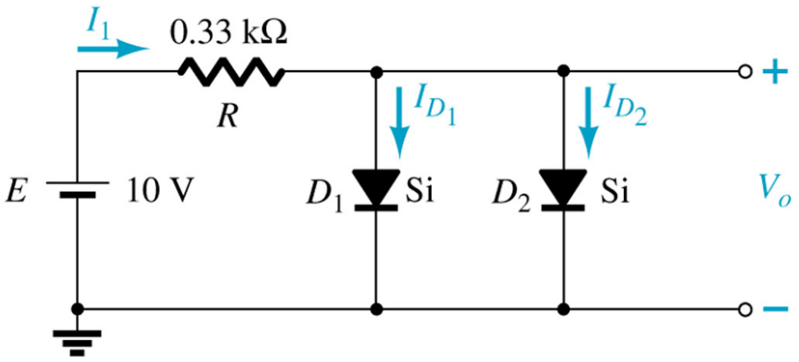



Figure 1.31: Diode circuit for Example 1.4.

**Solution:** First we need to determine the state of the diodes (i.e., ON or OFF). As the diodes are parallel, we let us make the following definitions

$$V_D = V_{D_1} = V_{D_2}$$
$$I_D = I_{D_1} + I_{D_2} = I_1$$

So, let us write down the KVL equation and obtain $V_D$

$$V_D = E - I_D\,R = 10 - 0.33k\,I_D$$

From the equation above, $V_D|_{I_D=0} = 10 \geq V_{D(ON)}$. So, both diodes are ON.

Thus,

$$V_{D_1} = V_{D(ON)} = 0.7\,\text{V} \qquad \ldots\text{from circuit behaviour}$$
$$V_{D_2} = V_{D(ON)} = 0.7\,\text{V} \qquad \ldots\text{from circuit behaviour}$$
$$V_o = V_D = 0.7\,\text{V}$$
$$I_1 = \frac{E - V_D}{R} = \frac{10 - 0.7}{0.33k} = 28.18\,\text{mA}$$
$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = 14.09\,\text{mA} \qquad \ldots\text{as } D_1 \equiv D_2$$

**Homework 1.1:** What will happen if $D_2$ is replaced by a Germanium diode and $D_1$ remains as a Silicon diode?

## 1.6 Diode Specification Sheets

Data about a diode is presented uniformly for many different diodes. This makes cross-matching of diodes for replacement or design easier.
Some of the key elements is listed below:

1. $V_F$: forward voltage at a specific current and temperature
2. $I_F$: maximum forward current at a specific temperature

3. $I_R$: maximum reverse current at a specific temperature
4. PIV or PRV or VBR: maximum reverse voltage at a specific temperature
5. Power Dissipation: maximum power dissipated at a specific temperature
6. $C$: Capacitance levels in reverse bias
7. $t_{rr}$: reverse recovery time
8. Temperatures: operating and storage temperature ranges

### 1.6.1 Semiconductor Notation

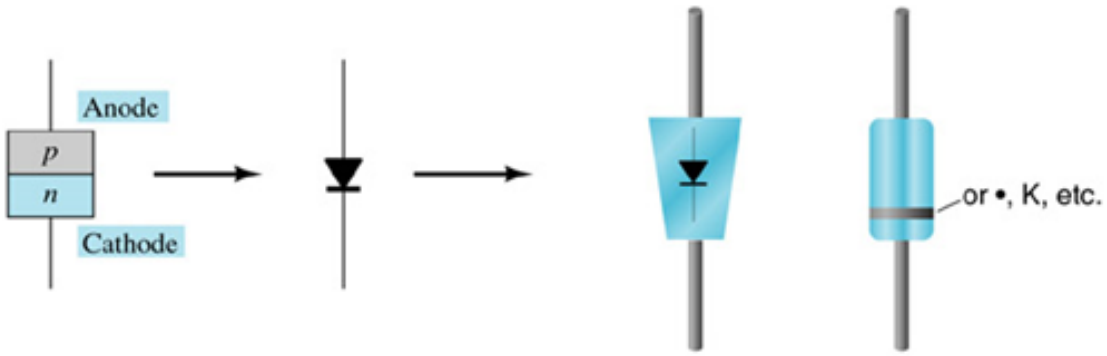



Figure 1.32: Semiconductor diode notation.

- Anode is abbreviated as A.
- Cathode is abbreviated as K (because the Cathode end of the diode symbol looks like a backwards K).

Examples of some diode types and packagings are shown in Figure 1.33 below.

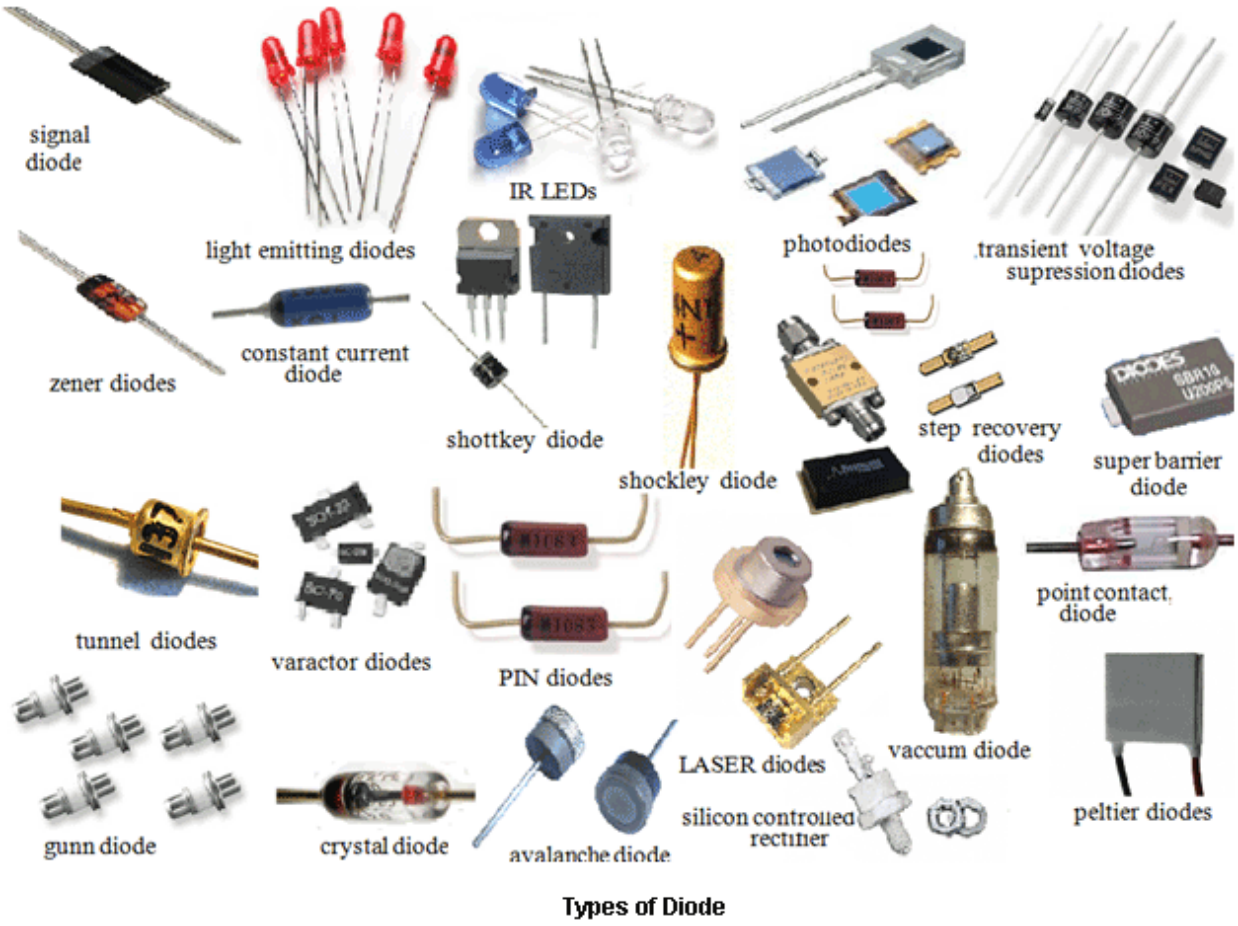



Figure 1.33: Some diode types and packagings.

### 1.6.2 Capacitance

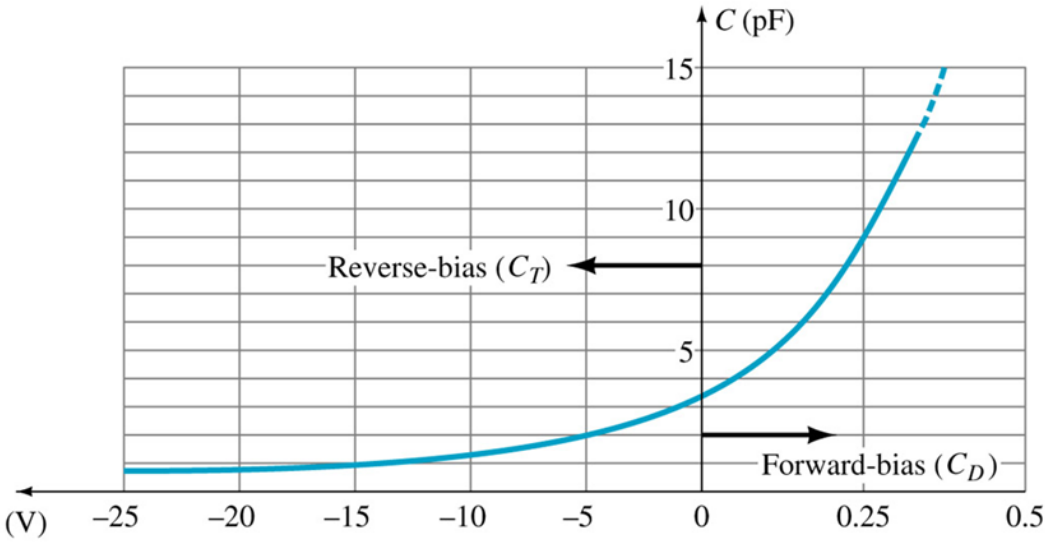



Figure 1.34: Transition and diffusion capacitance versus applied bias for a Silicon diode.

- In **reverse bias**, the depletion layer is very large. The diode's strong positive and negative polarities create capacitance, $C_T$. The amount of capacitance depends on the reverse voltage applied.
- In **forward bias**, storage capacitance or diffusion capacitance ($C_D$) exists as the diode voltage increases

## 1.7 Other Types of Diodes

Other types of diodes we like to mention are listed below

1. Zener Diode
2. Light Emitting Diode

## 1.8 Zener Diode

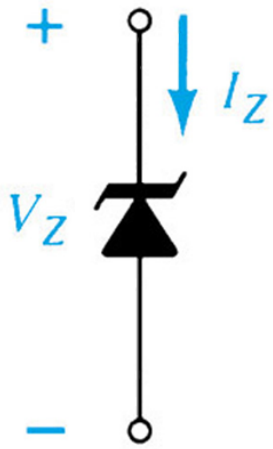



Figure 1.35: Zener diode symbol.

- A Zener is a diode operated in reverse bias at the Peak Inverse Voltage (PIV) called the **Zener voltage** ($V_Z$).
- Common Zener voltages: 1.8 V to 200 V.
- We are going to cover Zener diodes in more detail later in the course.

## 1.9 Light Emitting Diode (LED)

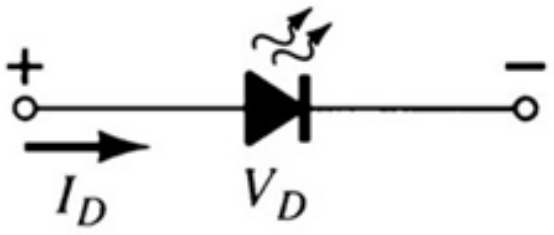



Figure 1.36: Circuit symbol of an LED.

- This diode when forward biased emits photons. These can be in the visible spectrum.
- The forward bias turn-on voltage is higher, usually around 2-3 V.
- A Litronix 7-segment LED display is shown in Figure 1.37 below

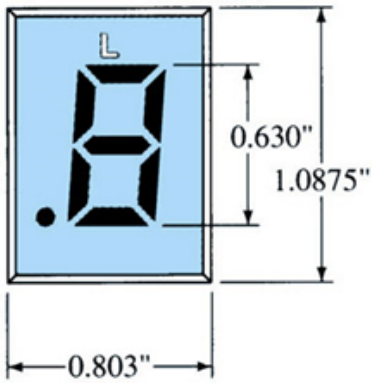



Figure 1.37: Litronix 7-segment LED display

- Relative intensity of each color versus wavelength appears in Figure 1.38 below.

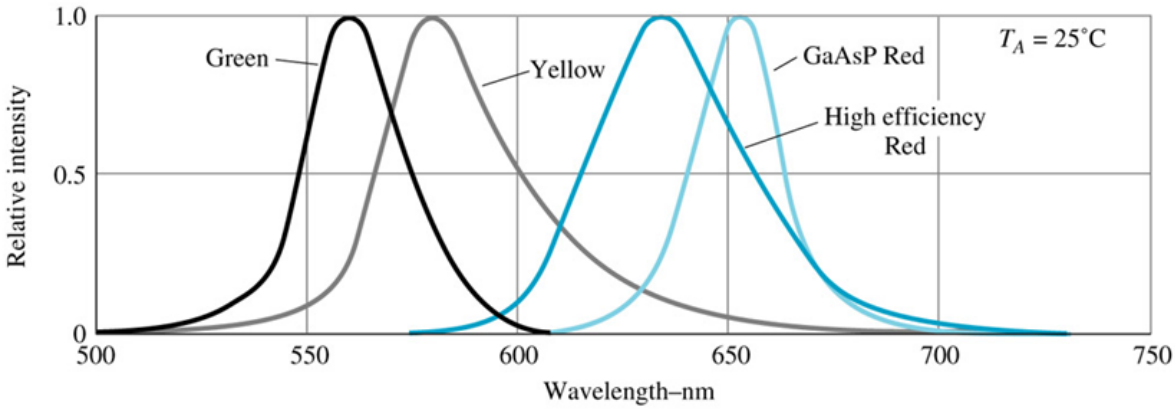



Figure 1.38: Relative intensity versus wavelength.

# Chapter 2

# Diode Applications

## 2.1 Clippers

Clipper diode circuits have the ability to *clip* off a portion of the input signal without distorting the remaining part of the alternating waveform.

Depending on the orientation of the diode, the positive or negative region of the input signal is *clipped* off.

There are two general categories of clippers: **series** and **parallel**. The series configuration is defined as one where the diode is in series with the load as shown in Figure 2.1 below, while the parallel variety has the diode in a branch parallel to the load.

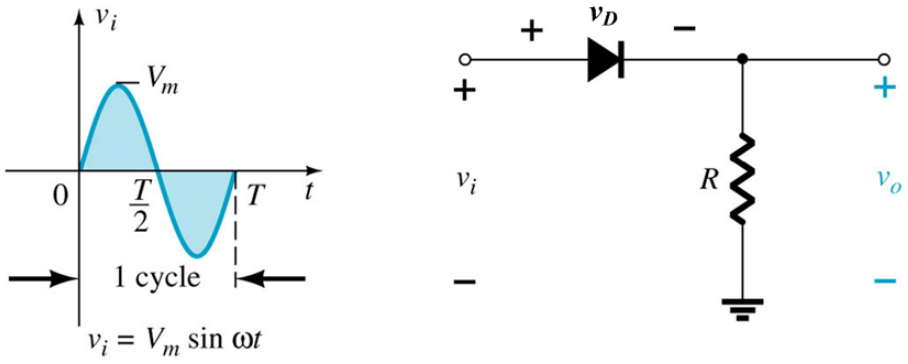



Figure 2.1: A series clipper circuit.

- Let us write down the KVL equation for the circuit in Figure 2.1 above

$$v_i - v_D - i_D R = 0 \quad \Rightarrow \quad v_D = v_i - i_D R \tag{2.1.1}$$

As $v_D|_{i_D=0} = v_i$, we have

$$\text{Diode state} = \begin{cases} ON, & \text{if } v_i \geq V_{D(ON)} \\ OFF, & \text{if } v_i < V_{D(ON)} \end{cases} \tag{2.1.2}$$

As the **output** $v_o$ is across the resistor $R$, i.e., $v_o = i_D R = v_i - v_D$, we have

$$\boxed{v_o = \begin{cases} v_i - V_{D(ON)}, & \text{if } v_i \geq V_{D(ON)} \\ 0, & \text{if } v_i < V_{D(ON)} \end{cases}} \tag{2.1.3}$$

- Let us plot equation (2.1.3) above, as a **voltage transfer characteristics** (VTC) curve, i.e., output versus input plot, in order to understand the clipper behaviour visually, as shown in Figure 2.2 below.

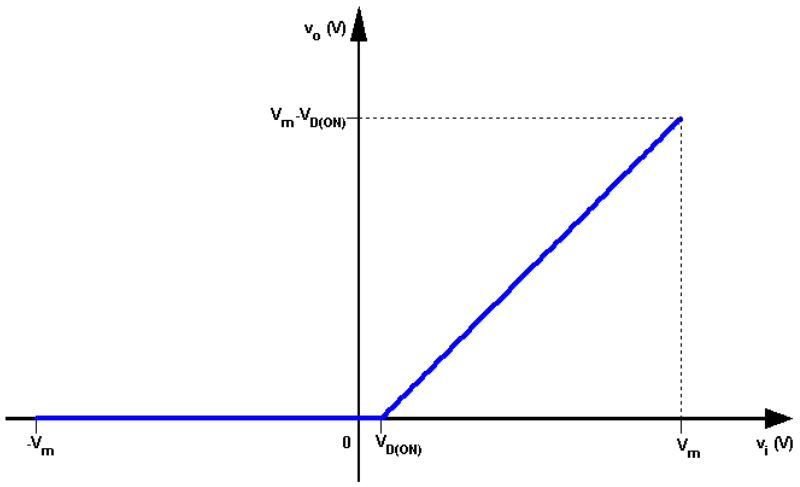



Figure 2.2: Voltage transfer characteristics (VTC) curve of the series clipper circuit Figure 2.1.

- Let us analyse the operation of the series clipper circuit Figure 2.1 for a sinusoidal input, using the **ideal diode** model, i.e., $V_{D(ON)} = 0$.

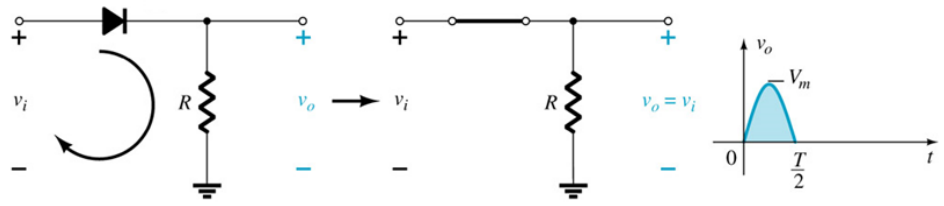



Figure 2.3: Positive half-cycle operation of the series clipper circuit in Figure 2.1.

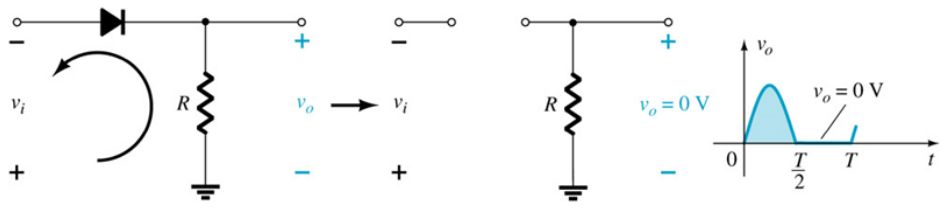



Figure 2.4: Negative half-cycle operation of the series clipper circuit in Figure 2.1.

As we see from Figure 2.3 and Figure 2.4 above, negative half-cycle portion of the signal is clipped off while the positive half-cycle portion remains intact.

**Example 2.1:** By adding a DC source to the circuit as shown in Figure 2.5, the voltage required to forward bias the diode can be changed.

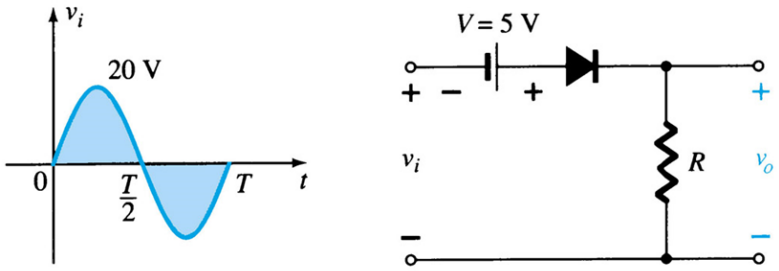



Figure 2.5: A series clipper circuit with a DC supply.

Consequently, the output will be given by

$$v_o = \begin{cases} v_i + 5\,\text{V} - V_{D(ON)}, & \text{if } v_i \geq V_{D(ON)} - 5\,\text{V} \\ 0, & \text{if } v_i < V_{D(ON)} - 5\,\text{V} \end{cases} \tag{2.1.4}$$

Let us sketch the output of the series clipper circuit Figure 2.5 for a sinusoidal input, using the **ideal diode** model, as shown in Figure 2.6 below.

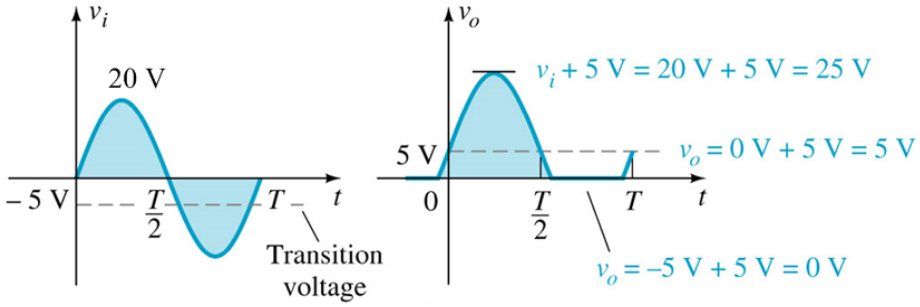



Figure 2.6: Input and output of the series clipper circuit in Figure 2.5.

**Example 2.2:** Various series clipper examples are shown in Figure 2.7 below (diodes are ideal).

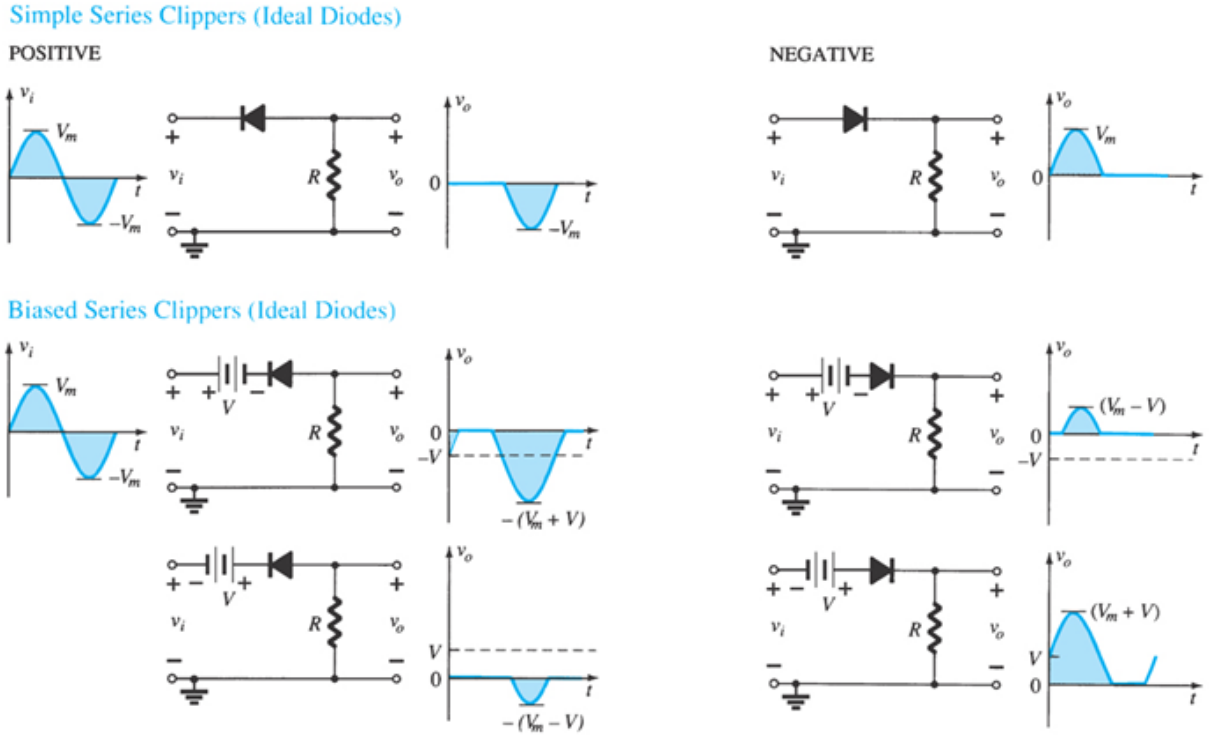



Figure 2.7: Various series clipper examples (diodes are ideal).

### 2.1.1 Parallel Clippers

By taking the output across the diode shown in Figure 2.8 below, the output equals to the input voltage when the diode is not conducting.

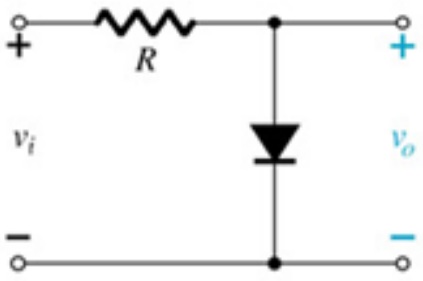



Figure 2.8: A parallel clipper circuit.

Hence, the output for this circuit will be given by

$$\boxed{v_o = \begin{cases} V_{D(ON)}, & \text{if } v_i \geq V_{D(ON)} \\ v_i, & \text{if } v_i < V_{D(ON)} \end{cases}} \tag{2.1.5}$$

Example input and output waveforms of the parallel clipper circuit Figure 2.8 for the **ideal diode** model are shown in Figure 2.9 below.

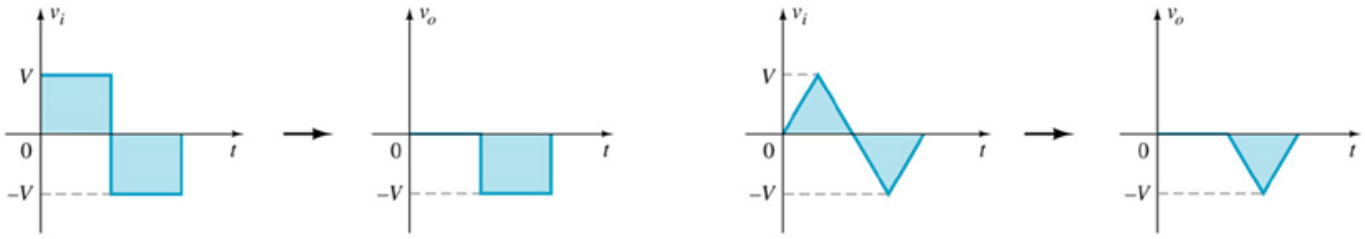



Figure 2.9: Sample input and output waveforms of the parallel clipper circuit in Figure 2.8.

**Example 2.3:** A DC source can also be added to change the diode's required forward bias voltage, as shown in Figure 2.10

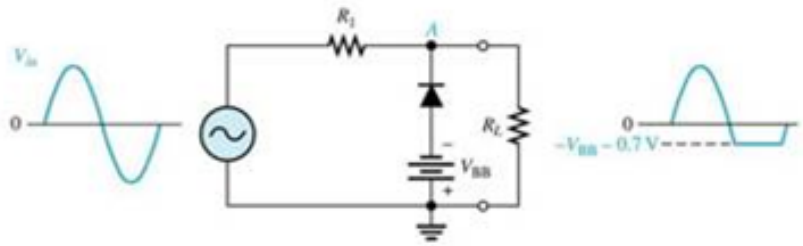



Figure 2.10: A parallel clipper circuit with a DC supply.

Consequently, the output will be given by

$$v_o = \begin{cases} -V_{D(ON)} - V_{BB}, & \text{if } v_i \leq -V_{D(ON)} - V_{BB} \\ v_i, & \text{if } v_i > -V_{D(ON)} - V_{BB} \end{cases} \tag{2.1.6}$$

**Homework 2.1:** Draw the VTC diagram of the parallel clipper circuit given in Figure 2.10 above.

**Homework 2.2:** Draw the output waveform and the VTC diagram when the diode is reversed.

**Example 2.4:** For the circuit shown in Figure 2.11 below, find the output for a sinusoidal input $v_i(t) = V_m \sin(2\pi t/T)$ where $(V_{B1}, V_{B2}) < V_m$ and draw the VTC diagram.

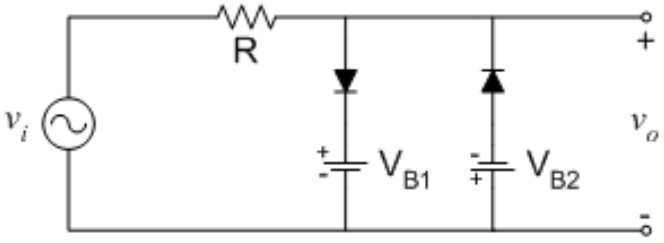



Figure 2.11: A diode limiter circuit.

Consequently, the output is given below and also shown in Figures 2.12(a) and 2.12(b) below

$$v_o = \begin{cases} V_{D(ON)} + V_{B1}, & \text{if } v_i \geq V_{D(ON)} + V_{B1}, \\ -V_{D(ON)} - V_{B2}, & \text{if } v_i \leq -V_{D(ON)} - V_{B2}, \\ v_i, & \text{else.} \end{cases} \tag{2.1.7}$$

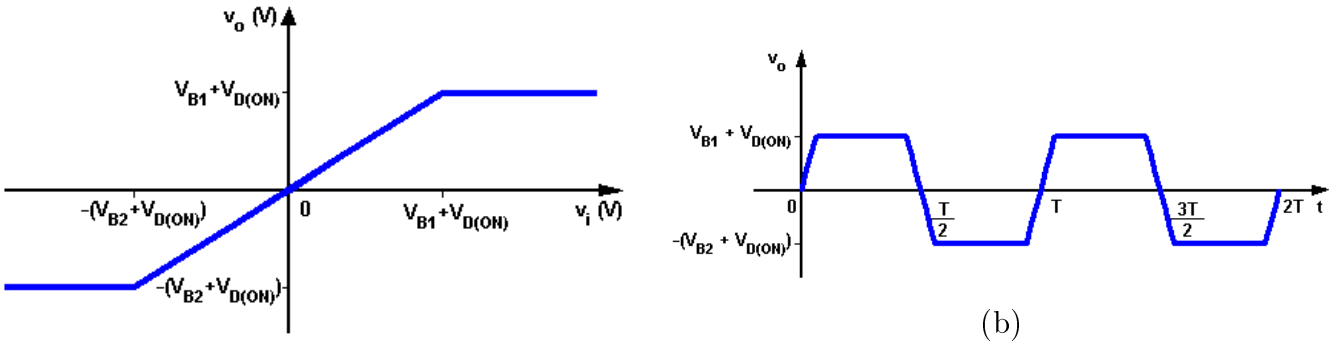



Figure 2.12: Outputs of the circuit in Figure 2.11: (a) VTC diagram, (b) output waveform.

**Example 2.5:** Various parallel clipper examples are shown in Figure 2.13 below (diodes are ideal).

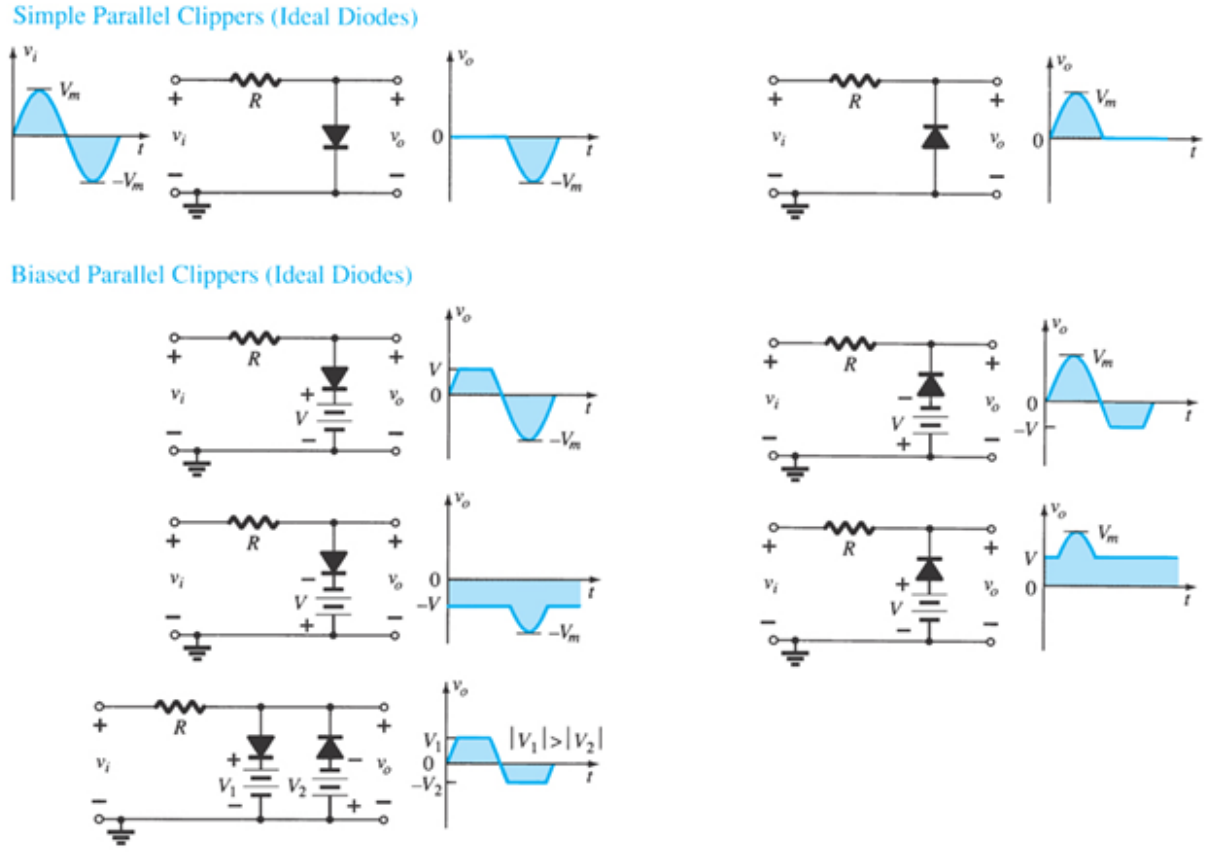



Figure 2.13: Various parallel clipper examples (diodes are ideal).

## 2.2 Clampers

Clamper circuits *clamp* a signal to different DC levels. The circuit must have a capacitor, a diode, and a resistive element as shown in Figure 2.14 below, but it can also employ an independent DC supply to introduce an additional shift.

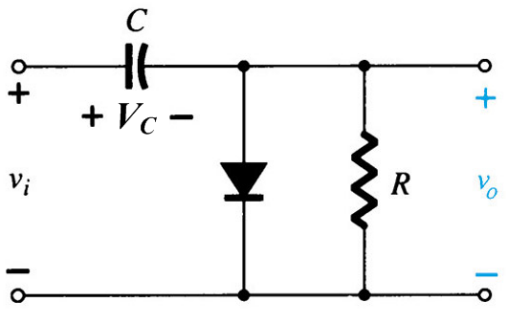



Figure 2.14: A clamper circuit.

Throughout the analysis, we will assume that for all practical purposes the **capacitor** will **fully discharge** in **five time constants**, i.e., $5\tau_{\text{discharge}}$, where time constant $\tau_{\text{discharge}} = RC$.

The magnitude of $R$ and $C$ must be chosen such that the **time constant** $\tau_{\text{discharge}} = RC$ is **large enough** to ensure that the voltage across the **capacitor does not discharge** significantly during the interval the **diode** is **nonconducting**.

For the circuit in Figure 2.14 above, the diode state is given by

$$\text{Diode state} = \begin{cases} ON, & \text{if } v_i \geq V_{D(ON)} + V_C \\ OFF, & \text{if } v_i < V_{D(ON)} + V_C \end{cases} \tag{2.2.8}$$

where $V_C$ is the voltage across the capacitor $C$.

The clamper output is given by

$$v_o = v_i - V_C. \tag{2.2.9}$$

- Consequently, when the capacitor is charged at the maximum voltage, i.e., $V_C = V_m - V_{D(ON)}$ and diode is OFF, the clamper output will be

$$v_o = v_i - (V_m - V_D(ON)). \tag{2.2.10}$$

**IMPORTANT**: The clamper **shifts** the signal **in the direction of the diode arrowhead** by an amount of $(V_m - V_{D(ON)})$.

- Let us generate steps for the clamper operation for the circuit in Figure 2.14 above, assuming capacitor is fully discharged initially, i.e., at $t = 0$, using the **ideal diode** model.

  1. The diode will be ON in the **first** positive half cycle as $V_C = 0$ and the capacitor will charge up very quickly to the peak value $V_m$ with a time constant $\tau_{charge} = Cr_{av} \cong 0$ where $r_{av} \cong 0\,\Omega$ is the internal resistance of the diode as shown in Figure 2.15 below.

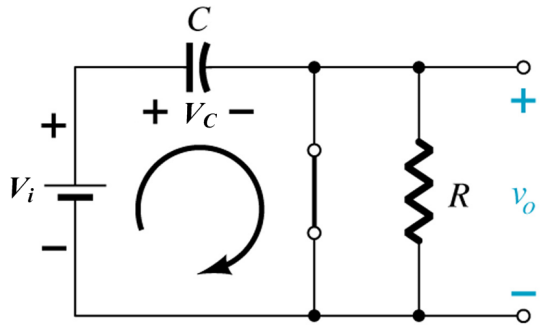



Figure 2.15: Charging operation of the clamper circuit in Figure 2.14.

2. Once the capacitor is charged, i.e., $V_C = V_m$. then the diode turns OFF, as shown in Figure 2.16 below.

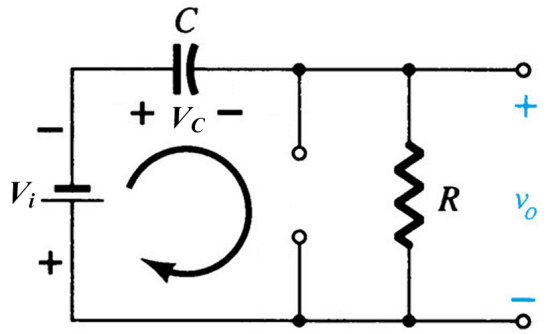



Figure 2.16: Discharging operation of the clamper circuit in Figure 2.14.

3. Capacitor will discharge until the input waveform gets larger than the capacitor voltage, i.e., $v_i(t) > v_C(t)$. Thus, the discharging period $(\frac{T}{2})$ must be much smaller than the fully discharge constant $5\tau_{\text{discharge}}$ in order to keep the voltage across the capacitor almost constant at $V_C \cong V_m$, i.e.,

$$5\tau_{\text{discharge}} \gg \frac{T}{2} \tag{2.2.11}$$

So, if take $\left(5\tau_{\text{discharge}} \geq 50\,\frac{T}{2}\right)$, then we obtain the following condition for the clamping operation

$$\boxed{\tau_{\text{discharge}} \geq 5T} \tag{2.2.12}$$

where $T$ is the period of the input signal $v_i$.

- **For a clamping operation, selected capacitor $C$ and resistor $R$ values should satisfy the discharge condition in** (2.2.12)**.**
- **IMPORTANT:** If it is not explicitly stated we are going to assume that **capacitor** is **already charged**, e.g., $V_C = V_m - V_{D(ON)}$.

**Example 2.6:** Consider the clamping circuit below and plot the output waveform. Assume the diode is **ideal**.

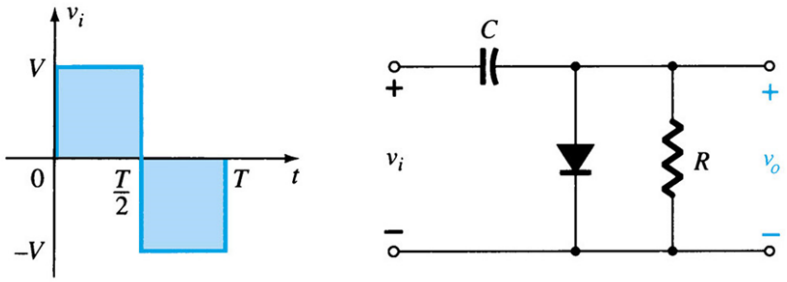



Figure 2.17: A clamper circuit with a square wave input.

**Solution:** As this is a clamping circuit, i.e., $\tau_{\text{discharge}} \leq 5T$, we obtain the following output

$$v_o = v_i - V + V_{D(ON)}$$

where $V_{D(ON)} = 0\,\text{V}$. The resulting waveform is shown in Figure 2.18 below.

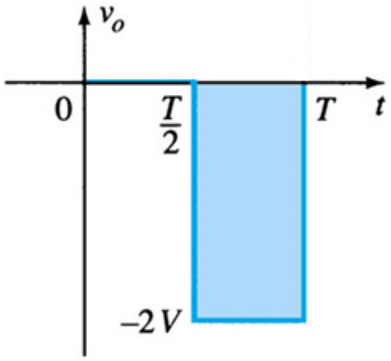



Figure 2.18: Output of the circuit given in Figure 2.17.

**Example 2.7:** Consider the clamping circuit below and plot the output waveform. Assume the diode is **ideal**.

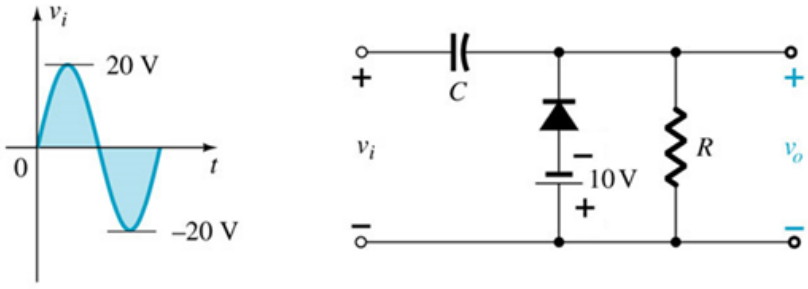



Figure 2.19: A clamper circuit with a sinusoidal input.

**Solution:** Assuming the capacitor is already charged at $V_C = -V_m + V_{D(ON)} + V_{BB} = -20 + 0 + 10 = -10\,\text{V}$, we obtain the following output

$$\begin{aligned} v_o &= v_i - (-V_m + V_{D(ON)} + V_{BB}) = v_i + V_m - V_{D(ON)} - V_{BB} = v_i + 20 - 0 - 10 \\ &= v_i + 10\,\text{V}. \end{aligned}$$

The resulting waveform is shown in Figure 2.20 below.

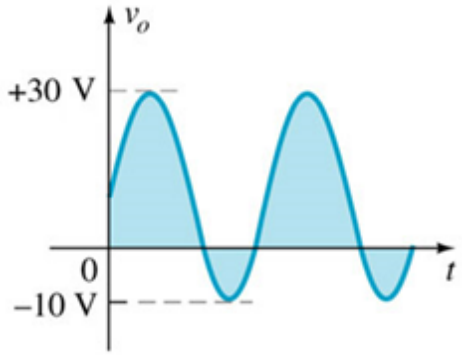



Figure 2.20: Output of the circuit given in Figure 2.19.

**Example 2.8:** Various clamper examples are shown in Figure 2.21 below (diodes are ideal).

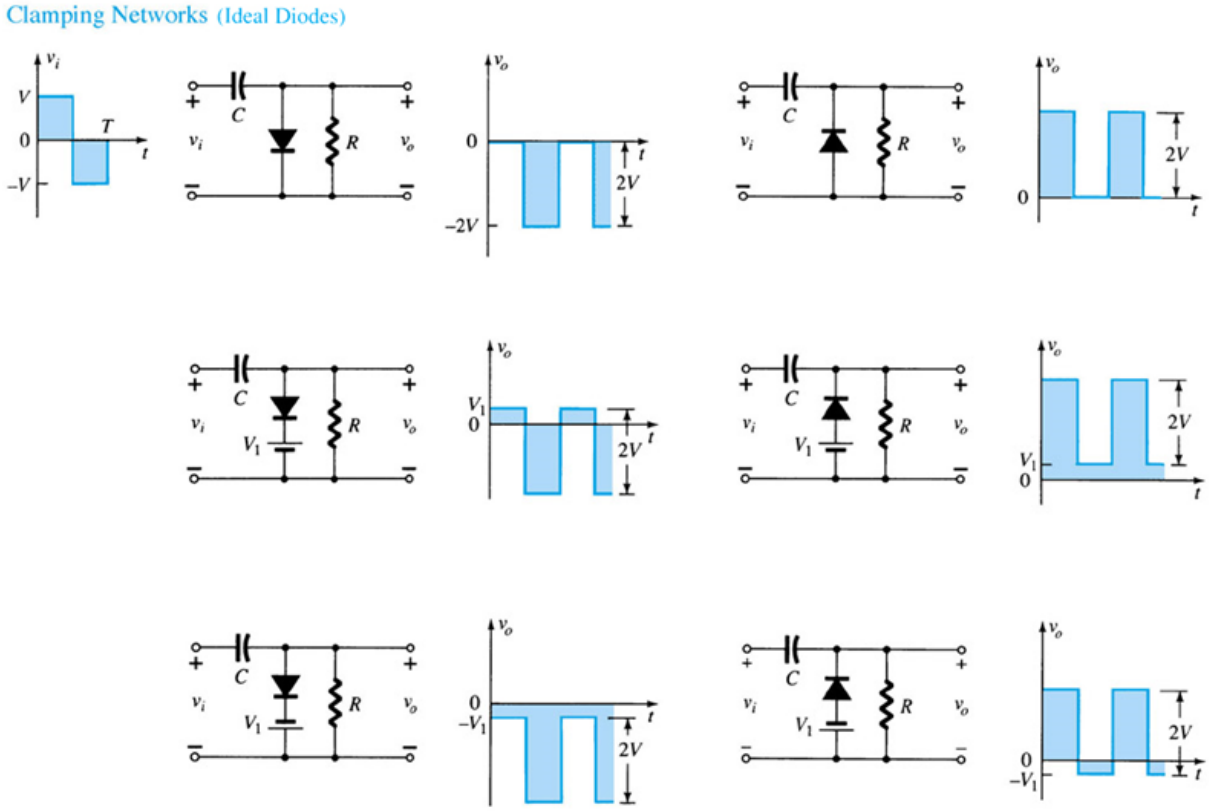



Figure 2.21: Various clamper examples (diodes are ideal and capacitors are charged).

## 2.3 Voltage Multiplier Circuits

### 2.3.1 Peak Rectifier

Once we consider a clamper circuit and take the output over the capacitor instead of the diode, we obtain the **peak rectifier** circuit shown in Figure 2.22 below producing a DC output at peak value of the input signal.

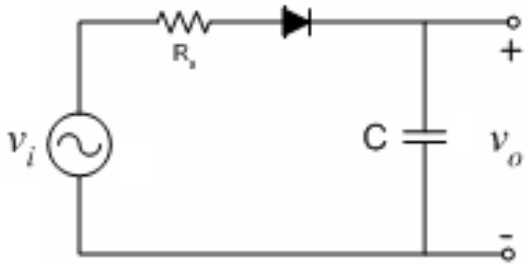
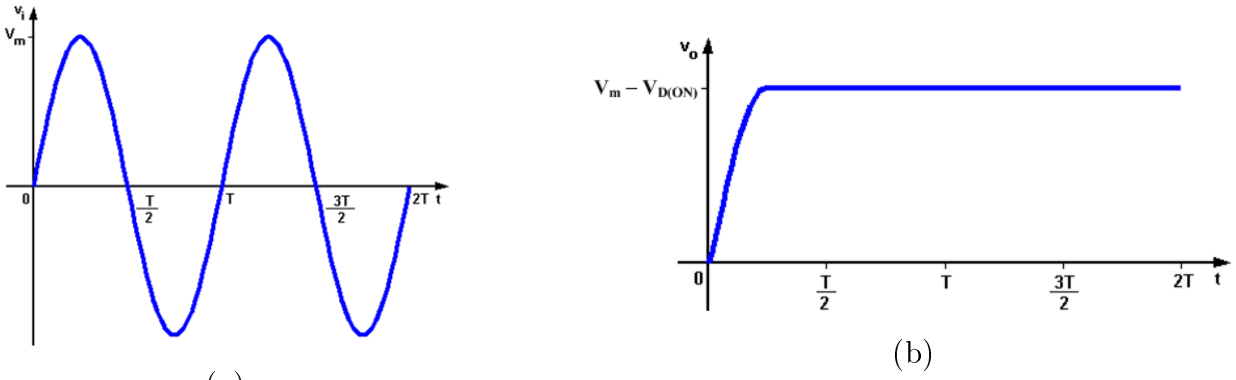



Figure 2.22: A peak rectifier circuit.

Corresponding input and output are also shown in figures 2.23(a) and 2.23(b) below. The capacitor is charged to the maximum value $\left(V_m - V_{D(ON)}\right)$ in the first positive half cycle (i.e., between 0 and $T/4$), then the diode turns OFF and capacitor cannot discharge retaining the charged value. This value is equal to the **peak value** $V_m$ for the **ideal diode**.




(a) (b)

Figure 2.23: For the circuit in Figure 2.22: (a) input waveform, (b) output waveform.

- When a load $R_L$ is connected, the discharge constant $\tau_{discharge} = R_L C$ should have a very high value compared to the half period $\left(\frac{T}{2}\right)$ of the signal, otherwise ripples are observed at the output voltage, i.e., $R_L$ should have a very large value.
- Using a combination of diodes and capacitors we can step up the output voltage of rectifier circuits. These circuits (some listed below) are called **voltage multiplier circuits**.
  1. Voltage Doubler
  2. Voltage Tripler
  3. Voltage Quadrupler

### 2.3.2 Voltage Doubler

A voltage doubler circuit is shown in Figure 2.24 below.

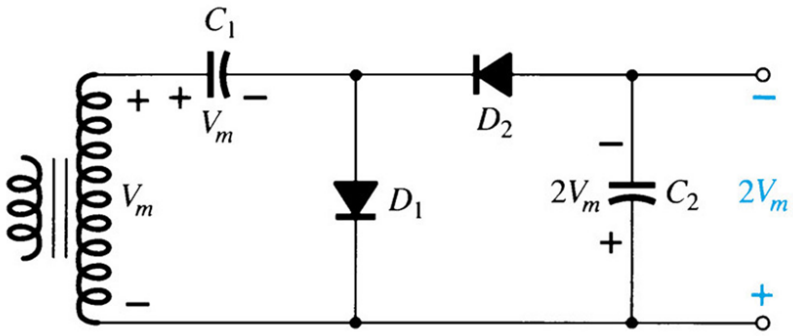
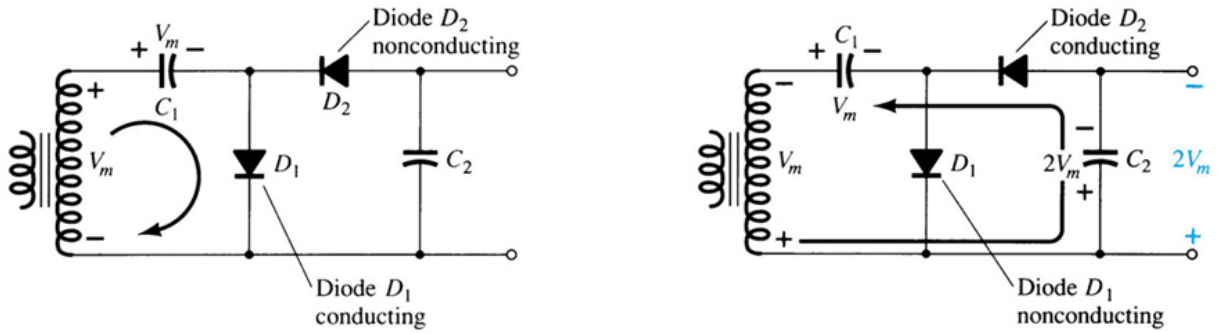



Figure 2.24: Voltage doubler circuit.

Using the **ideal diode** model, operation of the voltage doubler circuit are shown for the first positive and negative half-cycles in figures 2.25(a) and 2.25(b) below, respectively. After the first cycle, both diodes retain their OFF state.




(a) (b)

Figure 2.25: Operation of the circuit in Figure 2.24 at (a) first positive half-cycle, and (b) first negative half-cycle.

### 2.3.3 Voltage Tripler and Quadrupler

By adding more diode-capacitor networks the voltage can be increased as shown in Figure 2.26 below.

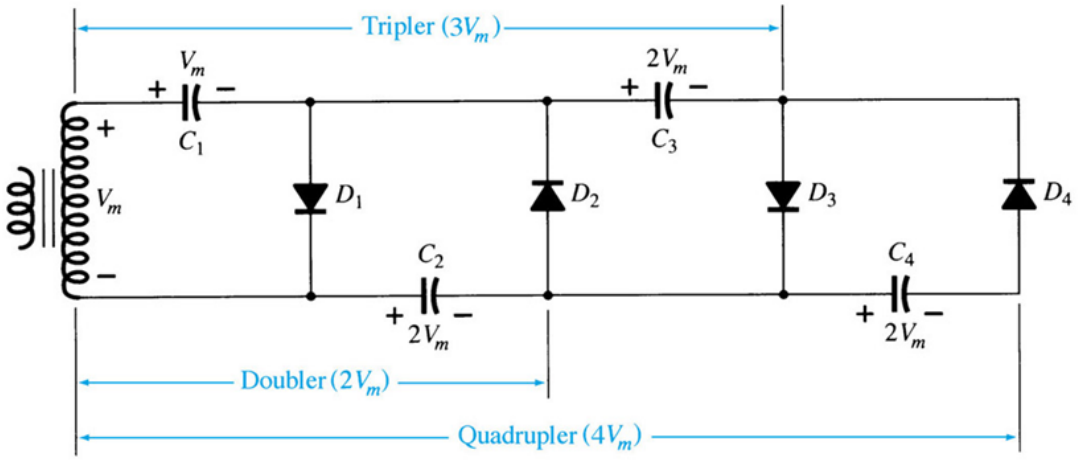
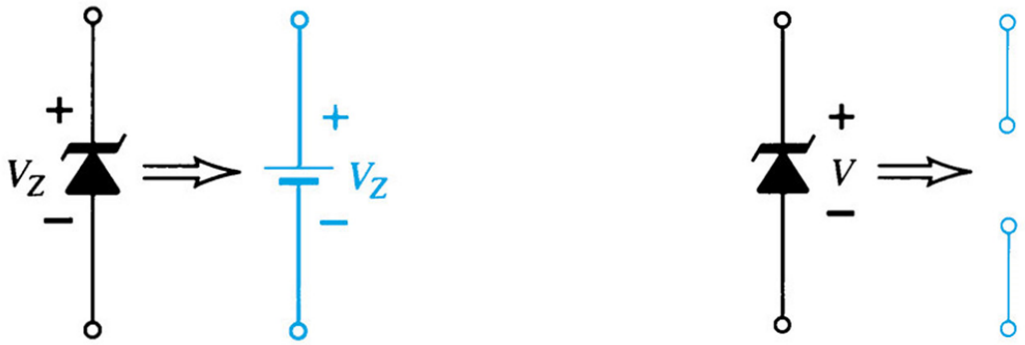



Figure 2.26: Voltage tripler/quadrupler circuit.

## 2.4 Zener Diode

Zener diode **operates** in **reverse bias** (RB) at the Zener Voltage ($V_Z$). Zener diode is ON when it operates on the Zener region, i.e., $-V_D \geq V_Z$, and is OFF when $0 < -V_D < V_Z$, as shown in figures 2.27(a) and 2.27(b) below.




(a) (b)

Figure 2.27: Zener diode operation: (a)ON (b) OFF.

- Although Zener diode behaves like a normal diode in forward bias, Zener diode is not normally used in forward bias.
- Zener diode also needs some minimum current $I_{Z(min)}$ in order to turn ON, although voltage threshold $-V_D \geq V_Z$ is satisfied. If not given, $I_{Z(min)} = 0\,\text{A}$.
- There is also a maximum power limit $P_{Z(max)}$ for the Zener diode. Note that, maximum power limit results in a maximum current limit $I_{Z(max)}$ given by $I_{Z(max)} = \frac{P_{Z(max)}}{V_Z}$.

### 2.4.1 Zener Regulator

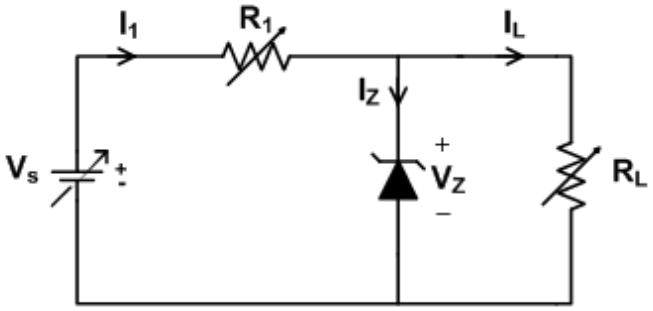



Figure 2.28: A general Zener diode circuit.

In a Zener regulator circuit likein Figure 2.28 above, Zener diode must be always ON in order to continuously regulate the voltage over the load $R_L$. So, let us derive the necessary equations for the two limiting factors $I_{Z(min)}$ and $I_{Z(max)}$ using

$$\boxed{I_Z = I_1 - I_L} \tag{2.4.13}$$

.

- Let us first write down the equation for $I_{Z(min)}$

$$\boxed{I_{Z(min)} = I_{1(min)} - I_{L(max)}} \tag{2.4.14}$$

where $I_{L(max)}$ and $I_{1(min)}$ are given by

$$I_{L(max)} = \frac{V_Z}{R_{L(min)}} \tag{2.4.15}$$

$$I_{1(min)} = \frac{V_{s(min)} - V_Z}{R_{1(max)}} \tag{2.4.16}$$

- Similarly, we can also write down the equation for $I_{Z(max)}$

$$\boxed{I_{Z(max)} = I_{1(max)} - I_{L(min)}} \tag{2.4.17}$$

where $I_{L(min)}$ and $I_{1(max)}$ are given by

$$I_{L(min)} = \frac{V_Z}{R_{L(max)}} \tag{2.4.18}$$

$$I_{1(max)} = \frac{V_{s(max)} - V_Z}{R_{1(min)}} \tag{2.4.19}$$

- Note that the values of $V_Z$, $I_{Z(min)}$ and $I_{Z(max)}$ (or $P_{Z(min)}$ and $P_{Z(max)}$) are specified in the specification sheet (or data sheet) of a Zener diode.

**Example 2.9:** (2004-2005 MI) In the figure below, $V_s$ is an unregulated voltage that varies between 6 V and 7 V while the Zener diode voltage is $V_Z = 5\,\text{V}$. The load resistor $R_L$ can have a value from $100\,\Omega$ to $\infty$ (i.e., open circuit). Also you can take $I_{Z(min)} \cong 0\,\text{A}$.

a) Find the **maximum** value of $R_1$ so that the load voltage $V_L$ would be still kept constant at 5 V **for all values** of $R_L$ and $V_s$.

b) Provide a symbolic expression for the **maximum power** dissipated by the Zener diode.

c) Determine the **minimum** value of $R_1$ so that the power dissipated by the Zener diode never exceeds 1 W **for all values** of $R_L$ and $V_s$.

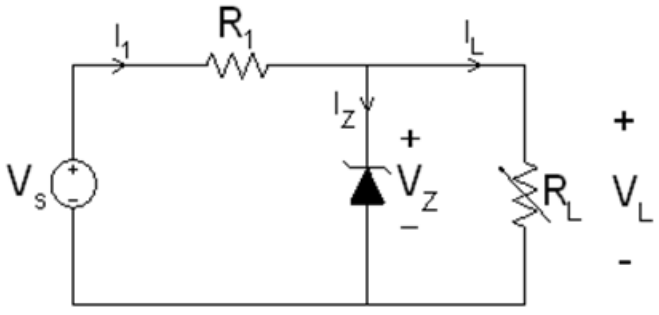



Figure 2.29: Zener diode circuit for Example 2.9.

**Solution:**

a) As $I_{Z(min)} = I_{1(min)} - I_{L(max)} = 0$, $I_{1(min)} = I_{L(max)}$, i.e.,

$$\frac{V_{s(min)} - V_Z}{R_{1(max)}} = \frac{V_Z}{R_{L(min)}}$$

$$R_{1(max)} = \frac{V_{s(min)} - V_Z}{V_Z} R_{L(min)} = \frac{6-5}{5} 100 = \underline{20\,\Omega}.$$

b) $P_{Z(max)} = V_Z I_{Z(max)}$.

c) It is given that $P_{Z(max)} = 1\,\text{W}$, so

$$I_{Z(max)} = \frac{P_{Z(max)}}{V_Z} = \frac{1}{5} = 0.2\,\text{A}$$

$$I_{L(min)} = \frac{V_Z}{R_{L(max)}} = \frac{5}{\infty} = 0\,\text{A}$$

$$I_{1(max)} = I_{Z(max)} + I_{L(min)} = I_{Z(max)} = 0.2\,\text{A}$$

$$R_{1(min)} = \frac{V_{s(max)} - V_Z}{I_{1(max)}} = \frac{7-5}{0.2} = \underline{10\,\Omega}.$$

### 2.4.2 Other Zener Diode Regulators

- A single Zener diode can limit one side of a sinusoidal waveform to the Zener voltage while clamping the other side to near zero as shown in Figure 2.30 below

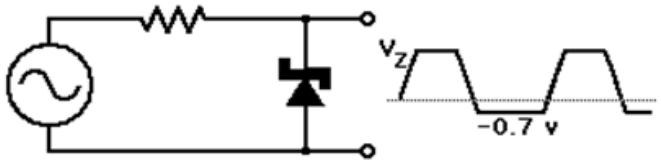



Figure 2.30: Single Zener diode clipper.

- With two opposing Zeners, the waveform can be limited to the Zener voltage on both polarities as shown in Figure 2.31 below.

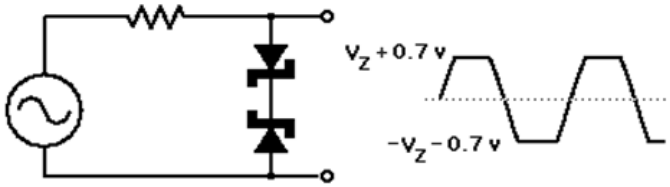



Figure 2.31: Dual Zener diode clipper.

### 2.4.3 Zener Diode Parameters

The basic parameters of a Zener diode are:

a) Obviously, the Zener voltage must be specified. The most common range of Zener voltage is 3.3 volts to 75 volts, however voltages out of this range are available.

b) A tolerance of the specified voltage must be stated. While the most popular tolerances are 5% and 10%, more precision tolerances as low as 0.05% are available. A test current ($I_{Z(test)}$) must be specified with the voltage and tolerance.

c) The power handling capability must be specified for the Zener diode. Popular power ranges are: 0.25, 0.5, 1, 5, 10, and 50 Watts.

## 2.5 Practical Applications of Diode Circuits

- **Rectifier Circuits**
  - Conversions of AC to DC for DC operated circuits
  - Battery Charging Circuits
- **Simple Diode Circuits**
  - Protective Circuits against
    - Overcurrent
    - Polarity Reversal
    - Currents caused by an inductive kick in a relay circuit
- **Zener Circuits**
  - Overvoltage Protection
  - Setting Reference Voltages

# Chapter 3

# Rectifiers and Voltage Regulating Filters

## 3.1 Properties of Electrical Signals

### 3.1.1 DC Component (Average Value) and AC Component

- Every (periodic) signal has a DC component and an AC component, i.e.,

$$v(t) = V_{DC} + v_{ac}(t) \tag{3.1.1}$$

  where $V_{DC}$ is the DC component and $v_{ac}(t)$ is the AC component.

- **DC component** $V_{DC}$ is defined as the **time-average** or **mean** of the signal within one period, i.e.,

$$\boxed{V_{DC} = V_{\text{avg}} = \frac{1}{T}\int_0^T v(t)dt} \tag{3.1.2}$$

  where $T$ is the period of the signal.

  $V_{DC}$ is the voltage value displayed for $v(t)$ on a DC voltmeter.

- **AC component** $v_{ac}(t)$ is the **zero-mean time-varying** component of the signal given by

$$\boxed{v_{ac}(t) = v(t) - V_{DC}} \tag{3.1.3}$$

**IMPORTANT:** In this course, we are going to use

1. **capital** letters for both quantity symbols and subscripts of **DC** components, e.g., $I_{DQ}$,
2. **small** letters for both quantity symbols and subscripts of **AC** components, e.g., $i_d$,
3. small letters for quantity symbols and capital letters for subscripts of **AC+DC** signals, e.g., $i_D$ where $i_D = I_{DQ} + i_d$.

**Example 3.1:** Let us calculate the DC component of the half-wave rectifier output shown in Figure 3.1 below.

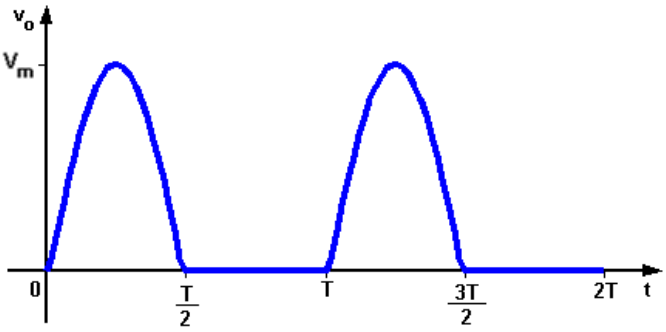



Figure 3.1: Ideal half-wave rectifier output of a sinusoidal input $v_i(t) = V_m \sin(2\pi t/T)$.

**Solution:** DC component of the signal given by its time-average in one period. However in the case of the half-wave rectifier output shown in Figure 3.1 above, second half-cycle of the signal is zero. So, we only need to integrate first half-cycle of the signal.

$$
\begin{aligned}
V_{DC} &= \frac{1}{T}\int_0^{T/2} V_m \sin(2\pi t/T)dt \\
&= \frac{1}{2\pi} V_m \int_0^{\pi} \sin\theta \, d\theta && \ldots \text{using change of variables with } \theta = \frac{2\pi t}{T} \\
&= \frac{V_m}{2\pi}\left[-\cos\theta\right]_0^{\pi} && \ldots \text{and } dt = \frac{T}{2\pi} d\theta. \\
&= \frac{V_m}{\pi} && (3.1.4) \\
&\cong 0.318\, V_m && (3.1.5)
\end{aligned}
$$

**Example 3.2:** Let us calculate the DC component of the full-wave rectifier output shown in Figure 3.2 below.

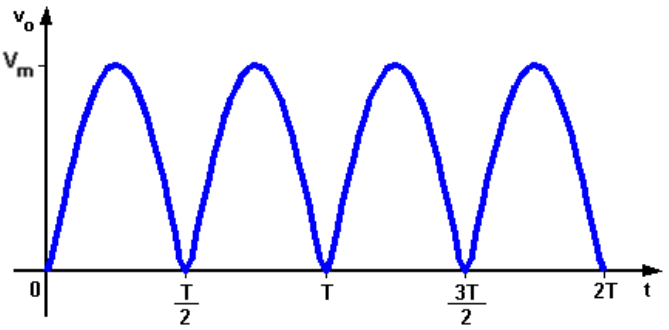



Figure 3.2: Ideal full-wave rectifier output of a sinusoidal input $v_i(t) = V_m \sin(2\pi t/T)$.

**Solution:** DC component of the signal given by its time-average in one period. However in the case of the full-wave rectifier output shown in Figure 3.2 above, the period of the output signal

is $\frac{T}{2}$.

$$
\begin{aligned}
V_{DC} &= \frac{2}{T}\int_0^{T/2} V_m \sin(2\pi t/T)dt \\
&= \frac{1}{\pi}V_m \int_0^{\pi} \sin\theta\, d\theta \qquad \ldots \text{using change of variables with } \theta = \frac{2\pi t}{T} \\
&= \frac{V_m}{\pi}\left[-\cos\theta\right]_0^{\pi} \qquad \ldots \text{and } dt = \frac{T}{2\pi}d\theta. \\
&= \frac{2V_m}{\pi} \qquad (3.1.6) \\
&\cong 0.636\, V_m \qquad (3.1.7)
\end{aligned}
$$

**Example 3.3:** Let us calculate the DC component of the triangular waveform shown in Figure 3.3 below.

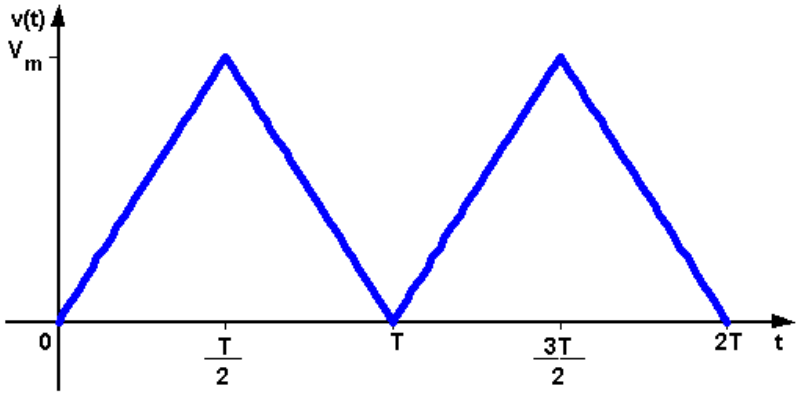



Figure 3.3: Triangular waveform.

**Solution:** DC component of the signal given by its time-average in one period. In this case the integral of the waveform in one period is the area of the triangle present ($V_m T/2$) in one period as seen in Figure 3.2 above.

$$
\begin{aligned}
V_{DC} &= \frac{1}{T}\int_0^{T} v(t)dt \\
&= \frac{1}{T}\left(\frac{V_m T}{2}\right) \qquad (3.1.8) \\
&= \frac{V_m}{2} \qquad (3.1.9)
\end{aligned}
$$

**Example 3.4:** Let us find the AC component of the triangular waveform shown in Figure 3.3.

**Solution:** AC component of the signal is obtained by subtracting the DC component, i.e.,

$$v_{ac}(t) = v(t) - V_{DC} = v(t) - \frac{V_m}{2}. \qquad (3.1.10)$$

Thus, the AC component of the triangular waveform is plotted as shown in Figure 3.4 below.

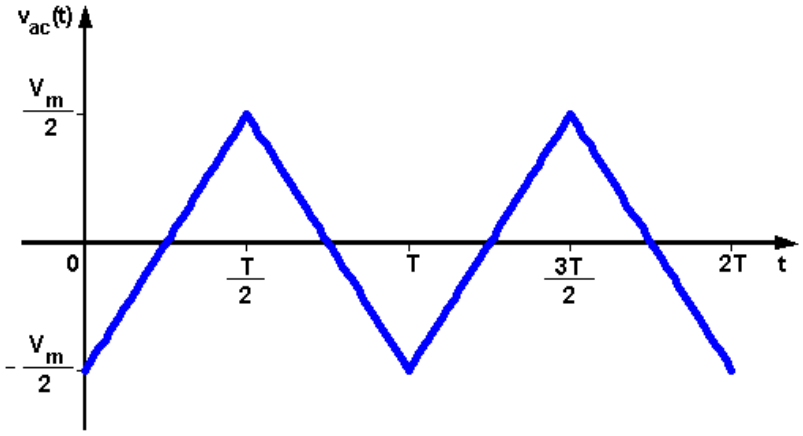



Figure 3.4: AC component of the triangular waveform in Figure 3.3.

### 3.1.2 Effective Value (RMS Value)

- **Average power** or **mean power** is defined as the time-average of the instantaneous power over a period, i.e.,

$$P_{\text{avg}} = \frac{1}{T}\int_0^T p(t)dt \tag{3.1.11}$$

where $p(t)$ is the instantaneous power and $T$ is the period of $p(t)$.

- The idea of effective current and voltage values comes from the need for writing the average power as a multiple of voltage and current values just like the Watt's law, i.e.,

$$P_{\text{avg}} = V_{\text{effective}} I_{\text{effective}} \tag{3.1.12}$$

where $V_{\text{effective}}$ and $I_{\text{effective}}$ are the effective voltage and current values, respectively.

#### Effective Voltage Value

- Let us obtain the effective voltage value $V_{\text{effective}}$ by defining average power over a resistor $R$

$$\begin{aligned} P_{\text{avg}} &= \frac{1}{T}\int_0^T \frac{v^2(t)}{R}dt \\ &= \frac{1}{R}\underbrace{\left(\frac{1}{T}\int_0^T v^2(t)dt\right)}_{V^2_{\text{effective}}} \qquad (3.1.13) \\ &= \frac{V^2_{\text{effective}}}{R} \qquad (3.1.14) \end{aligned}$$

- Thus, effective voltage value $V_{\text{effective}}$ is given as the **root-mean-square** (RMS) of the voltage signal, i.e.,

$$\boxed{V_{\text{effective}} = V_{\text{rms}} = \sqrt{\frac{1}{T}\int_0^T v^2(t)dt}} \tag{3.1.15}$$

$V_{\text{rms}}$ is the voltage value displayed for $v(t)$ on an AC voltmeter.

**Effective Current Value**

- Let us obtain the effective current value $I_{\text{effective}}$ by defining average power over a resistor $R$

$$\begin{aligned} P_{\text{avg}} &= \frac{1}{T}\int_0^T i^2(t)Rdt \\ &= \underbrace{\left(\frac{1}{T}\int_0^T i^2(t)dt\right)}_{I^2_{\text{effective}}} R \qquad (3.1.16) \\ &= I^2_{\text{effective}}R \qquad (3.1.17) \end{aligned}$$

- Thus, effective current value $I_{\text{effective}}$ is given as the **root-mean-square** (RMS) of the current signal, i.e.,

$$\boxed{I_{\text{effective}} = I_{\text{rms}} = \sqrt{\frac{1}{T}\int_0^T i^2(t)dt}} \qquad (3.1.18)$$

$I_{\text{rms}}$ is the voltage value displayed for $i(t)$ on an AC ammeter.

**Example 3.5:** Calculate the RMS value $V_{\text{rms}}$ of the mixed signal

$$v(t) = A + B\cos\omega t.$$

**Solution:** Let us find $V^2_{\text{rms}}$ first where $\omega = 2\pi f = 2\pi/T$

$$\begin{aligned} V^2_{\text{rms}} &= \frac{1}{T}\int_0^T (A + B\cos\omega t)^2\, dt \\ &= \frac{1}{T}\int_0^T \left(A^2 + \cancel{2AB\cos\omega t} + B^2\cos^2\omega t\right) dt \\ &= \frac{1}{T}\left(\left[A^2\, t\right]_0^T + \frac{B^2}{2}\int_0^T (1+\cos 2\omega t)\, dt\right) \\ &= A^2 + \frac{B^2}{2} + \frac{B^2}{2T}\cancel{\left[\frac{\sin 2\omega t}{T}\right]_0^T} \\ &= A^2 + \frac{B^2}{2} \end{aligned}$$

So,

$$V_{\text{rms}} = \sqrt{A^2 + \frac{B^2}{2}}$$

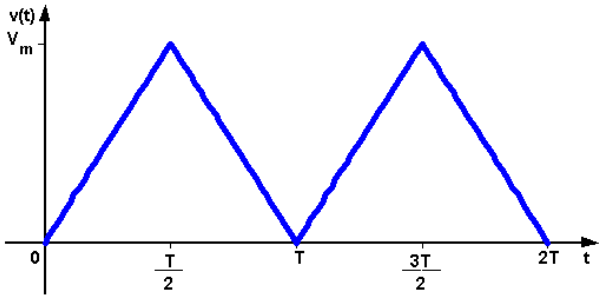
- We can generalize the result of Example 3.5 for the RMS value $V_{\text{rms}}$ of a general AC+DC signal $v(t)$ where

$$v(t) = V_{DC} + v_{ac}(t),$$

as the **combined RMS equation** given below

$$\boxed{V_{\text{rms}} = \sqrt{V_{DC}^2 + V_{ac(\text{rms})}^2}} \tag{3.1.19}$$

**Example 3.6:** Calculate the RMS value of the triangular waveform shown in Figure 3.5 below.




$$v(t) = \begin{cases} \dfrac{2V_m}{T}t, & 0 \le t < T/2 \\ 2V_m - \dfrac{2V_m}{T}t, & T/2 \le t < T \end{cases}$$

Figure 3.5: Triangular waveform and its analytical expression.

**Solution:** Let us calculate $V_{\text{rms}}^2$ by using integration by parts

$$\begin{aligned} V_{\text{rms}}^2 &= \frac{1}{T}\left(\int_0^{T/2}\left(\frac{2V_m}{T}t\right)^2 dt + \int_{T/2}^{T}\left(2V_m - \frac{2V_m}{T}t\right)^2 dt\right) \\ &= \frac{1}{T}\left(\frac{4V_m^2}{T^2}\int_0^{T/2} t^2 dt + 4V_m^2\int_{T/2}^{T}\left(1 - \frac{2}{T}t + \frac{1}{T^2}t^2\right) dt\right) \\ &= \frac{4V_m^2}{T^3}\left[\frac{t^3}{3}\right]_0^{T/2} + \frac{4V_m^2}{T}\left[t - \frac{t^2}{T} + \frac{t^3}{3T^2}\right]_{T/2}^{T} \\ &= \frac{4V_m^2}{\cancel{T^3}}\frac{\cancel{T^3}}{24} + \frac{4V_m^2}{\cancel{T}}\left[\frac{\cancel{T}}{2} - \frac{3\cancel{T}}{4} + \frac{7\cancel{T}}{24}\right] \\ &= \frac{V_m^2}{3} \end{aligned}$$

So, the **RMS value** of the **triangular waveform** is given by

$$V_{\text{rms}} = \frac{V_m}{\sqrt{3}} \tag{3.1.20}$$

**Example 3.7:** Calculate the RMS value of the ideal half-wave rectifier output given in Figure 3.1.

**Solution:** Let us first calculate the $V_{\text{rms}}^2$

$$\begin{aligned} V_{\text{rms}}^2 &= \frac{1}{T}\int_0^{T/2} V_m^2 \sin^2(2\pi t/T)dt \\ &= \frac{1}{2\pi}V_m^2 \int_0^{\pi} \sin^2\theta \, d\theta && \ldots \text{using change of variables } \theta = \frac{2\pi t}{T} \\ &= \frac{V_m^2}{2\pi}\int_0^{\pi} \frac{1}{2}(1 - \cancel{\cos 2\theta})d\theta && \ldots \text{using trigonometric identities} \\ &= \frac{V_m^2}{4} \end{aligned}$$

So, the **RMS value** of the **ideal half-wave rectifier output** is given by

$$V_{\text{rms}} = \frac{V_m}{2} \tag{3.1.21}$$

**Example 3.8:** Calculate the RMS value of the ideal full-wave rectifier output given in Figure 3.2.

**Solution:** Let us first calculate the $V_{\text{rms}}^2$

$$\begin{aligned} V_{\text{rms}}^2 &= \frac{2}{T}\int_0^{T/2} V_m^2 \sin^2(2\pi t/T)dt \\ &= \frac{1}{\pi}V_m^2 \int_0^{\pi} \sin^2\theta \, d\theta && \ldots \text{using change of variables } \theta = \frac{2\pi t}{T} \\ &= \frac{V_m^2}{\pi}\int_0^{\pi} \frac{1}{2}(1 - \cancel{\cos 2\theta})d\theta && \ldots \text{using trigonometric identities} \\ &= \frac{V_m^2}{2} \end{aligned}$$

So, the **RMS value** of the **ideal full-wave rectifier output** is given by

$$V_{\text{rms}} = \frac{V_m}{\sqrt{2}} \cong 0.707\, V_m \tag{3.1.22}$$

**Example 3.9:** Calculate the RMS value $V_{ac(\text{rms})}$ of the AC component of the triangular waveform shown in Figure 3.4.

**Solution:** We are going to use the combined RMS equation given in (3.1.19) with the already calculated DC and RMS values of the triangular waveform given in (3.1.9) and (3.1.20),

respectively as follows

$$\begin{aligned} V_{ac(\text{rms})}^2 &= V_{rms}^2 - V_{DC}^2 \\ &= \left(\frac{V_m}{\sqrt{3}}\right)^2 - \left(\frac{V_m}{2}\right)^2 \\ &= \frac{V_m^2}{3} - \frac{V_m^2}{4} \\ &= \frac{V_m^2}{12}. \end{aligned}$$

So, the **RMS value** of the **AC component of the triangular waveform** is given by

$$\boxed{V_{ac(\text{rms})} = \frac{V_m}{2\sqrt{3}}} \tag{3.1.23}$$

**Example 3.10:** Calculate the RMS value $V_{ac(\text{rms})}$ of the AC component of the ideal half-wave rectifier output.

**Solution:** We are going to use the combined RMS equation given in (3.1.19) with the already calculated DC and RMS values of the ideal half-wave rectifier output given in (3.1.4) and (3.1.21), respectively as follows

$$\begin{aligned} V_{ac(\text{rms})}^2 &= V_{rms}^2 - V_{DC}^2 \\ &= \left(\frac{V_m}{2}\right)^2 - \left(\frac{V_m}{\pi}\right)^2 \\ &= \frac{V_m^2}{4} - \frac{V_m^2}{\pi^2} \end{aligned}$$

So, the **RMS value** of the **AC component of the half-wave rectifier output** is given by

$$V_{ac(\text{rms})} = V_m\sqrt{\frac{1}{4} - \frac{1}{\pi^2}} \cong 0.386\, V_m \tag{3.1.24}$$

**Example 3.11:** Calculate the RMS value $V_{ac(\text{rms})}$ of the AC component of the ideal full-wave rectifier output.

**Solution:** We are going to use the combined RMS equation given in (3.1.19) with the already calculated DC and RMS values of the ideal full-wave rectifier output given in (3.1.6) and (3.1.22), respectively, as follows

$$\begin{aligned} V_{ac(\text{rms})}^2 &= V_{rms}^2 - V_{DC}^2 \\ &= \left(\frac{V_m}{\sqrt{2}}\right)^2 - \left(\frac{2V_m}{\pi}\right)^2 \\ &= \frac{V_m^2}{2} - \frac{4V_m^2}{\pi^2} \end{aligned}$$

So, the **RMS value** of the **AC component of the full-wave rectifier output** is given by

$$V_{ac(\text{rms})} = V_m\sqrt{\frac{1}{2} - \frac{4}{\pi^2}} \cong 0.308\, V_m \tag{3.1.25}$$

## 3.2 Half-Wave Rectifier

- Generating a waveform with a **non-zero mean** value, i.e., **non-zero DC component**, from an AC waveform (i.e., a zero-mean time-varying signal) is called **rectification**. The circuits which perform rectification are called **rectifiers**. This is a crude AC to DC conversion.
- A **half-wave rectifier** rectifies only half-cycle of the waveform, i.e., circuits conducts only for one-half of the AC cycle, maintaining the average of the output signal non-zero.
- A **half-wave rectifier circuit** is the same as the **series clipper circuit** shown in Figure 3.6 below.

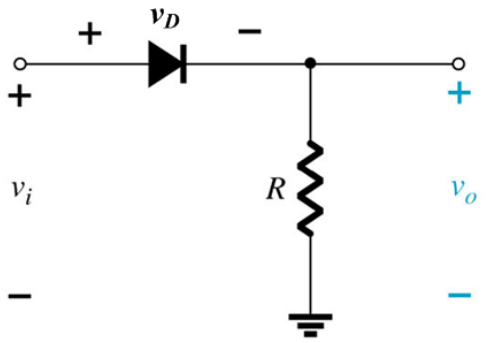



Figure 3.6: A half-wave rectifier circuit.

- Sample input and ideal output waveforms for an half-wave rectifier such as given inFigure 3.6 are given in Figure 3.7 below.

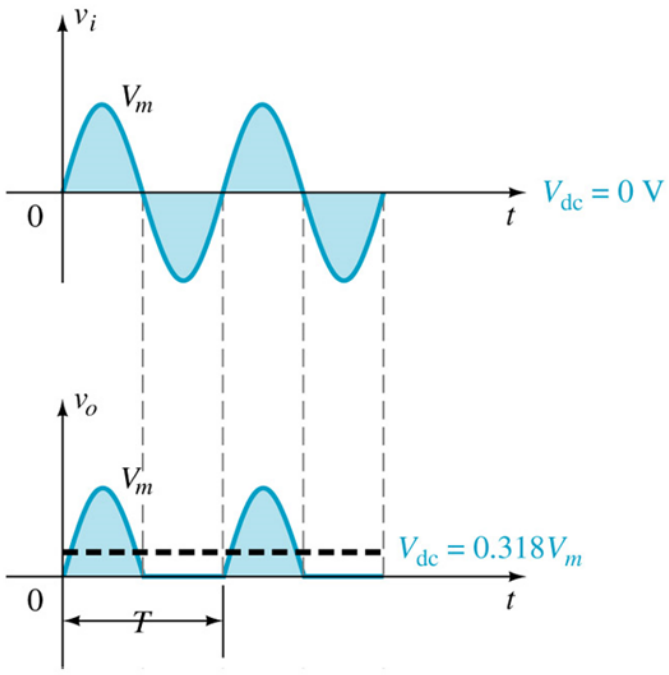



Figure 3.7: Input and ideal output waveforms for the half-wave rectifier given in Figure 3.6.

- The DC voltage output of the half-wave rectifier is the DC component of the output waveform and as calculated before in (3.1.4) it is given by

$$\boxed{V_{DC(\text{half-wave})} = \frac{1}{\pi} V_m \cong 0.318\, V_m} \tag{3.2.26}$$

where $V_m$ is the peak voltage of the input sinusoidal signal.

- The output of the half-wave rectifier for $V_{D(ON)} = 0.7\,\text{V}$ is shown in Figure 3.8 below

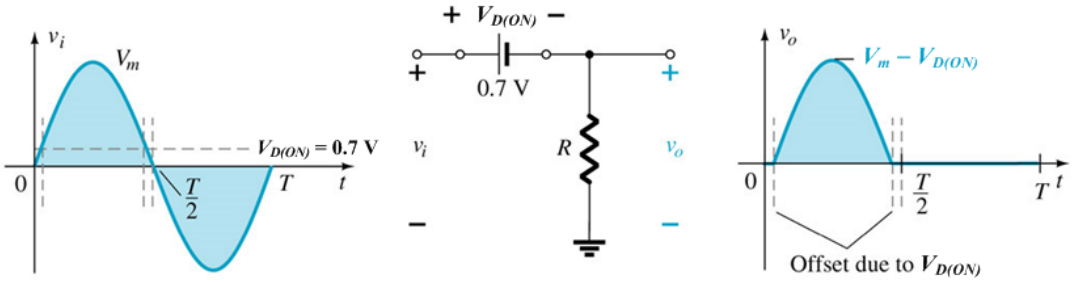



Figure 3.8: Input and output waveforms for the half-wave rectifier when $V_{D(ON)} = 0.7\,\text{V}$.

When $V_{D(ON)} \neq 0$, the DC voltage output of the half-wave rectifier is approximately equal to

$$\boxed{V_{DC(\text{half-wave})} \cong \frac{1}{\pi} V_m - \frac{1}{2} V_{D(ON)} = 0.318\, V_m - 0.5\, V_{D(ON)}} \tag{3.2.27}$$

- When the diode is **OFF**, **maximum negative voltage** between the terminals of the diode is the negative peak value $-V_m$. So, the peak-inverse-voltage for the half-wave rectifier is given by

$$\boxed{\text{PIV}_{(\text{half-wave rectifier})} = V_m} \tag{3.2.28}$$

Thus, we need to select a diode with a PIV rating greater than $V_m$, i.e., $\text{PIV}_{\text{diode}} > V_m$, to use in our half-wave rectifier circuit.

## 3.3 Full-Wave Rectifier

- A **full-wave rectifier** rectifies both cycles of the waveform producing a higher DC output as shown in Figure 3.9 below

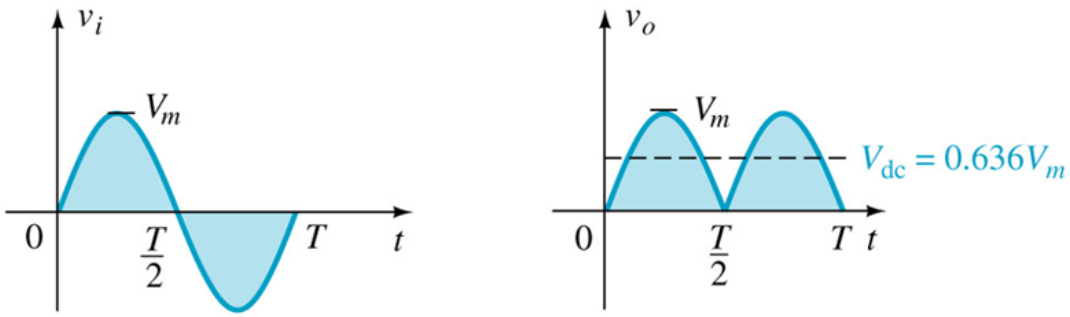



Figure 3.9: Input and ideal output waveforms of the full-wave rectifier.

- The DC voltage output of the full-wave rectifier is the DC component of the output waveform and as calculated before in (3.1.6) it is given by

$$\boxed{V_{DC(\text{full-wave})} = \frac{2}{\pi} V_m \cong 0.636\, V_m} \tag{3.3.29}$$

where $V_m$ is the peak voltage of the input sinusoidal.

**Full-Wave Rectifier Circuits**

There are two types of full-wave rectifier circuits:

1. Center-Tapped Transformer Full-Wave Rectifier
2. Full-Wave Bridge Rectifier

### 3.3.1 Center-Tapped Transformer Full-Wave Rectifier

Center-tapped transformer full-wave rectifier shown in Figure 3.10 below requires a center-tapped (CT) transformer to establish the replica of the input signal across each section of the secondary of the transformer and then combining two half-wave rectifiers together where the two half-wave rectifiers operate on opposite cycles of the input signal.

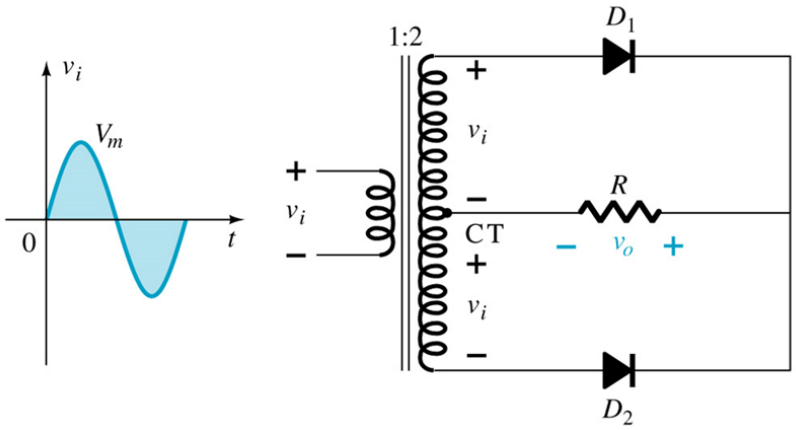



Figure 3.10: Center-tapped transformer full-wave rectifier.

Here, $D_1$ operates on the positive half-cycle and $D_2$ operates on the negative half-cycle of input $v_i$.

- Using the ideal diode model, operation of the center-tapped transformer full-wave rectifier are shown for positive and negative cycles in Figure 3.11 and Figure 3.12 below, respectively.

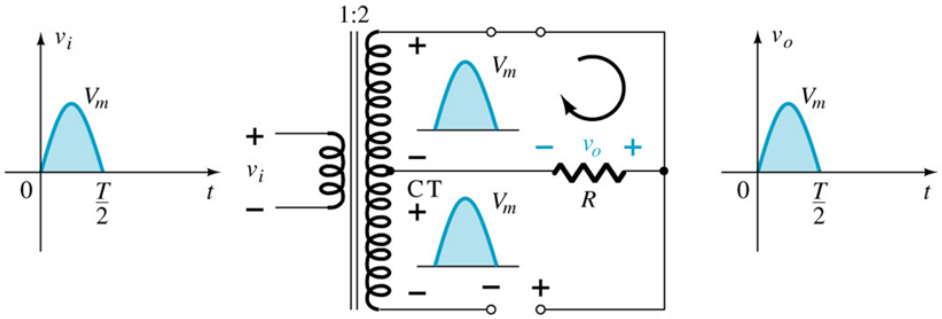



Figure 3.11: Positive half-cycle operation of the center-tapped transformer full-wave rectifier in Figure 3.10.

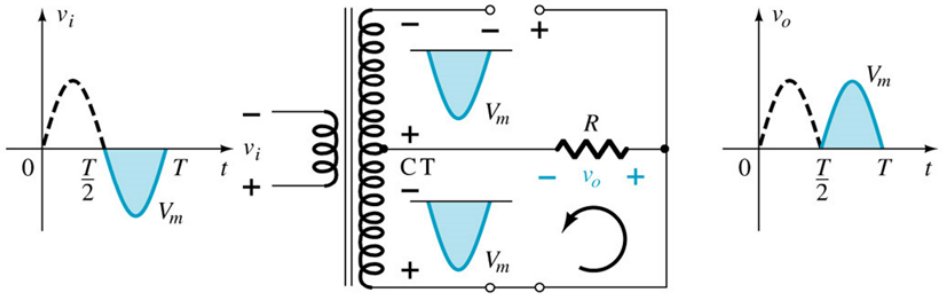



Figure 3.12: Negative half-cycle operation of the center-tapped transformer full-wave rectifier in Figure 3.10.

- When the diodes are **OFF**, **maximum negative voltage** between the terminals of the diodes are twice the negative peak value. So, the peak-inverse-voltage for the center-tapped transformer full-wave rectifier is given by

$$\boxed{\text{PIV}_{(\text{center-tapped})} = 2V_m} \tag{3.3.30}$$

- When the diodes are not ideal, i.e., $V_{D(ON)} \neq 0$, the DC voltage output of the center-tapped transformer full-wave rectifier is approximately equal to

$$\boxed{V_{DC(\text{center-tapped})} \cong \frac{2}{\pi}V_m - V_{D(ON)} = 0.636\,V_m - V_{D(ON)}} \tag{3.3.31}$$

where $V_m$ is the peak voltage of the input sinusoidal signal.

### 3.3.2 Full-Wave Bridge Rectifier

The most popular circuit to achieve full-wave rectification is four diodes in a bridge configuration as shown in Figure 3.13 below. The popularity of the rectifier comes from the fact that it eliminates the need for a transformer.

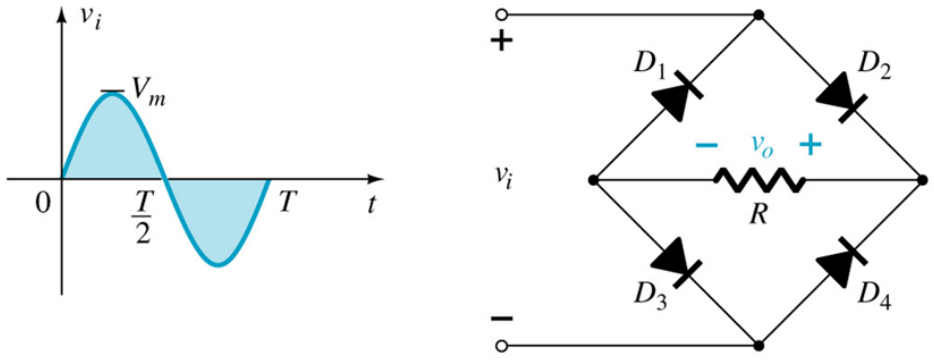



Figure 3.13: Full-wave bridge rectifier.

Here, $D_2$ and $D_3$ operate on the positive half-cycle, and $D_4$ and $D_1$ operate on the negative half-cycle of input $v_i$.

- Using the ideal diode model, operation of the full-wave bridge rectifier are shown for positive and negative cycles in Figure 3.14 and Figure 3.15 below, respectively.

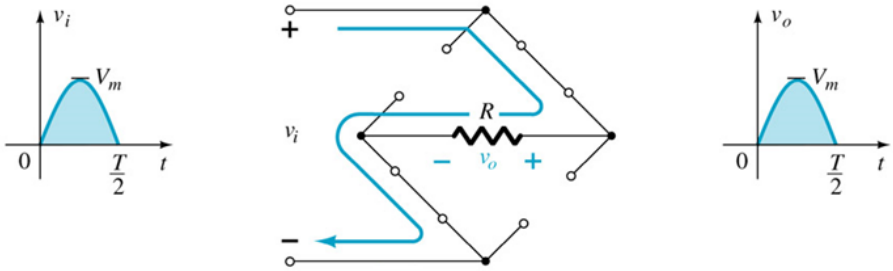



Figure 3.14: Positive half-cycle operation of the full-wave bridge rectifier in Figure 3.13.

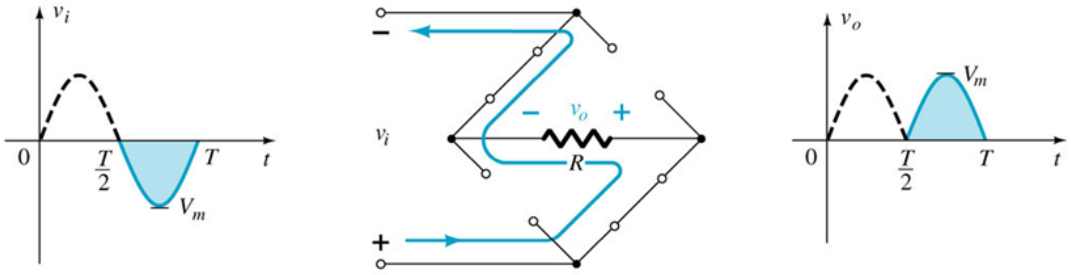



Figure 3.15: Negative half-cycle operation of the full-wave bridge rectifier in Figure 3.13.

- When the diodes are **OFF**, **maximum negative voltage** between the terminals of the diodes are equal to the negative peak value. So, the peak-inverse-voltage for the full-wave bridge rectifier is given by

$$\boxed{\text{PIV}_{(\text{bridge})} = V_m} \tag{3.3.32}$$

- The positive half-cycle operation and full output of the full-wave bridge rectifier for $V_{D(ON)} = 0.7\,\text{V}$ is shown in Figure 3.16 below

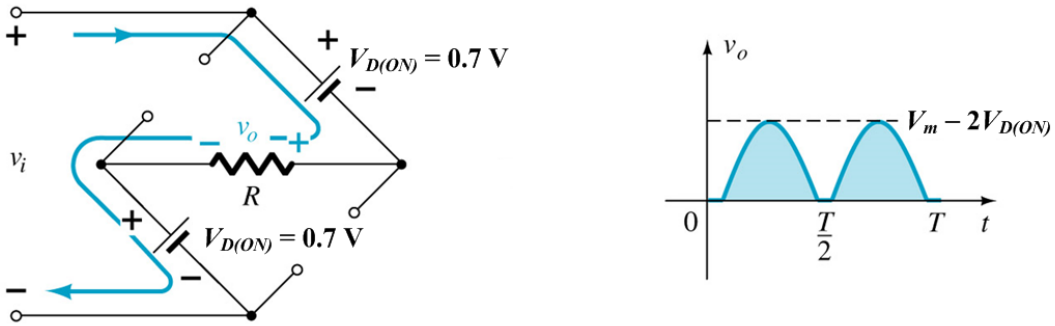



Figure 3.16: Positive-half cycle operation and full output of the full-wave bridge rectifier when $V_{D(ON)} = 0.7\,\text{V}$.

When the diodes are not ideal, i.e., $V_{D(ON)} \neq 0$, the DC voltage output of the full-wave bridge rectifier is approximately equal to

$$\boxed{V_{DC(\text{bridge})} \cong \frac{2}{\pi} V_m - 2V_{D(ON)} = 0.636\,V_m - 2V_{D(ON)}} \tag{3.3.33}$$

where $V_m$ is the peak voltage of the input sinusoidal signal.

## 3.4 Rectifier Summary

Summary of the rectifier circuits is given in Table 3.1 below.

Table 3.1: Rectifier Summary

| **Rectifier** | **Ideal Output** | **Realistic Output** | **PIV** |
|---|---|---|---|
| Half-Wave Rectifier | $V_{DC} = 0.318\,V_m$ | $V_{DC} = 0.318\,V_m - 0.5\,V_{D(ON)}$ | $V_m$ |
| Center-Tapped Transformer Full-Wave Rectifier | $V_{DC} = 0.636\,V_m$ | $V_{DC} = 0.636\,V_m - V_{D(ON)}$ | $2V_m$ |
| Full-Wave Bridge Rectifier | $V_{DC} = 0.636\,V_m$ | $V_{DC} = 0.636\,V_m - 2V_{D(ON)}$ | $V_m$ |
| **Note:** $V_m$ is the peak value of the sinusoidal input voltage. | | | |

**Homework 3.1:** Compare the center-tapped transformer rectifier and bridge rectifier listing their advantages and disadvantages. Which one is more preferable and why?

## 3.5 Voltage Regulation and Ripple Factor

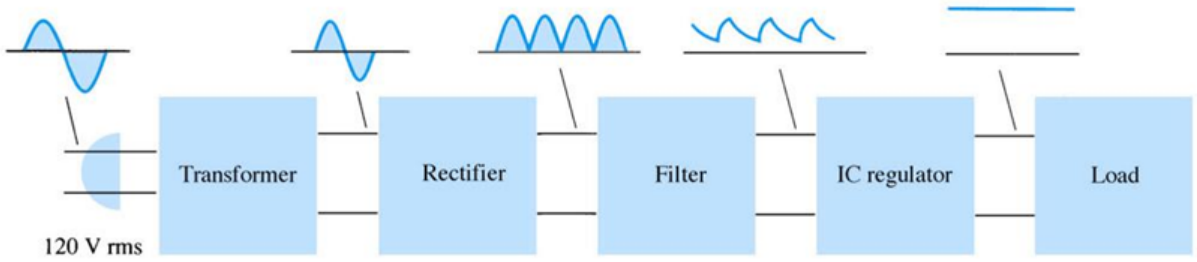



Figure 3.17: Block diagram showing parts of a power supply.

A block diagram containing the parts of a typical power supply and the voltages at various points in the unit is shown in shown in Figure 3.17 above.

1. The mains AC voltage (120 Vrms 60 Hz in USA, and 230 Vrms 50 Hz in Europe), is connected to a transformer, which steps that AC voltage down to the level for the desired DC output.
2. A diode rectifier then provides a full-wave rectified voltage.
3. Full-wave rectified voltage is then filtered by a simple capacitor filter to produce a DC voltage. This resulting DC voltage usually has some **ripple** or AC voltage variation.
4. Finally, obtained DC voltage is regulated to obtain a desired fixed DC voltage. The regulation circuit takes a DC voltage and provides a somewhat lower DC voltage, which remains the same even if the input DC voltage varies or the output load changes. Although one of the simplest regulators is a Zener regulator, usually an integrated circuit (IC) voltage regulator unit is used for voltage regulation.

### 3.5.1 Voltage Regulation

- An important factor in a power supply is the amount the DC output voltage changes over a range of loads. The voltage provided at the output under no-load condition (no current drawn from the supply) is reduced when load current is drawn from the supply (under load). The amount the DC voltage changes between the no-load (NL) and full-load (FL) conditions is described by a factor called **voltage regulation** (VR) given by

$$\boxed{\%\text{VR} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100} \tag{3.5.34}$$

**Example 3.12:** A DC voltage supply provides 60 V when the output is unloaded. When connected to a load, the output drops to 56 V. Calculate the value of voltage regulation.

**Solution:**

$$\%\text{VR} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{60 - 56}{56} \times 100 = 7.1\%.$$

- The smaller the voltage regulation, the better the operation of the voltage supply circuit.

### 3.5.2 Ripple Factor

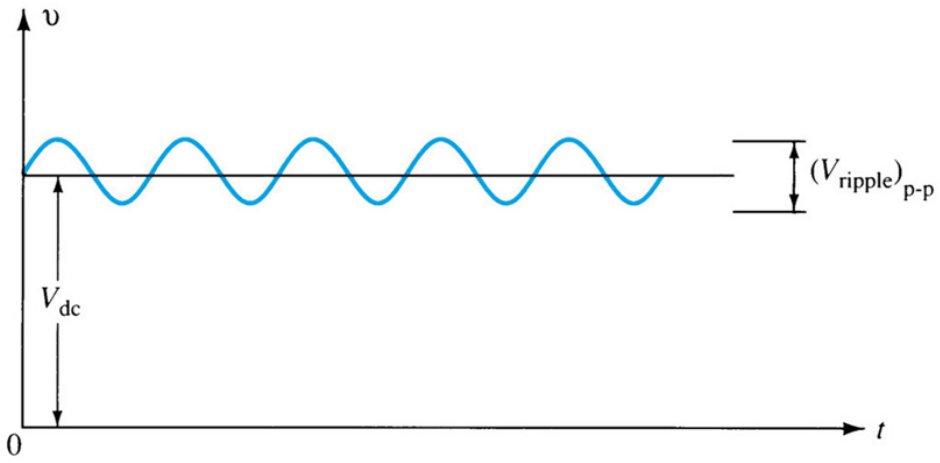



Figure 3.18: Filter voltage waveform showing DC and ripple voltages.

- The filtered output shown in Figure 3.18 above has a DC value and some AC variation (ripple). The smaller the AC variation with respect to the DC level, the better the filter circuit's operation (or the better the power supply). This ratio is called the **ripple factor** ($r$) expressed by

$$\boxed{\%r = \frac{V_{r(\text{rms})}}{V_{DC}} \times 100} \tag{3.5.35}$$

where $V_{r(\text{rms})}$ the RMS value of the AC ripple voltage $v_r(t)$ fluctuating around the DC value $V_{DC}$ at the output.

**Example 3.13:** Calculate the ripple factor of the ideal half-wave rectifier output shown in Figure 3.1.

**Solution:** From (3.1.5) and (3.1.24), we can obtain the ripple factor as

$$\%r_{(\text{half-wave})} = \frac{V_{ac(\text{rms})(\text{half-wave})}}{V_{DC(\text{half-wave})}} \times 100 = \frac{0.386\,V_m}{0.318\,V_m} \times 100 = 121\%.$$

**Example 3.14:** Calculate the ripple factor of the ideal full-wave rectifier output shown in Figure 3.2.

**Solution:** From (3.1.7) and (3.1.25), we can obtain the ripple factor as

$$\%r_{(\text{full-wave})} = \frac{V_{ac(\text{rms})(\text{full-wave})}}{V_{DC(\text{full-wave})}} \times 100 = \frac{0.308\,V_m}{0.636\,V_m} \times 100 = 48\%.$$

## 3.6 Capacitor Filter

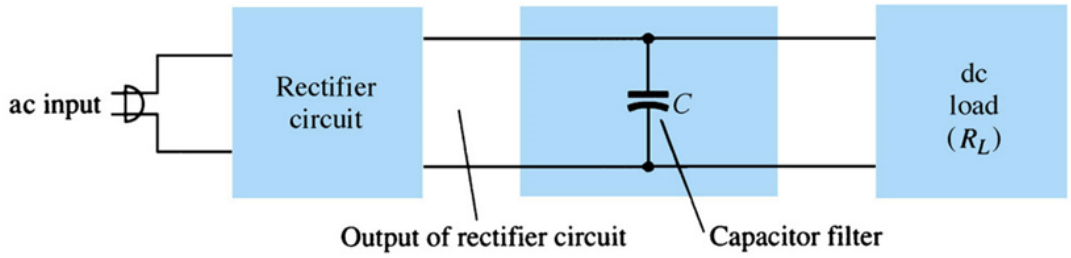



Figure 3.19: Simple capacitor filter.

- A very popular filter circuit is the capacitor-filter circuit shown in Figure 3.19 above. A capacitor is connected at the rectifier output, and a DC voltage is obtained across the capacitor.

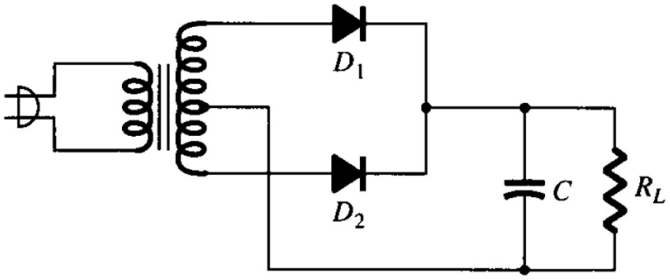
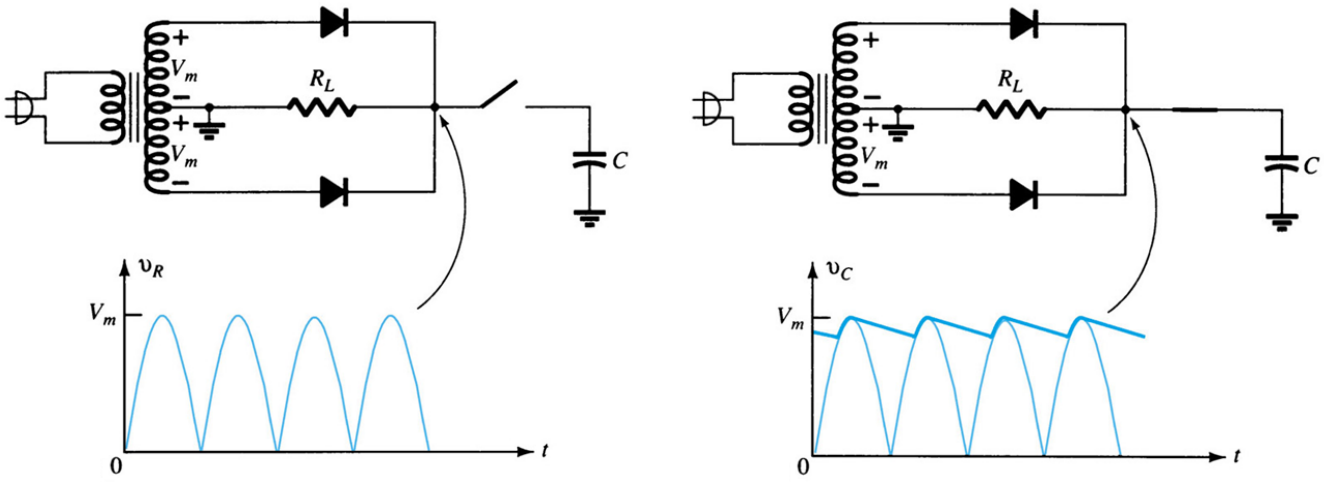



Figure 3.20: Capacitor filter after a center-tapped transformer full-wave rectifier.

- So, a full-wave rectifier integrated with a capacitor filter is shown in Figure 3.20 above.




(a) (b)

Figure 3.21: Capacitor filter operation: (a) ideal full-wave rectifier output, (b) filtered output voltage.

Figure 3.21(a) above shows the output voltage of the ideal full-wave rectifier before the signal is filtered,

while Figure 3.21(b) above shows the resulting waveform after the filter capacitor is connected at the rectifier output.

Notice that the filtered waveform is essentially a DC voltage with some ripple (or AC variation).

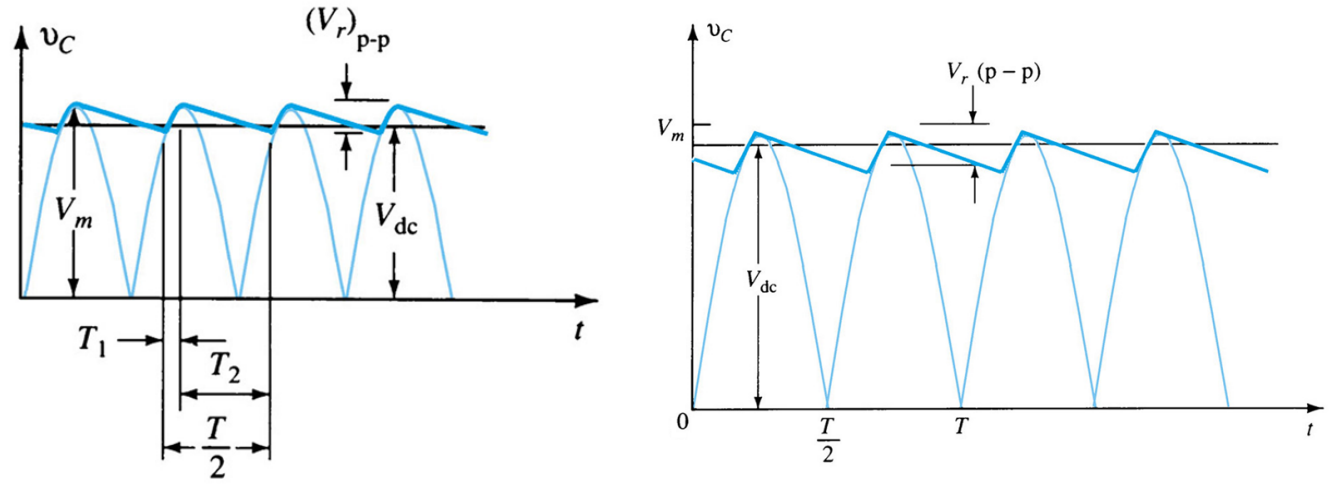



Figure 3.22: Capacitor filter output after a full-wave rectifier: (a) actual output, (b) approximate output where ripple waveform is approximated by a triangular waveform.

- When we analyse the capacitor filter output shown in Figure 3.22(a) above,

  Time $T_1$ is the time during which diodes of the full-wave rectifier conduct, charging the capacitor up to the peak rectifier voltage, $V_m$.

  Time $T_2$ is the time interval during which the rectifier voltage drops below the peak voltage, and the capacitor discharges through the load.

  Since the charge-discharge cycle occurs for each half-cycle for a full-wave rectifier, the period of the rectified waveform is $T/2$ (one-half the input signal frequency).

- The **ripples** of the filtered voltage can be approximated by a **triangular waveform** as shown in Figure 3.22(b) above, where the output waveform has a DC level $V_{DC}$ and a triangular ripple voltage $V_{r(\text{rms})}$ as the capacitor charges and discharges.

### 3.6.1 Ripple Factor of Capacitor Filter

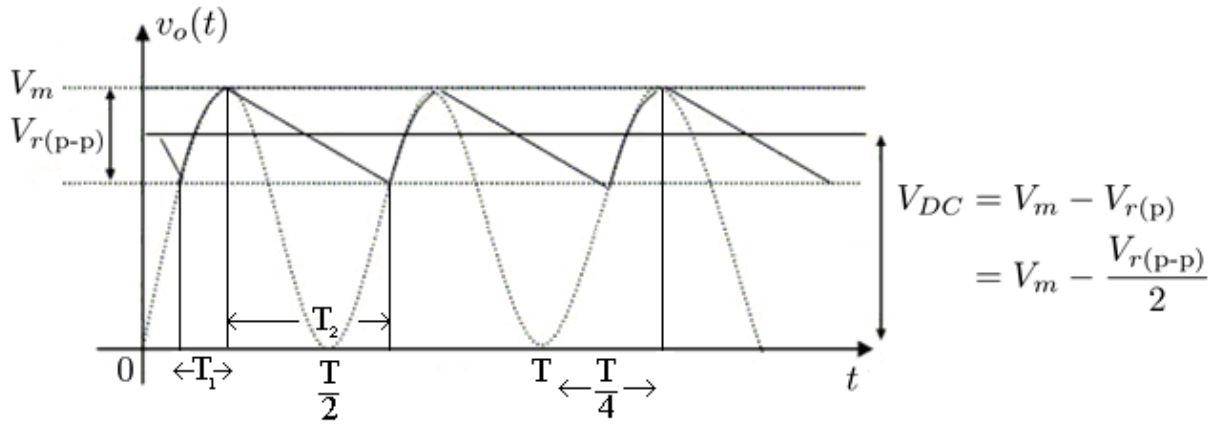



Figure 3.23: Capacitor filter output (after a full-wave rectifier) with charging and discharging timings.

Let us derive the expression for the ripple factor of the capacitor filter output shown in Figure 3.23 above

1. Charging period $T_1$ and discharging period $T_2$ together constitute the whole period $T/2$. Thus,

$$T_2 = \frac{T}{2} - T_1 \tag{3.6.36}$$

2. Peak-to-peak ripple voltage $V_{r(\text{p-p})}$ is given by

$$V_{r(\text{p-p})} = 2\,(V_m - V_{DC}) \tag{3.6.37}$$

3. We can express discharge current (i.e., load current) $I_{DC}$ as follows

$$I_{DC} = C\frac{\Delta V}{\Delta t} = C\frac{V_{r(\text{p-p})}}{T_2} \tag{3.6.38}$$

4. Using similar triangles we can obtain an expression for $T_1$

$$\frac{V_{r(\text{p-p})}}{T_1} \cong \frac{V_m}{T/4} \tag{3.6.39}$$

$$T_1 \cong \frac{V_{r(\text{p-p})}}{V_m}\frac{T}{4} \tag{3.6.40}$$

$$\cong \frac{2\,(V_m - V_{DC})}{V_m}\frac{T}{4} \qquad \ldots \text{from (3.6.37)}, \tag{3.6.41}$$

$$\cong \frac{T}{2} - \frac{V_{DC}T}{2V_m} \tag{3.6.42}$$

5. We can obtain $T_2$ from Step 1 and Step 3, i.e., from (3.6.37) and (3.6.42)

$$T_2 = \frac{V_{DC}T}{2V_m} \tag{3.6.43}$$

6. We can obtain $V_{r(\text{p-p})}$ from Step 3 and Step 5, i.e., from (3.6.38) and (3.6.43)

$$\boxed{V_{r(\text{p-p})} = \frac{I_{DC}}{2fC}\frac{V_{DC}}{V_m} = \frac{I_{DC}}{f_{\text{ripple}}C}\frac{V_{DC}}{V_m}} \tag{3.6.44}$$

where $f_{\text{ripple}} = 2f$ and $f = 1/T$ is the frequency of the input AC voltage.

7. Similarly, we can obtain $V_{r(\text{rms})}$ from Step 6 by using the RMS value of an AC triangular waveform given in (3.1.23)

$$V_{r(\text{rms})} = \frac{V_{r(\text{p-p})}}{2\sqrt{3}} \qquad \ldots \text{i.e., } V_{r(\text{p})} = \sqrt{3}V_{r(\text{rms})} \tag{3.6.45}$$

$$= \frac{I_{DC}}{2\sqrt{3}f_{\text{ripple}}C}\frac{V_{DC}}{V_m} \tag{3.6.46}$$

8. Thus, ripple factor $r$ is given by

$$r = \frac{V_{r(\text{rms})}}{V_{DC}} \tag{3.6.47}$$

$$= \frac{1}{2\sqrt{3}f_{\text{ripple}}CR_L}\frac{V_{DC}}{V_m} \qquad \ldots \text{as } V_{DC} = I_{DC}R_L \tag{3.6.48}$$

Due to $V_{r(\text{p})} = \sqrt{3}V_{r(\text{rms})}$ and $V_m = V_{DC} + V_{r(\text{p})}$, we obtain $\frac{V_{DC}}{V_m}$ as

$$\boxed{\frac{V_{DC}}{V_m} = \frac{V_{DC}}{V_{DC} + V_{r(\text{p})}} = \frac{1}{1 + \frac{V_{r(\text{p})}}{V_{DC}}} = \frac{1}{1 + \frac{\sqrt{3}V_{r(\text{rms})}}{V_{DC}}} = \frac{1}{1 + \sqrt{3}r}} \tag{3.6.49}$$

9. For light load (i.e., $r < 6.5\%$), $\dfrac{V_{DC}}{V_m} = \dfrac{1}{1 + \sqrt{3}r}$ ratio approaches to one, i.e.,

$$\frac{V_{DC}}{V_m} \cong 1.$$

So, expression for the ripple factor $r$ reduces to

$$\boxed{r \cong \frac{1}{2\sqrt{3}f_{\text{ripple}}CR_L}} \tag{3.6.50}$$

10. Hence when $\frac{V_{DC}}{V_m} \cong 1$, peak-to-peak ripple voltage $V_{r(p-p)}$ becomes

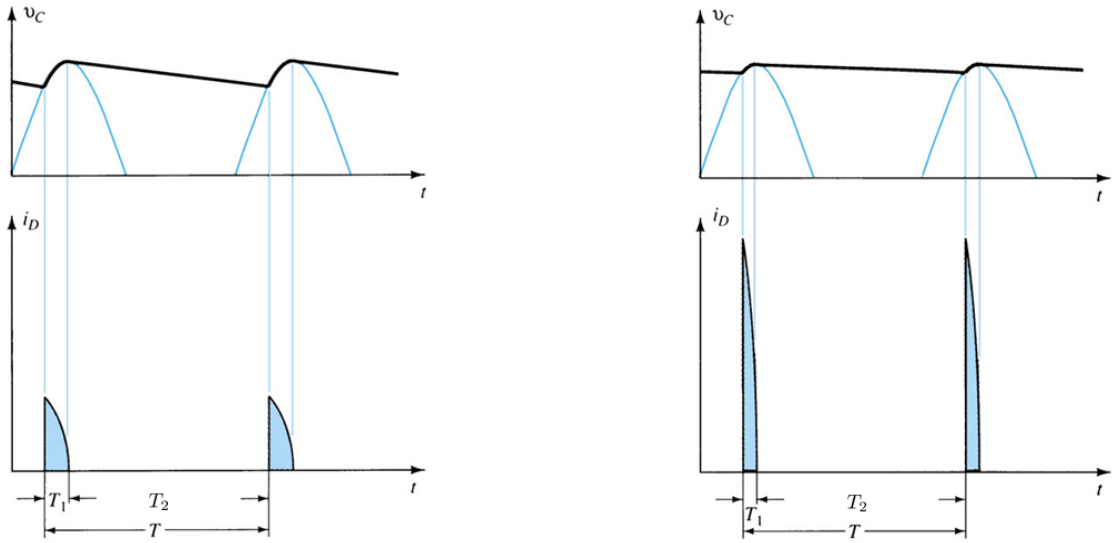
$$\boxed{V_{r(\text{p-p})} \cong \frac{I_{DC}}{f_{\text{ripple}}C}} \tag{3.6.51}$$

Thus, the **larger** the **capacitor** the **smaller** the **ripple voltage** and ripple factor.

### 3.6.2 Diode Conduction Period and Peak Diode Current

Larger values of capacitance provide less ripple and higher average voltage, thereby providing better filter action. From this, one might conclude that to improve the performance of a capacitor filter it is only necessary to increase the size of the filter capacitor. The capacitor, however, also affects the peak current drawn through the rectifying diodes, and as will be shown next, the larger the value of the capacitor, the larger the peak current drawn through the rectifying diodes.

Recall that the diodes conduct during period $T_1$, during which time the diode must provide the necessary average current to charge the capacitor. The shorter this time interval, the larger the amount of the charging current. Figure 3.24 shows this relation for a half-wave rectified signal (it would be the same basic operation for full-wave). Notice that for smaller values of capacitor, with $T_1$ larger, the peak diode current is less than for larger values of filter capacitor.




(a) (b)

Figure 3.24: Capacitor filter output voltage and diode current waveforms for a half-wave rectifier: (a) small $C$, (b) large $C$.

Since the total discharge must equal to total charge, the following relation can be used (assuming constant diode current during charging period):

$$I_{DC}T_2 = I_{\text{peak}}T_1 \tag{3.6.52}$$

$$I_{\text{peak}} = \frac{T_2}{T_1}I_{DC} \tag{3.6.53}$$

where $T_2 \cong T$ for a half-wave rectifier as shown in Figure 3.24 above. Similarly, $T_2 \cong \dfrac{T}{2}$ for a full-wave rectifier.

- Note that $f_{\text{ripple}} = f$ for a half-wave rectifier as seen from Figure 3.24, and $f_{\text{ripple}} = 2f$ for a full-wave rectifier as seen from Figure 3.22.

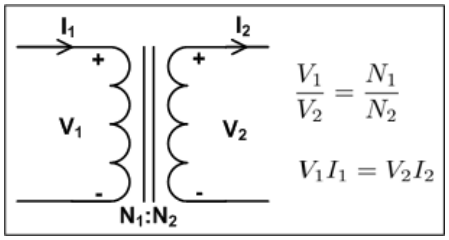
**Example 3.15:** (2004-2005 MI) A power-supply circuit is needed to deliver 0.1 A and an average of 15 V to a load. The AC source available is 230 Vrms with a frequency of 50 Hz. Assume that a **full-wave rectifier** circuit is to be used with a smoothing capacitor in parallel with the load as shown in the figure below. The **peak-to-peak** ripple voltage is to be 0.4 V. Allow $V_{D(ON)} = 0.7\,\text{V}$ for the forward diode voltage drop.

Find

a) The turns-ratio $n = N_1/N_2$ that is needed,

b) The load resistor $R_L$, and

c) The approximate value of the smoothing capacitor $C$.



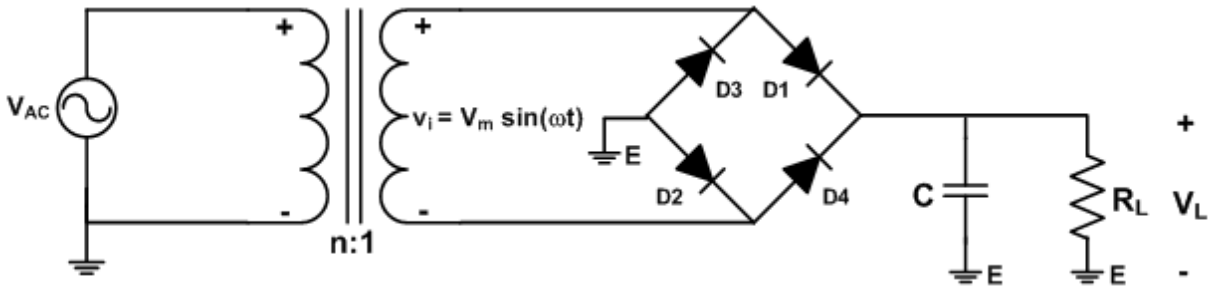




Figure 3.25: Capacitor filter circuit for Example 3.15.

**Solution:** For a full-wave bridge rectifier, DC voltage drop due to the diodes is $2V_{D(ON)}$.

a) As $V_{DC} = 15\,\text{V}$ and $V_{r(\text{p-p})} = 0.4\,\text{V}$, peak value $V_m$ of the AC voltage at the secondary terminal of the transformer is given by

$$V_m = V_{DC} + V_{r(\text{p-p})}/2 + 2V_{D(ON)} = 15 + 0.4/2 + 2(0.7) = 16.6\,\text{V}.$$

Thus the turns ratio $n$ is given by

$$n = \frac{V_{AC(\text{p})}}{V_m} = \frac{\sqrt{2}V_{AC(\text{rms})}}{V_m} = \frac{\sqrt{2}(230)}{16.6} = 19.6.$$

b) As $V_{DC} = 15\,\text{V}$ and $I_{DC} = 0.1\,\text{A}$, $R_L$ is given by

$$R_L = \frac{V_{DC}}{I_{DC}} = \frac{15}{0.1} = 150\,\Omega.$$

c) As $\frac{V_{DC}}{V_{DC}+V_{r(\text{p})}} = \frac{15}{15.2} \cong 1$, then $V_{r(\text{p-p})} \cong \frac{I_{DC}}{f_{\text{ripple}}C}$. So, capacitor $C$ is given by

$$C = \frac{I_{DC}}{f_{\text{ripple}}V_{r(\text{p-p})}} = \frac{I_{DC}}{2fV_{r(\text{p-p})}} = \frac{0.1}{2(50)(0.4)} = 2.5\,\text{mF}.$$

## 3.7 Additional RC Filter

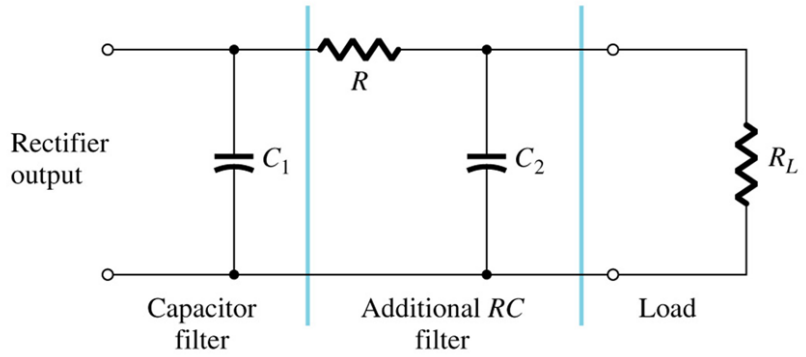



Figure 3.26: Additional $RC$ filter stage.

It is possible to further reduce the amount of ripple across a filter capacitor by using an additional $RC$ filter section as shown in Figure 3.26 above.

The purpose of the added $RC$ section is to pass most of the DC component while attenuating (reducing) as much of the AC component as possible. Figure 3.27 shows a full-wave rectifier with capacitor filter followed by an $RC$ filter section.

Thus, adding an $RC$ section will further reduce the ripple voltage and decrease the surge current through the diodes.

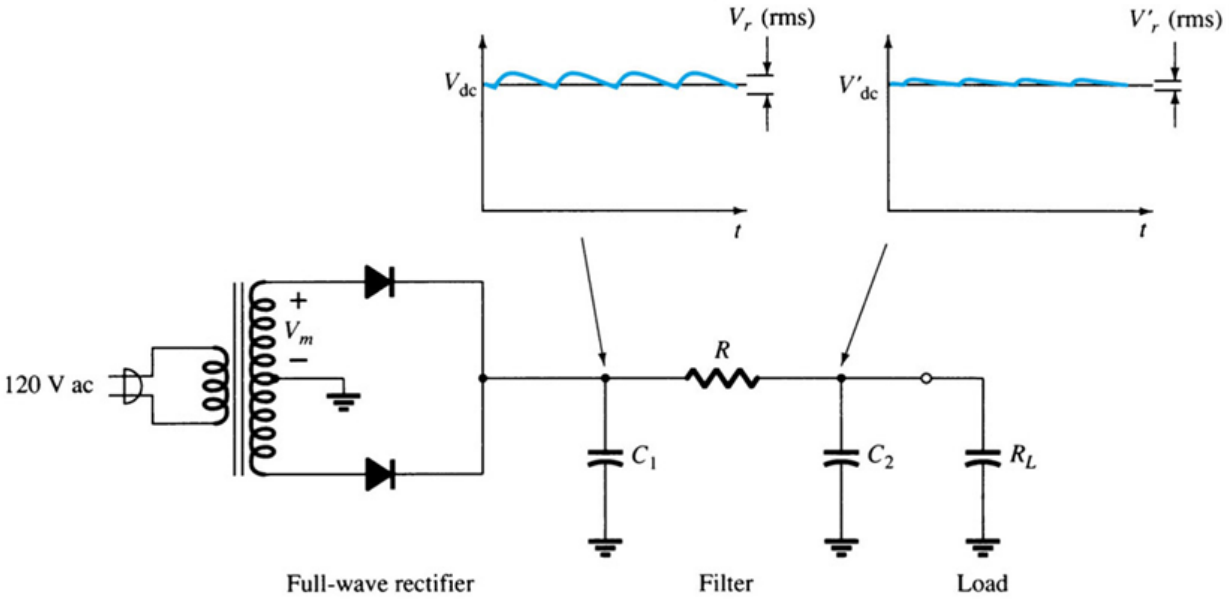



Figure 3.27: Center-tapped transformer full-wave rectifier and RC filter circuit.

As ripple component of the capacitor filter is much smaller than the DC component, the operation of the filter circuit can be analysed using **superposition** for the DC and AC components of signal.

- So, we are going to first use the DC equivalent circuit (i.e., DC analysis) in order to obtain $V'_{DC}$.
- Then, we are going to use the AC equivalent circuit (i.e., AC analysis) in order to obtain $V'_{r(\text{rms})}$.

### 3.7.1 DC Operation

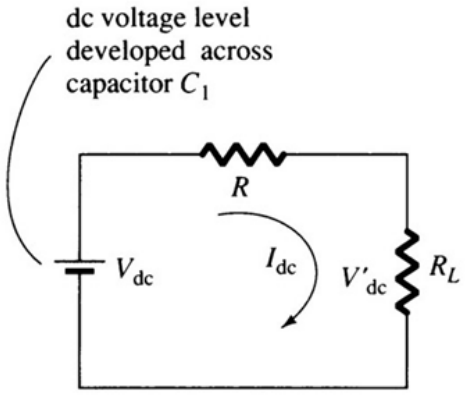



Figure 3.28: DC equivalent circuit of the additional $RC$ filter stage in Figure 3.26.

DC equivalent circuit, where both capacitors are open-circuit for DC operation, of the additional $RC$ filter stage is shown in Figure 3.28 above.

Thus, DC output of the RC filter stage is given by

$$V'_{DC} = \frac{R_L}{R + R_L} V_{DC} \tag{3.7.54}$$

where $V_{DC}$ is the DC output of the capacitor filter.

### 3.7.2 AC Operation

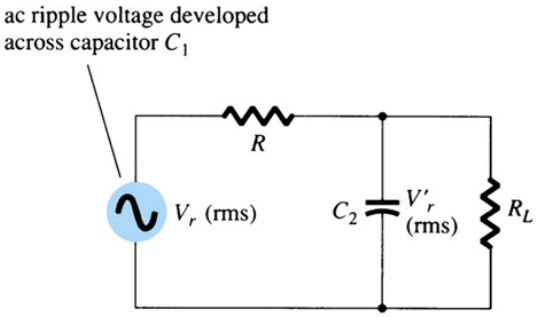



Figure 3.29: AC equivalent circuit of the additional $RC$ filter stage in Figure 3.26.

AC equivalent circuit of the additional $RC$ filter stage is shown in Figure 3.29 above.

So, AC output of the RC filter stage is given by

$$V'_{r(\text{rms})} = \left| \frac{1}{1 + \dfrac{R}{Z'}} \right| V_{r(\text{rms})} \tag{3.7.55}$$

where $Z'$ is the parallel impedance of the capacitor $C_2$ and the load $R_L$, i.e.,

$$Z' = Z_C || R_L \tag{3.7.56}$$

$$|Z'| = \frac{R_L X_C}{\sqrt{R_L^2 + X_C^2}} \tag{3.7.57}$$

and $Z_C = -jX_C$ with $X_C = \dfrac{1}{\omega C_2}$ and $\omega = 2\pi f_{\text{ripple}}$.

**Simplification**

- If $R_L \gg X_C$, e.g., $R_L \geq 5X_C$, then $|Z'| \cong X_C$.

  Consequently, $V'_{r(\text{rms})}$ could be written as

$$\boxed{V'_{r(\text{rms})} \cong \frac{1}{\sqrt{1 + \dfrac{R^2}{X_C^2}}} V_{r(\text{rms})} = \frac{X_C}{\sqrt{R^2 + X_C^2}} V_{r(\text{rms})}} \tag{3.7.58}$$

- Additionally if $\dfrac{R^2}{X_C^2} \gg 1$, then the above expression further reduces to

$$V'_{r(\text{rms})} \approx \frac{X_C}{R} V_{r(\text{rms})} \tag{3.7.59}$$

**Example 3.16:** Consider the circuit below with $f_{\text{ripple}} = 50\,\text{Hz}$, $C_2 = 10\,\mu\text{F}$ and $R_L = 2\,\text{k}\Omega$, and calculate $X_{C_2}$ and $|Z_{C_2}||R_L|$.

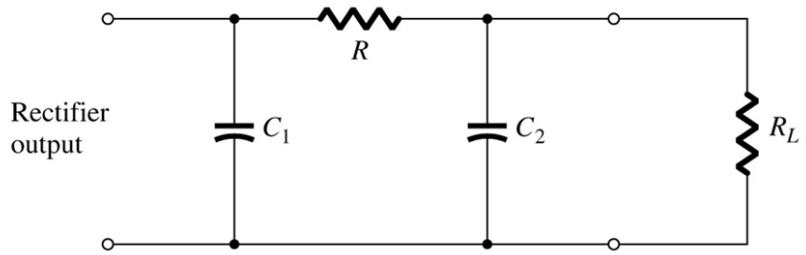



Figure 3.30: Capacitor filter circuit for Example 3.16.

**Solution:** Let us calculate $X_C$ and $|Z'|$ where $X_C = X_{C_2}$ and $Z' = Z_{C_2}||R_L$

$$X_C = \frac{1}{2\pi f_{\text{ripple}} C_2} = \frac{1}{2\pi(50)(10\mu)} = 318\,\Omega,$$

$$|Z'| = \frac{R_L X_C}{\sqrt{R_L^2 + X_C^2}} = \frac{(2k)(318)}{\sqrt{(2k)^2 + (318)^2}} = 314\,\Omega.$$

Thus, the assumption $|Z'| \cong X_C$ holds when $R_L \geq 5X_C$.

**Example 3.17:** Consider the circuit in Figure 3.31 below with $f_{\text{mains}} = 50\,\text{Hz}$.

a) Find the DC and AC voltages over the load,

b) Find the ripple factors, $\%r$ and $\%r'$ values,

c) Find the voltage regulation factor %VR.

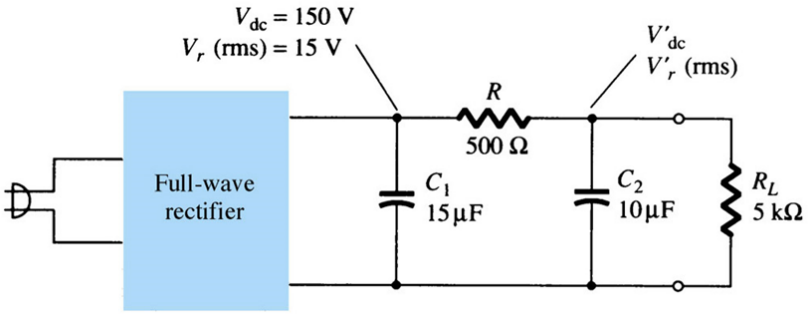



Figure 3.31: Capacitor filter circuit for Example 3.17.

**Solution:** As a full-wave rectifier is used $f_{\text{ripple}} = 2f_{\text{mains}} = 100\,\text{Hz}$.

a) Let us find $V'_{DC}$ first

$$V'_{DC} = \frac{R_L}{R + R_L} V_{DC} = \frac{5k}{0.5k + 5k} 150 = 136.4\,\text{V}.$$

We see that DC voltage value dropped by 13.6 V.

Now, let us find $X_C$

$$X_C = \frac{1}{2\pi f_{\text{ripple}} C_2} = \frac{1}{2\pi(100)(10\mu)} = 159\,\Omega$$

As $R_L \gg X_C$,

$$V'_{r(\text{rms})} = \frac{X_C}{\sqrt{R^2 + X_C^2}} V_{r(\text{rms})} = \frac{159}{\sqrt{500^2 + 159^2}} 15 = 4.55\,\text{V}$$

We see that ripple voltage reduced by a factor of 3.3 times.

b) Ripple factors before $\%r$ and after $\%r'$ are given by

$$\%r = \frac{V_{r(\text{rms})}}{V_{DC}} \times 100 = \frac{15}{150} \times 100 = 10\%$$
$$\%r' = \frac{V'_{r(\text{rms})}}{V'_{DC}} \times 100 = \frac{4.55}{136.4} \times 100 = 3.34\%$$

We see that ripple factor reduced by a factor of 3 times.

c) Voltage regulation %VR is given by

$$\%\text{VR} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{150 - 136.4}{136.4} \times 100 = 9.97\%.$$

- If we want the DC voltage drop to be smaller but AC ripple drop to be higher, we can achieve it by replacing the resistor $R$ with a component such that its DC resistance is small while its AC resistance is high. Such a component is an **inductor**.

## 3.8 $\pi$-Filter

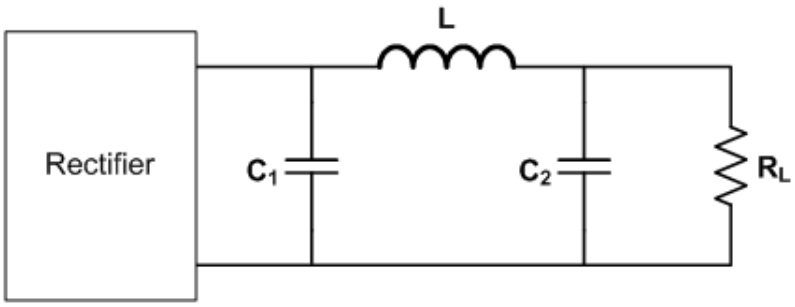



Figure 3.32: $\pi$-filter stage.

By replacing resistor $R$ in the $RC$ filter with inductor $L$, we obtain a $\pi$-filter as shown in Figure 3.32 above.

While DC resistance $R_\ell$ of the coil is small and is AC reactance $X_L$ is high.

**Example 3.18:** For the $\pi$-filter shown in Figure 3.32, the output DC voltage and current are given as 200 V and 50 mA. Also $V_{DC(C_1)} = 210\,\text{V}$, $V_{r(C_1)} = 12\,\text{Vrms}$ and the frequency of the ripple voltage $f_{\text{ripple}} = 100\,\text{Hz}$. In order to satisfy $r' \leq 2\%$, determine the values of $R_L$, $R_\ell$, $L$ and $C_2$. Explain any assumptions you make. NOTE: $R_\ell$ denotes the DC resistance of the coil.

**Solution:** As $V'_{DC} = 200\,\text{V}$ and $I'_{DC} = 50\,\text{mA}$, the load $R_L$ is given by

$$R_L = V'_{DC}/I'_{DC} = 200/50m = 4\,\text{k}\Omega.$$

We know that $V'_{DC} = \frac{R_L}{R_\ell + R_L} V_{DC}$, so $R_\ell$ is given by

$$R_\ell = (V_{DC} - V'_{DC})R_L/V'_{DC} = (210 - 200)/200 = 200\,\Omega.$$

Let us find the ripple voltage requirement as $V'_{r(\text{rms})} \leq (2\%)V'_{DC} = (2\%)(200) = 4\,\text{Vrms}$

$$V'_{r(\text{rms})} \leq 4\,\text{Vrms}.$$

Let us select $X_C \ll R_L$ as $X_C = R_L/10 = 4k/10 = 400\,\Omega$.

Note that $Z_L = R_\ell + jX_L$, and assuming $X_L \gg R_\ell$ we will take $Z_L \cong jX_L$.

We know that $\dfrac{X_L - X_C}{X_C} \geq \dfrac{V_{r(\text{rms})}}{V'_{r(\text{rms})}} = \dfrac{12}{4} = 3$, so $X_L$ is given by

$$X_L \geq 4X_C = (4)(400) = 1.6\,\text{k}\Omega$$

So, let us select $X_L = 1.7\text{k}\Omega$ and find the value of inductance $L$ as follows

$$L = \frac{X_L}{\omega} = \frac{X_L}{2\pi f_{\text{ripple}}} = \frac{1.7k}{2\pi(100)} = 2.7\,\text{H}.$$

As $X_C = 400\,\Omega$, we can find the value of capacitance $C$ as follows

$$C = \frac{1}{\omega X_C} = \frac{1}{2\pi f_{\text{ripple}} X_C} = \frac{1}{2\pi(100)(400)} = 4\,\mu\text{F}.$$

# Chapter 4

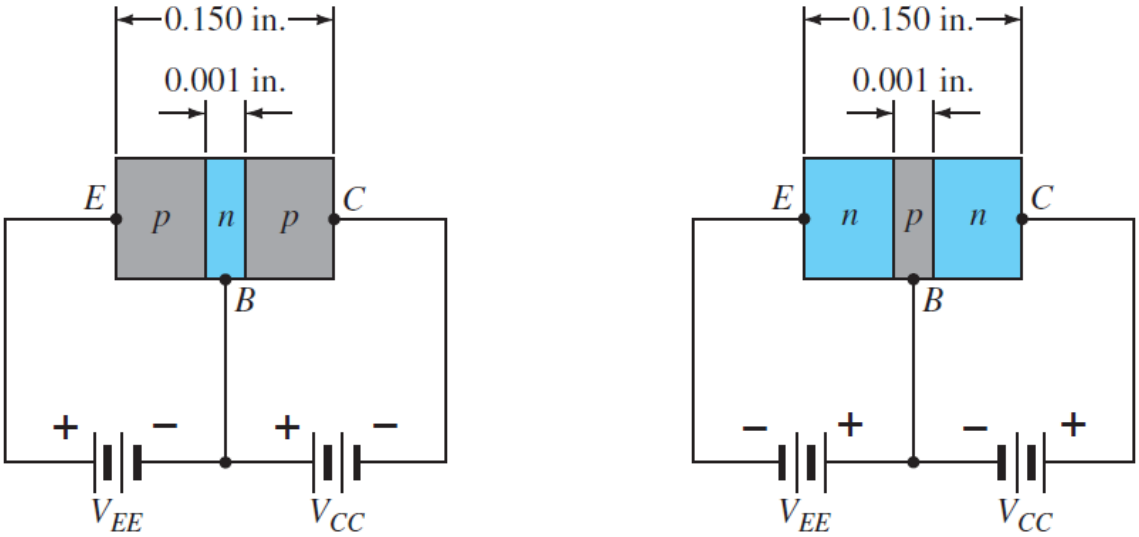
# Bipolar Junction Transistor (BJT)

## 4.1 Bipolar Junction Transistor

**Bipolar junction transistor** (BJT) is a three-layer semiconductor device consisting of either two $n$- and one $p$-type layers of material or two $p$- and one $n$-type layers of material. The former is called an *npn* transistor, and the latter is called a *pnp* transistor. Both are shown in Figure 4.1 below with the proper DC biasing.

The terminals have been indicated by the capital letters $E$ for **emitter**, $C$ for **collector**, and $B$ for **base**. Emitter is the source of the majority carriers (electrons in an *npn* transistor and holes in a *pnp* transistor). In simple wording, majority carriers are emitted from the emitter and collected by the collector.

The term **bipolar** reflects the fact that holes and electrons participate in the current conduction process.

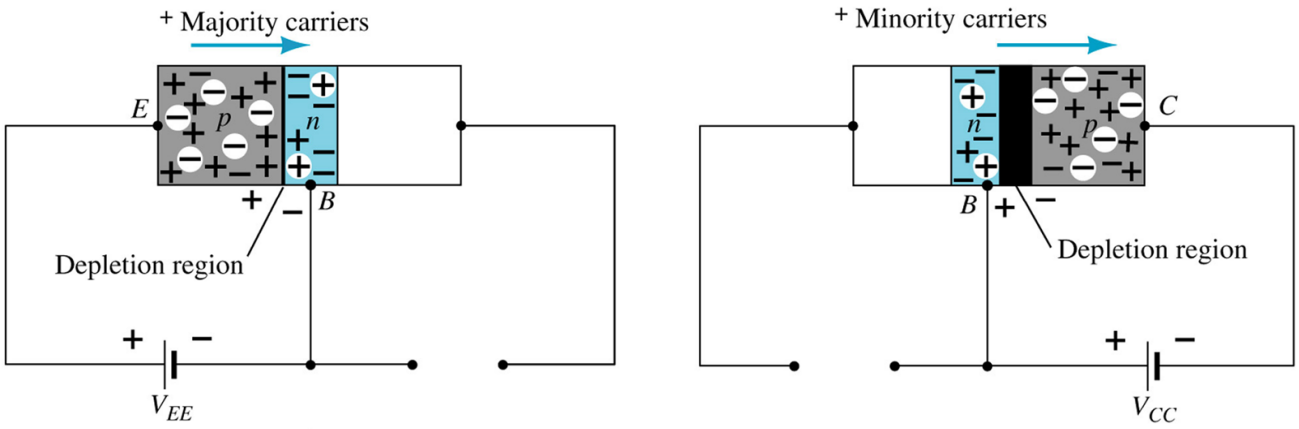



(a) (b)

Figure 4.1: Types of transistors: (a) *pnp*, (b) *npn*.

The basic operation of the transistor will now be described using the *pnp* transistor. The operation of the *npn* transistor is exactly the same if the roles played by the electron and hole are interchanged. In Figure 4.2(a) below *pnp* transistor has been redrawn by removing the bias of base-collector junction (keeping base-emitter junction forward-biased). The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of **majority carriers** from emitter to base (i.e., **holes** from **emitter** to **base**).

Let us now remove the bias of base-emitter junction (keeping base-collector junction reverse-biased) as shown in Figure 4.2(b) below. Recall that the flow of majority carriers (electrons from base to collector) is zero, resulting in only a **minority-carrier** flow (i.e., **holes** from **base** to **collector**).




(a) (b)

Figure 4.2: Biasing a transistor: (a) base-emitter forward-biased, (b) base-collector reverse-biased.

Once the **base-emitter** junction is **forward-biased**, and **base-collector** junction **reverse-biased** at the same time.

Then, most of the **holes** (majority carriers of the emitter region) coming from emitter region to the base region are **swept away** to the collector region as holes are the minority carriers for the base region and base-collector junction is reverse biased.

This basic transistor operation is shown in Figure 4.3 below as

$$\boxed{I_E = I_C + I_B} \tag{4.1.1}$$

where collector current $I_C$ is comprised of two components

$$I_C = I_{C(\text{majority})} + I_{CO(\text{minority})} \cong I_{C(\text{majority})} \tag{4.1.2}$$

Here, the minority-current component is called the **leakage current** with the symbol $I_{CO}$ (reverse-bias $I_C$ current with emitter terminal open). Generally $I_C$ is measured in milliamperes and $I_{CO}$ is measured in microamperes or nanoamperes. $I_{CO}$, like $I_s$ for a reverse-biased diode, is temperature sensitive and must be examined carefully when applications of wide temperature ranges are considered.

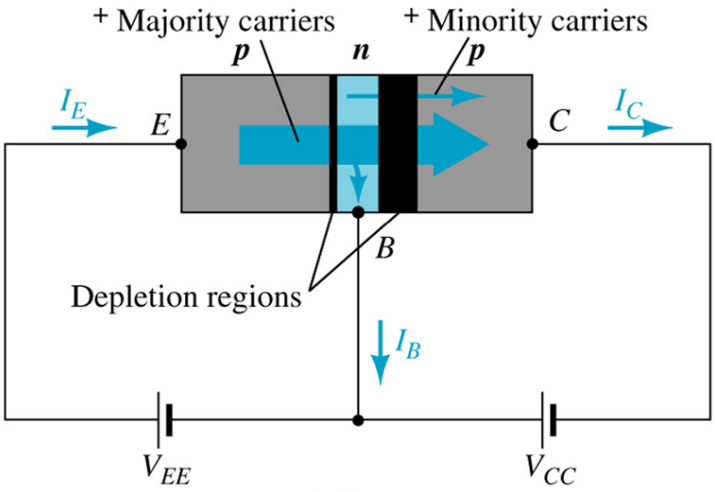



Figure 4.3: Current flow in a properly biased *pnp* transistor.

## 4.2 Common-Base Configuration

The common-base terminology is derived from the fact that the **base** is **common** to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential.

On the BJT **circuit symbol**, an **arrow** is always drawn at the **emitter** leg of the transistor as shown in Figures 4.4(a) and 4.4(b) below in the **forward direction** of the base-emitter *pn* junction like the diode symbol. Hence, from the direction of the arrow we can determine type of the transistor, i.e., *npn* or *pnp*.

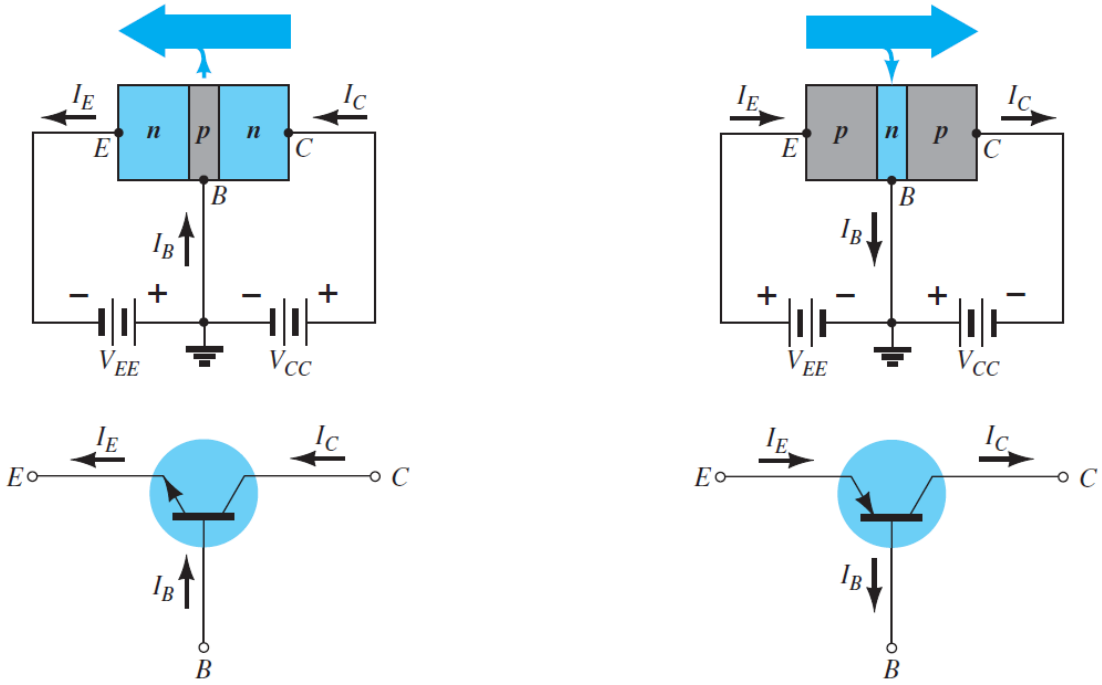


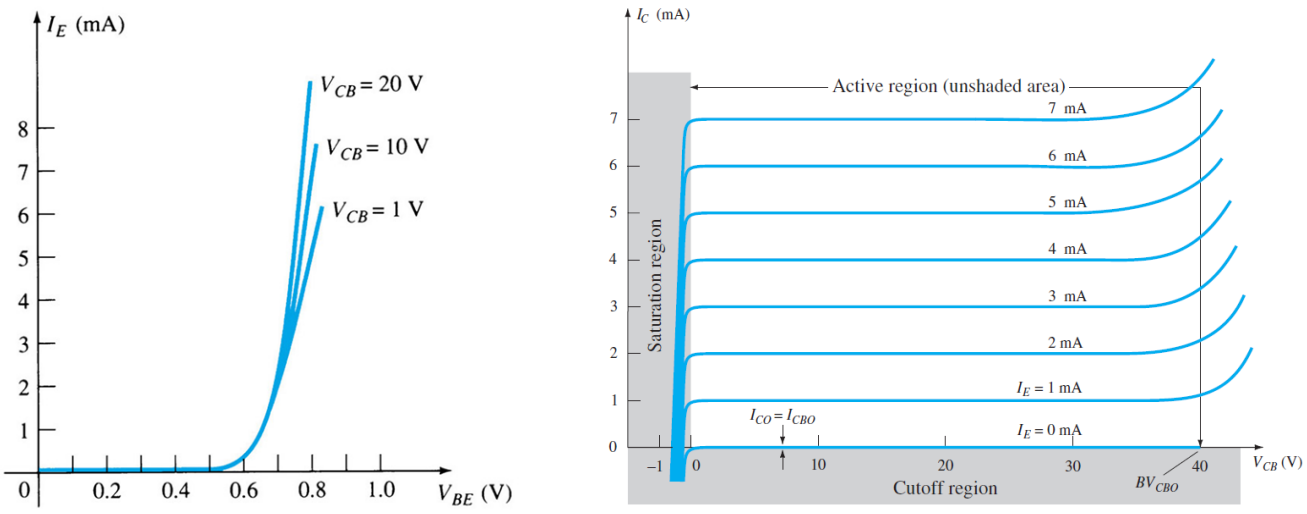

Figure 4.4: Notation and symbols used with the common-base configuration: (a) *npn* transistor, (b) *pnp* transistor.

### 4.2.1 Input and Output Characteristics

To fully describe the behavior of a three-terminal device requires two sets of characteristics—one for the input parameters and the other for the output side.

The input set for the common-base amplifier relates an input current ($I_E$) to an input voltage ($V_{BE}$) for various levels of output voltage ($V_{CB}$) as shown in Figure 4.5(a) below.

The output set relates an output current ($I_C$) to an output voltage ($V_{CB}$) for various levels of input current ($I_E$) as shown in Figure 4.5(b) below. The output set of characteristics has three basic regions of interest, the **active**, **cutoff**, and **saturation** regions. The active region is the region normally employed for linear amplifiers.




(a) (b)

Figure 4.5: Characteristics of an *npn* common-base amplifier: a) Input characteristics, b) Output characteristics.

### 4.2.2 Three Modes of Operation

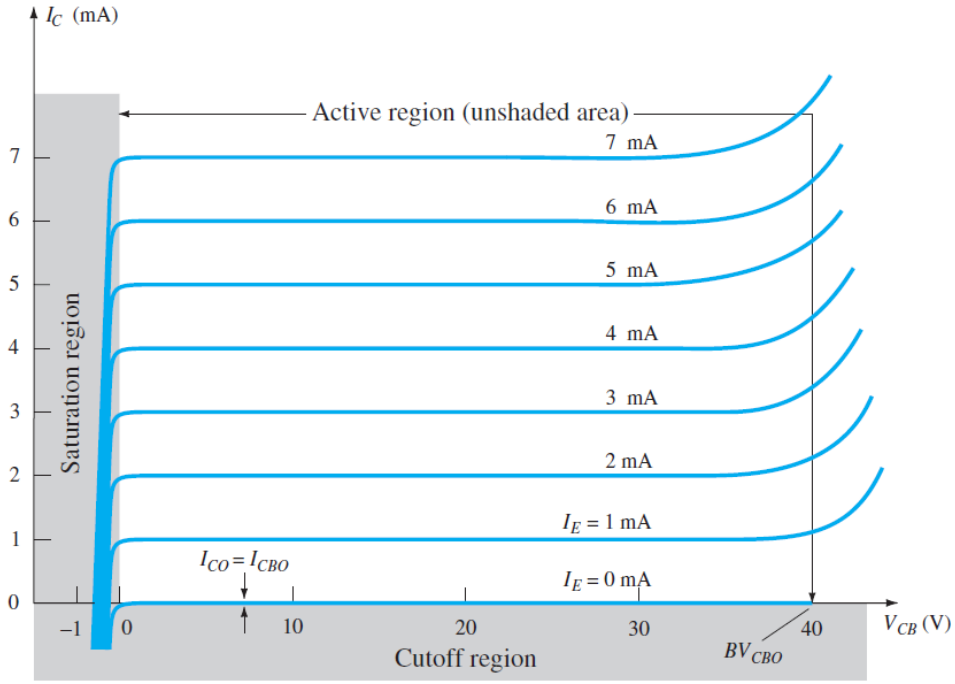



Figure 4.6: Output characteristics of a common-base amplifier.

- **Cut-Off:** The amplifier is basically off: $I_E = 0\,\text{A}$, $I_C = I_{CBO} \cong 0\,\text{A}$ and $I_B \cong 0\,\text{A}$.
  - Base-Emitter junction: **reverse-biased**, i.e., OFF.
  - Base-Collector junction: **reverse-biased**, i.e., OFF.
- **Active:** *Operating region of the amplifier*: $I_C \cong I_E$ and $V_{BE} \cong V_{BE(ON)}$.

- Base-Emitter junction: **forward-biased**, i.e., ON.
- Base-Collector junction: **reverse-biased**, i.e., OFF.

- **Saturation:** The amplifier is saturated: $I_C = I_{C(sat)}$ and $V_{CE} = V_{CE(sat)} \cong 0\,\text{V}$.
  - Base-Emitter junction: **forward-biased**, i.e., ON.
  - Base-Collector junction: **forward-biased**, i.e., ON.

### 4.2.3 Currents

- For any mode (or state) of the transistor and for any configuration, emitter current is **always** the **sum** of the base and collector currents, i.e.,

$$\boxed{I_E = I_C + I_B} \tag{4.2.3}$$

- Note that, collector current $I_C$ is comprised of majority and minority carrier current components

$$I_C = I_{C(\text{majority})} + I_{C(\text{minority})} = I_{C(\text{majority})} + I_{CO} \cong I_{C(\text{majority})} \tag{4.2.4}$$

where $I_{CO}$ is called the reverse saturation current (or leakage current). The notation most frequently used for $I_{CO}$ in data and specification sheets is $I_{CBO}$ (the collector-to-base current with the emitter leg open) as shown in Figure 4.7 below.

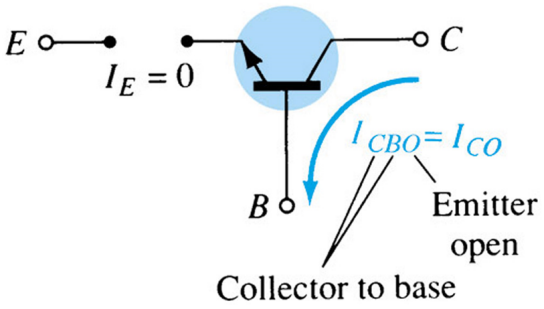



Figure 4.7: Common-base cutoff current (or reverse saturation current), $I_{CBO}$.

### 4.2.4 Alpha ($\alpha$)

- In the active mode the DC levels of $I_C$ and $I_E$ due to the majority carriers are related by a quantity called alpha ($\alpha_{DC}$), i.e., $I_{C(\text{majority})} = \alpha_{DC} I_E$. However, as $I_{CBO}$ is very small we define $\alpha_{DC}$ as

$$\boxed{\alpha_{DC} = \frac{I_C}{I_E}.} \tag{4.2.5}$$

In the specification sheets, $\alpha_{DC}$ is expressed as $h_{FB}$ which is the static forward current transfer ratio.

- For AC situations where the point of operation moves on the characteristic curve, an AC alpha ($\alpha_{ac}$) is defined by

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}} = \left.\frac{\partial I_C}{\partial I_E}\right|_{Q\text{-point}} \tag{4.2.6}$$

  In the specification sheets, $\alpha_{ac}$ is expressed as $h_{fb}$ which is the small signal forward current transfer ratio.

- For most situations the magnitudes of $\alpha_{ac}$ and $\alpha_{DC}$ are quite close,permitting the use of the magnitude of one for the other, i.e.,

$$\boxed{\alpha = \alpha_{ac} = \alpha_{DC} \cong 1.} \tag{4.2.7}$$

  Ideally $\alpha = 1$, but in reality it lies between 0.9 and 0.998.

### 4.2.5 Simplification (Active Mode)

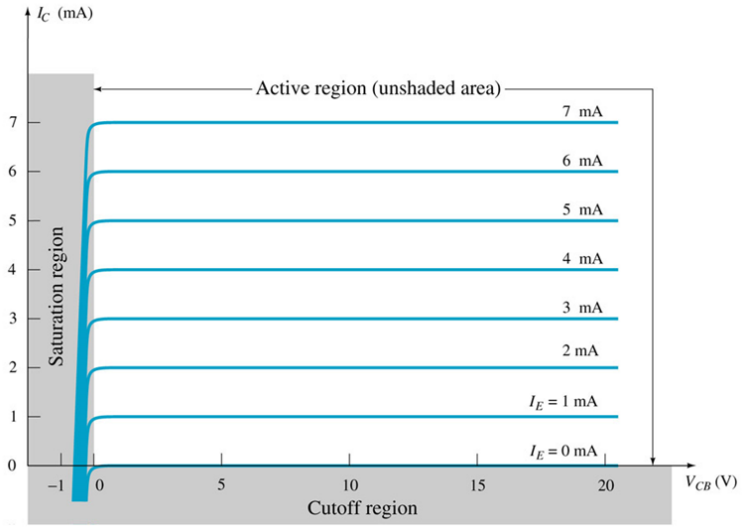



Figure 4.8: Simplified output characteristics of a common-base amplifier.

- As we see from Figure 4.8 above,

$$I_C \cong I_E \tag{4.2.8}$$

  i.e., $\alpha \cong 1$

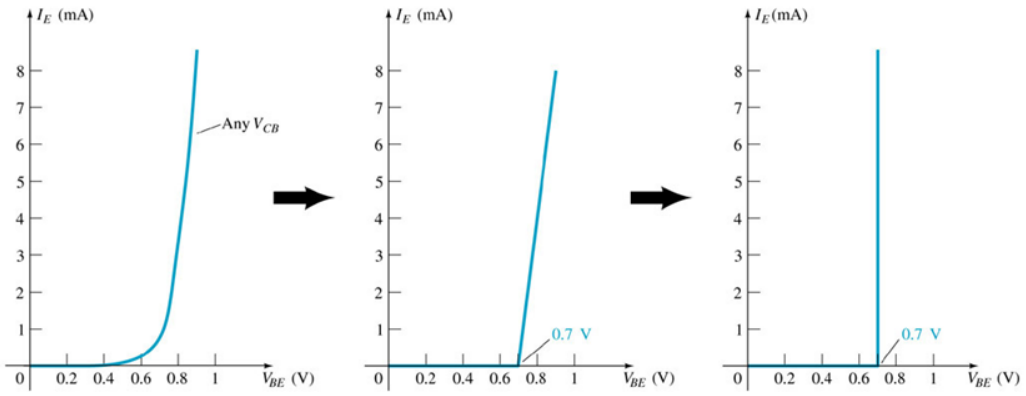



Figure 4.9: Simplified input characteristics of a common-base amplifier.

- As we see from Figure 4.9 above,

$$V_{BE} \cong V_{BE(ON)} = 0.7\,\text{V}. \tag{4.2.9}$$

### 4.2.6 AC Amplification

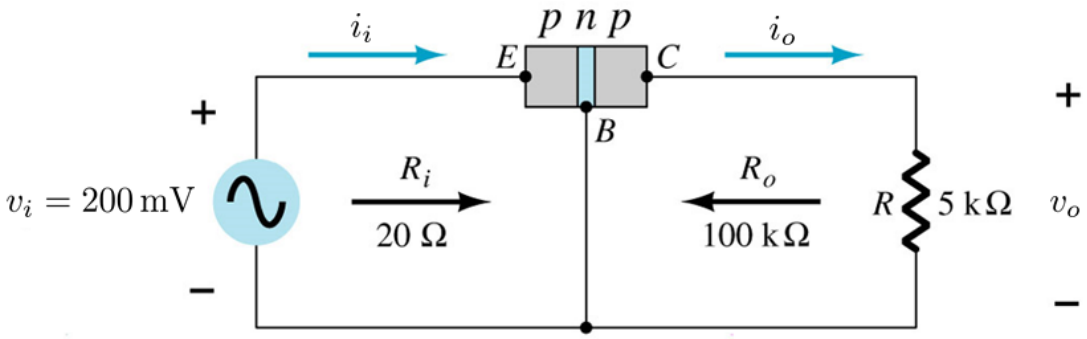



Figure 4.10: AC equivalent circuit of a common-base amplifier.

**Example 4.1:** For Figure 4.10 above, find output $v_o$ and voltage gain $A_v$.

**Solution:** Let us first find $i_i = i_e$ as,

$$i_i = i_e = \frac{v_i}{R_i} = \frac{200\,\text{mV}}{20\,\Omega} = 10\,\text{mA}.$$

As $\alpha_{ac} \cong 1$, $i_c \cong i_e = 10\,\text{mA}$. Thus, $i_o = \frac{R_o}{R_o+R} i_c = \frac{100k}{100k+5k} i_c \cong i_c = 10\,\text{mA}$.

Consequently, output voltage $v_o$ and voltage gain $A_v$ are given by

$$v_o = i_o R = (10\,\text{mA})(5\,\text{k}\Omega) = 50\,\text{V},$$
$$A_v = \frac{v_o}{v_i} = \frac{50\,\text{V}}{200\,\text{mV}} = 250.$$

## 4.3 Common-Emitter Configuration

The common-emitter terminology is derived from the fact that the **emitter** is **common** to both the input and output sides of the configuration. In addition, the emitter is usually the terminal closest to, or at, ground potential.

On the BJT **circuit symbol**, an **arrow** is always drawn at the **emitter** leg of the transistor as shown in Figures 4.11(a) and 4.11(b) below in the **forward direction** of the base-emitter *pn* junction like the diode symbol. Hence, from the direction of the arrow we can determine type of the transistor, i.e., *npn* or *pnp*.

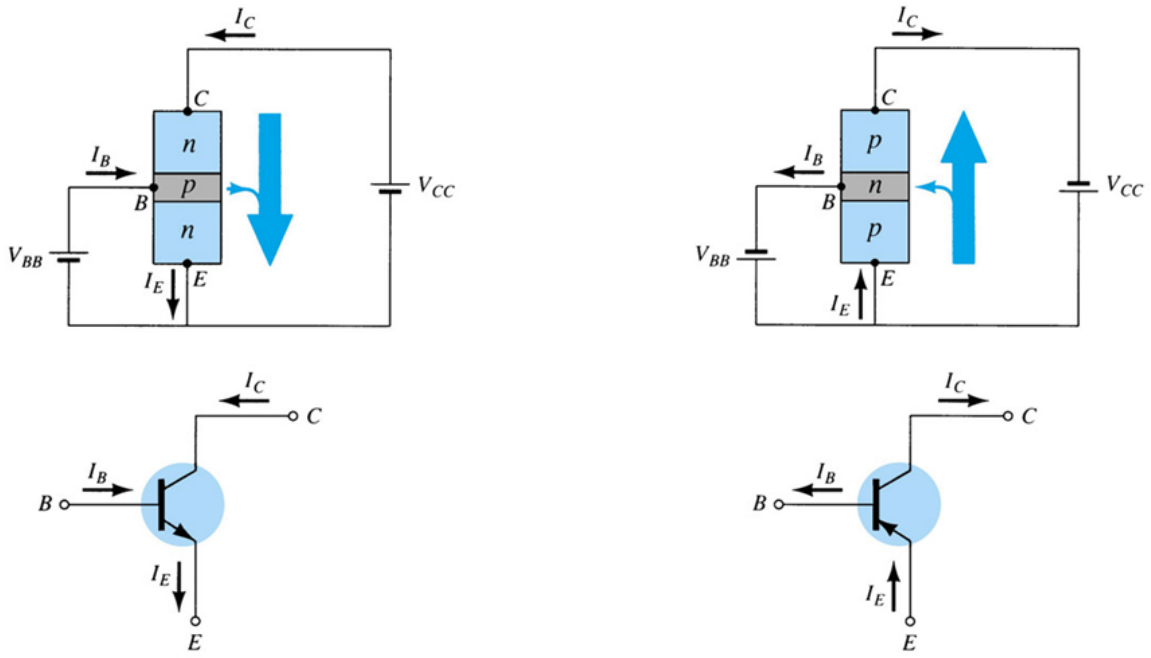
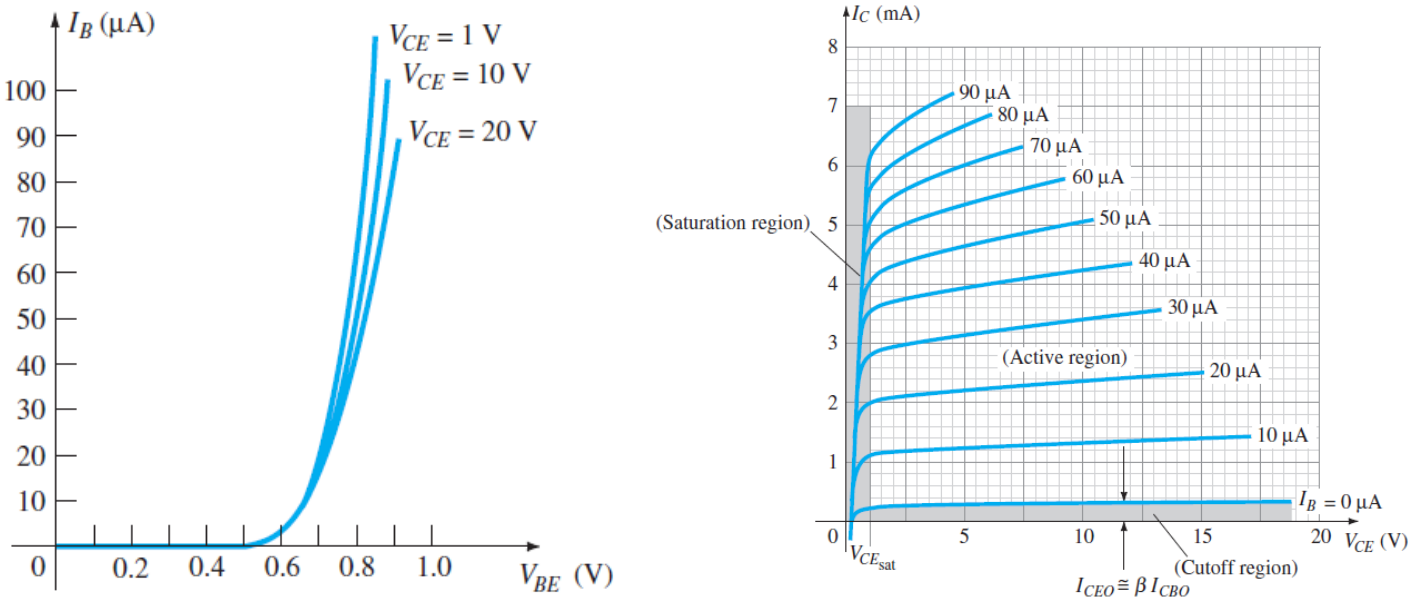



Figure 4.11: Notation and symbols used with the common-emitter configuration: (a) *npn* transistor, (b) *pnp* transistor.

### 4.3.1 Input and Output Characteristics

The input set for the common-emitter amplifier relates an input current ($I_B$) to an input voltage ($V_{BE}$) for various levels of output voltage ($V_{BC}$) as shown in Figure 4.12(a) below.

The output set relates an output current ($I_C$) to an output voltage ($V_{CE}$) for various levels of input current ($I_B$) as shown in Figure 4.12(b) below. The output set of characteristics has three basic regions of interest, the **active**, **cutoff**, and **saturation** regions. The active region is the region normally employed for linear amplifiers.




(a) (b)

Figure 4.12: Characteristics of an *npn* common-emitter amplifier: a) Input characteristics, b) Output characteristics.

### 4.3.2 Currents

Collector current $I_C$ is given by $I_C = \alpha I_E + I_{CBO}$ where $I_E = I_C + I_B$. So,

$$I_C = \alpha I_E + I_{CBO} \tag{4.3.10}$$
$$= \alpha (I_C + I_B) + I_{CBO} \tag{4.3.11}$$
$$= \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \tag{4.3.12}$$
$$= \beta I_B + I_{CEO} \tag{4.3.13}$$
$$\cong \beta I_B \tag{4.3.14}$$

where $I_{CEO}$ is the common-emitter cutoff current (or the collector-to-emitter current with the base leg open) as shown in Figure 4.13 below and defined by

$$\boxed{I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B = 0\,\text{A}} = (\beta + 1)\, I_{CBO}} \tag{4.3.15}$$

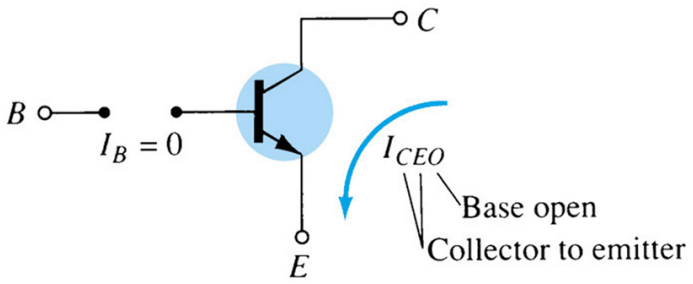



Figure 4.13: Common-emitter cutoff current, $I_{CEO}$.

### 4.3.3 Beta ($\beta$)

- In the active mode, the DC levels of $I_C$ and $I_B$ are related by a quantity called beta ($\beta_{DC}$). However, as $I_{CEO}$ is very small, we define $\beta_{DC}$ as

$$\boxed{\beta_{DC} = \frac{I_C}{I_B}.} \tag{4.3.16}$$

  In the specification sheets, $\beta_{DC}$ is expressed as $h_{FE}$ which is the static forward current gain.

- For AC situations where the point of operation moves on the characteristic curve, an AC beta ($\beta_{ac}$) is defined by

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = \left.\frac{\partial I_C}{\partial I_B}\right|_{Q\text{-point}} \tag{4.3.17}$$

  In the specification sheets, $\beta_{ac}$ is expressed as $h_{fe}$ which is the small signal forward current gain.

- For most situations the magnitudes of $\beta_{ac}$ and $\beta_{DC}$ are quite close,permitting the use of the magnitude of one for the other, i.e.,

$$\boxed{\beta = \beta_{ac} = \beta_{DC}} \tag{4.3.18}$$

#### 4.3.3.1 Determining $\beta$ from a graph

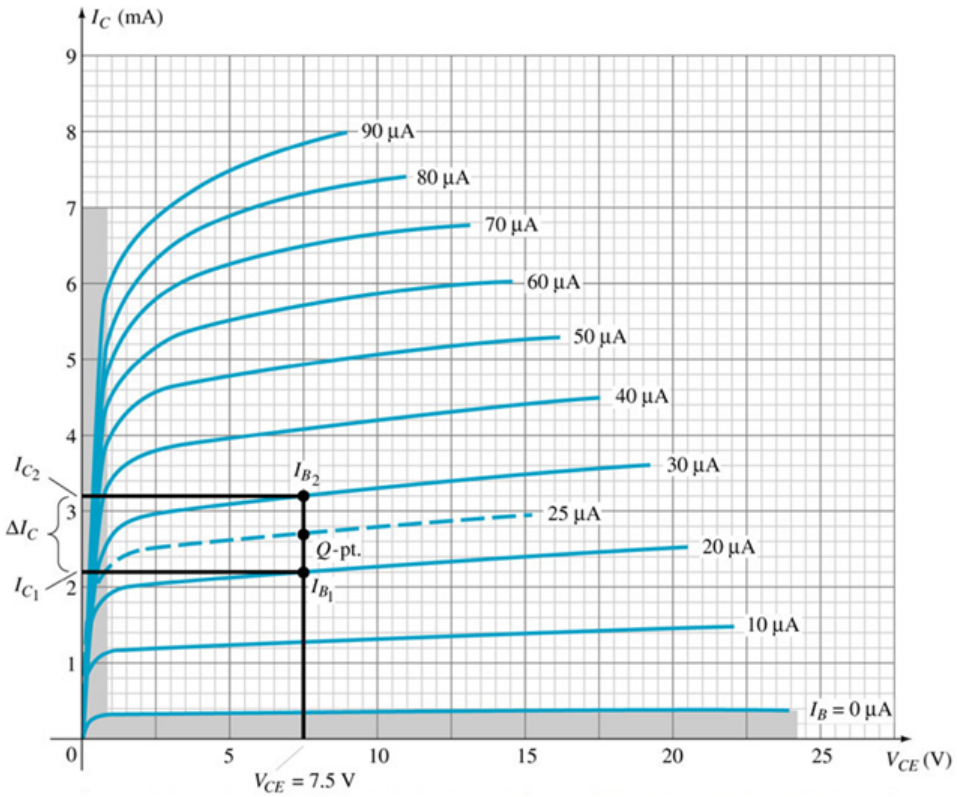



Figure 4.14: Determining $\beta_{DC}$ and $\beta_{ac}$ from the output characteristics.

**Example 4.2:** From Figure 4.14 above, determine $\beta_{DC}$ and $\beta_{ac}$.

**Solution:** Reading the values at $Q$-point, i.e., at $V_{CEQ} = 7.5\,\text{V}$, from the figure above, $\beta_{DC}$ and $\beta_{ac}$ are given by

$$\beta_{DC} = \frac{I_{CQ}}{I_{BQ}} = \frac{2.7\,\text{mA}}{25\,\mu\text{A}} = 108$$
$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{Q\text{-point}} = \frac{3.2\,\text{mA} - 2.2\,\text{mA}}{30\,\mu\text{A} - 20\,\mu\text{A}} = 100$$

We see that $\beta_{ac} \cong \beta_{DC}$.

### 4.3.4 Relationship between $\beta$ and $\alpha$

- As we derived before, $\beta$ is given by

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \tag{4.3.19}$$

- Similarly, $\alpha$ is given by

$$\boxed{\alpha = \frac{\beta}{\beta+1}} \tag{4.3.20}$$

### 4.3.5 Simplification (Active Mode)

**Simplification (Active Mode)**

- In the active mode, collector and emitter currents $I_C$ and $I_E$ are given by

$$I_C = \beta I_B \tag{4.3.21}$$
$$I_E = (\beta+1)\, I_B \qquad \ldots \text{as } I_E = I_C + I_B \tag{4.3.22}$$

- Base-emitter junction is also ON. So,

$$V_{BE} \cong V_{BE(ON)} = 0.7\,\text{V}. \tag{4.3.23}$$

## 4.4 Common-Collector Configuration

The common-collector terminology is derived from the fact that the **collector** is **common** to both the input and output sides of the configuration. In addition, the collector is usually the terminal closest to, or at, ground potential.

Input and output characteristics are similar to those of the common-emitter amplifier, except the output current is the emitter current $I_E$ instead of the collector current $I_C$.

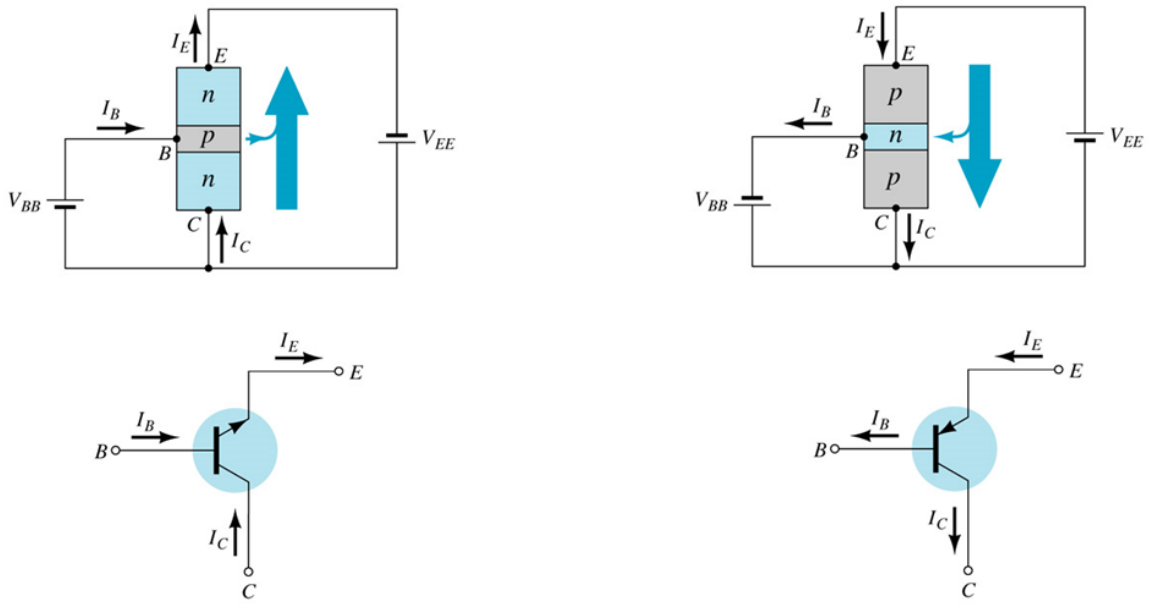



Figure 4.15: Notation and symbols used with the common-collector configuration: (a) *npn* transistor, (b) *pnp* transistor.

## 4.5 Operating Limits

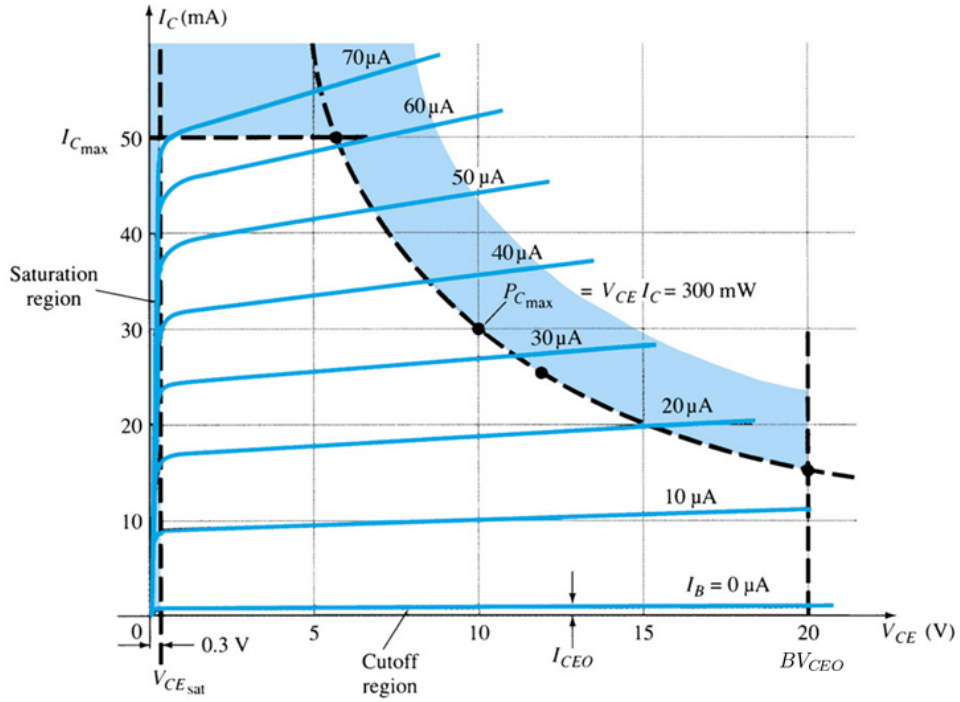



Figure 4.16: Defining the region of operation for a transistor.

The figure above shows the limitations for the linear region of a common-emitter configuration:

1. Maximum and minimum $CE$ voltages: $BV_{CEO}$ and $V_{CE(\text{sat})}$. Maximum collector-to-emitter voltage is often abbreviated as $BV_{CEO}$ or $V_{(BR)CEO}$ in the specification sheets.
2. Maximum and minimum collector current: $I_{C(\max)}$ and $I_{CEO}$.
3. Maximum power curve: $P_{C(\max)}$.

- Design operating point ($Q$-point) to be in the middle of the linear region (white region).

  Note that maximum power curves in different configurations are given below

  a) Common-Base: $V_{CB}I_C = P_{C(\max)}$.
  b) Common-Emitter: $V_{CE}I_C = P_{C(\max)}$.
  c) Common-Collector: $V_{CE}I_E = P_{C(\max)}$.

- An example BJT packaging is shown in Figure 4.17 below.

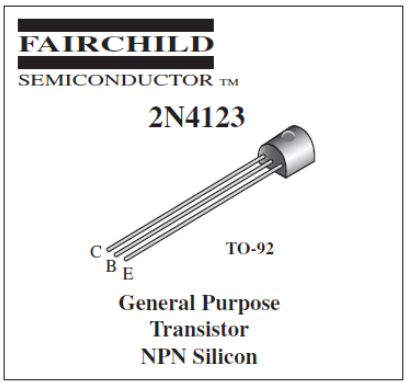
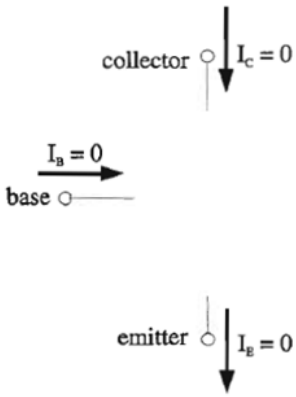



Figure 4.17: An example BJT packaging.

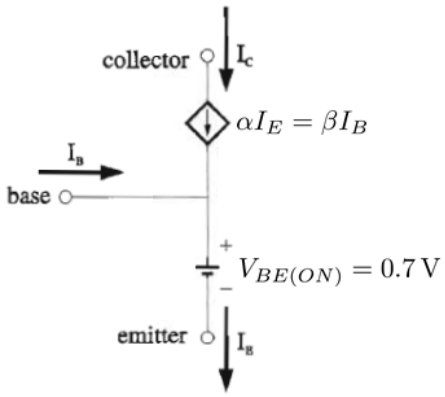
## 4.6 Simplified BJT Model

We can summarize the simplified *npn* BJT model with its state and circuit behaviour with the table below and in Figure 4.18.

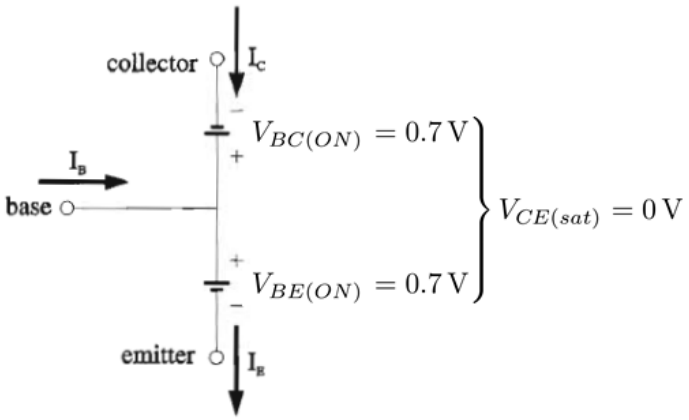
| **Simplified *npn* BJT Model** | | |
|---|---|---|
| **State** | **Circuit Behaviour** | **Test Condition** |
| CUTOFF | $I_B = 0$,<br>$I_C = 0,\ I_E = 0$ | $V_{BE} < V_{BE(ON)}$,<br>$V_{BC} < V_{BC(ON)}$ |
| ACTIVE | $V_{BE} = V_{BE(ON)}$,<br>$I_C = \beta I_B$ | $I_B \geq 0$,<br>$V_{CE} > V_{CE(sat)}$ |
| SATURATION | $V_{BE} = V_{BE(ON)}$,<br>$V_{CE} = V_{CE(sat)}$ | $I_B \geq 0$,<br>$I_C < \beta I_B$ |




(a) Cutoff




(b) Active




(c) Saturation

Figure 4.18: States of the simplified *npn* BJT model: (a) Cutoff, (b) Active, (c) Saturation

- For a *pnp* BJT transistor, the **polarities** and **directions** are simply **reversed**.

  For example, the device will be ON (e.g., in ACTIVE mode) when $V_{EB} \geq V_{BE(ON)}$.

# Chapter 5

# DC Biasing of BJTs

## 5.1 DC Biasing

Biasing refers to the DC voltages applied to the transistor to put it into **active mode**, so that it can amplify the AC signal.

The DC input establishes an **operating point** or quiescent point called the ***Q*-point**.

Proper DC biasing should try to set the $Q$-point towards the middle of active region, e.g., Point $B$ in Figure 5.1 below.

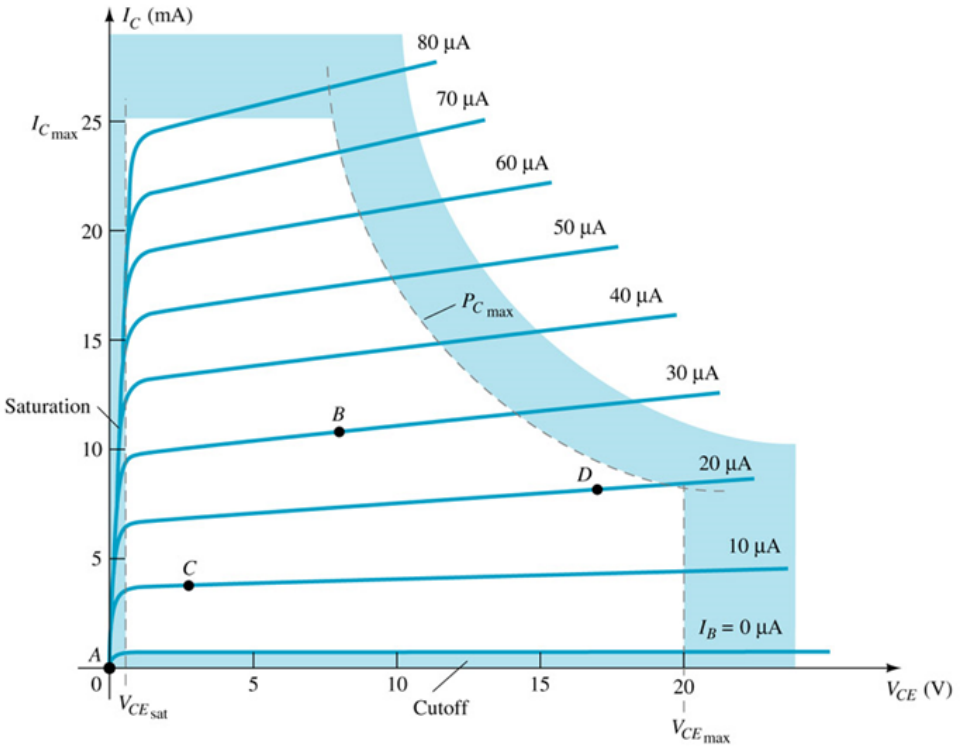



Figure 5.1: Various operating points within the limits of operation of a BJT transistor.

## 5.2 Three States of Operation

Proper DC biasing sets the BJT transistor into the **active state**, so that it can amplify the AC signal. Let us remember the states of the transistor:

- **Active:** Operating state of the amplifier: $I_C = \beta I_B$.
  - Base-Emitter ($BE$) junction: **forward-biased** (ON).
  - Base-Collector ($BC$) junction: **reverse-biased** (OFF).
- **Cut-Off:** The amplifier is basically off. There is **no current**, i.e., $I_C = I_B = I_E = 0\,\text{A}$.
  - Base-Emitter ($BE$) junction: **reverse-biased** (OFF).
  - Base-Collector ($BC$) junction: **reverse-biased** (OFF).
- **Saturation:** The amplifier is saturated. Voltages are fixed, e.g., $V_{CE} = V_{CE(sat)} \cong 0\,\text{V}$. **Output** is **distorted**, i.e., not the same shape as the input waveform.
  - Base-Emitter ($BE$) junction: **forward-biased** (ON).
  - Base-Collector ($BC$) junction: **forward-biased** (ON).

## 5.3 BJT DC Analysis

1. Draw the DC equivalent circuit (signal frequency is zero, i.e., $f = 0$)
   a) Capacitors are open circuit, i.e., $X_C \to \infty$.
   b) Kill the AC power sources (short-circuit AC voltage sources and open-circuit AC current sources).
   c) Inductors are short circuit or replaced by their DC resistance (winding resistance) if given, i.e., $X_L \to 0$.
2. Write KVL for the loop which contains $BE$ junction
   a) Take $V_{BE} = V_{BE(ON)}$ to ensure the transistor is ON (or not in the cut-off state). Note: For a *pnp* transistor, $V_{EB} = V_{BE(ON)}$.
   b) Determine the base current $I_{BQ}$ (or emitter current $I_{EQ}$).
3. Write KVL for the loop which contains $CE$ terminals
   a) Assume the transistor is in the active state and take $I_{CQ} = \beta I_{BQ}$ (or $I_{CQ} = \alpha I_{EQ}$).
   b) Calculate $V_{CEQ}$.
   c) If $V_{CEQ} \leq V_{CE(sat)}$ then the transistor is in the saturation (SAT) state (i.e., $I_{CQ} \neq \beta I_{BQ}$), so take $V_{CEQ} = V_{CE(sat)}$ and recalculate $I_{CQ}$.
   NOTE: Normally, a BJT should not be in the saturation state if it is used as an amplifier.

## 5.4 DC Biasing Circuits

Most common four common-emitter biasing circuits are given below

1. Fixed-Bias Circuit
2. Emitter-Stabilized Bias Circuit
3. Voltage Divider Bias Circuit
4. Collector Feedback Bias Circuit

### 5.4.1 Fixed-Bias Circuit

Fixed-bias circuit is given in Figure 5.2 below

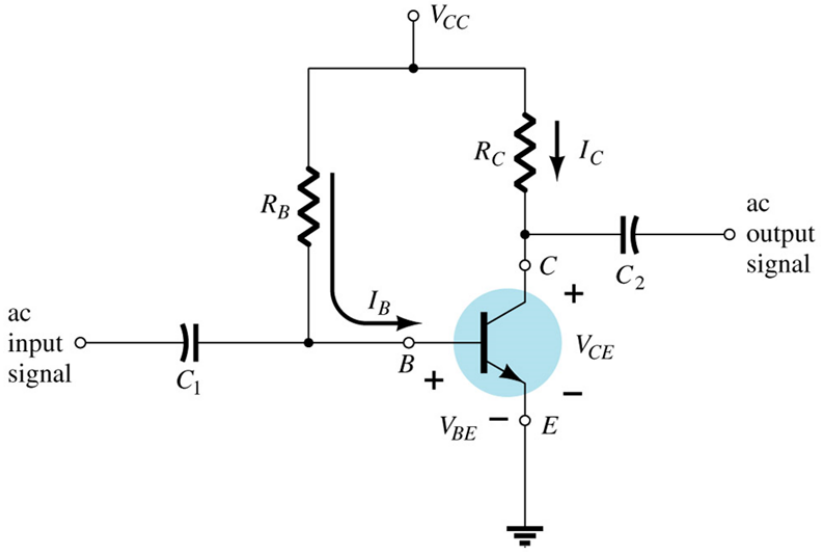



Figure 5.2: Fixed-bias BJT circuit.

Let us start DC analysis by drawing the DC equivalent circuit as shown in Figure 5.3 below

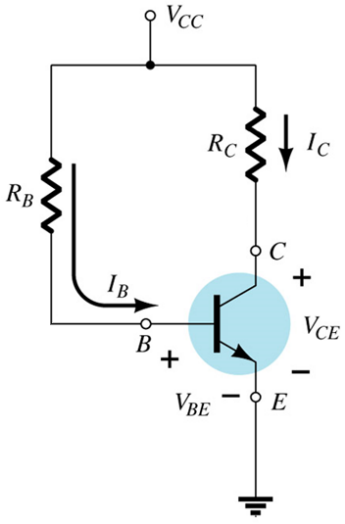



Figure 5.3: DC equivalent circuit of the fixed-bias circuit in Figure 5.2.

#### 5.4.1.1 Base-Emitter Loop

Let us continue with the $BE$ loop shown in Figure 5.4 below

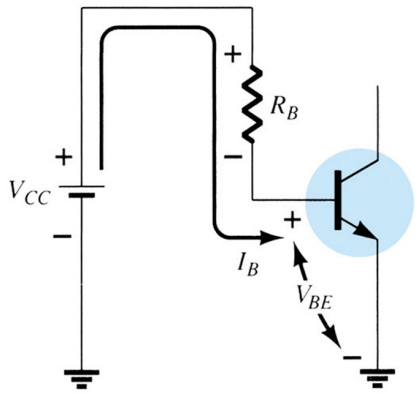



Figure 5.4: Base-emitter loop of the fixed-bias circuit in Figure 5.2.

Writing KVL on the $BE$ loop

$$V_{CC} - I_B R_B - V_{BE} = 0 \tag{5.4.1}$$

and given $V_{BE} = V_{BE(ON)}$, we obtain $I_{BQ}$ as

$$\boxed{I_{BQ} = \frac{V_{CC} - V_{BE(ON)}}{R_B}} \tag{5.4.2}$$

#### 5.4.1.2 Collector-Emitter Loop

Let us continue with the $CE$ loop shown in Figure 5.5 below

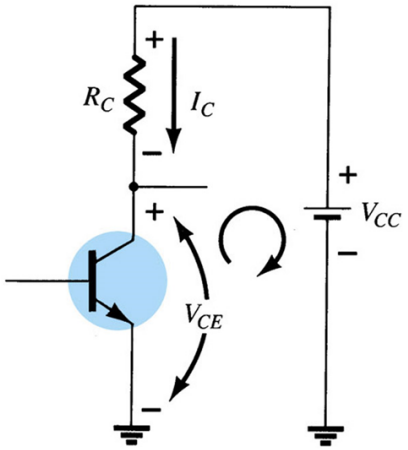



Figure 5.5: Collector-emitter loop of the fixed-bias circuit in Figure 5.2.

Writing KVL on the $CE$ loop (i.e., DC load-line equation)

$$V_{CC} - I_C R_C - V_{CE} = 0 \tag{5.4.3}$$

and given (assuming BJT is in active state)

$$\boxed{I_{CQ} = \beta I_{BQ}} \tag{5.4.4}$$

we obtain $V_{CEQ}$ as

$$\boxed{V_{CEQ} = V_{CC} - I_{CQ}R_C} \tag{5.4.5}$$

Thus, we obtained the $Q$-point $(I_{CQ}, V_{CEQ})$, i.e., the operating point.

#### 5.4.1.3 Saturation

The term **saturation** is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of water. For a transistor operating in the saturation region, the **current** is a **maximum** value for the particular design.

Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE(sat)}$. If we approximate the curves of Figure 5.6(a) by those appearing in Figure 5.6(b), then the saturation voltage $V_{CE(sat)}$ is assumed to be 0 V, i.e,

$$\boxed{V_{CE(sat)} \cong 0\,\text{V}} \tag{5.4.6}$$

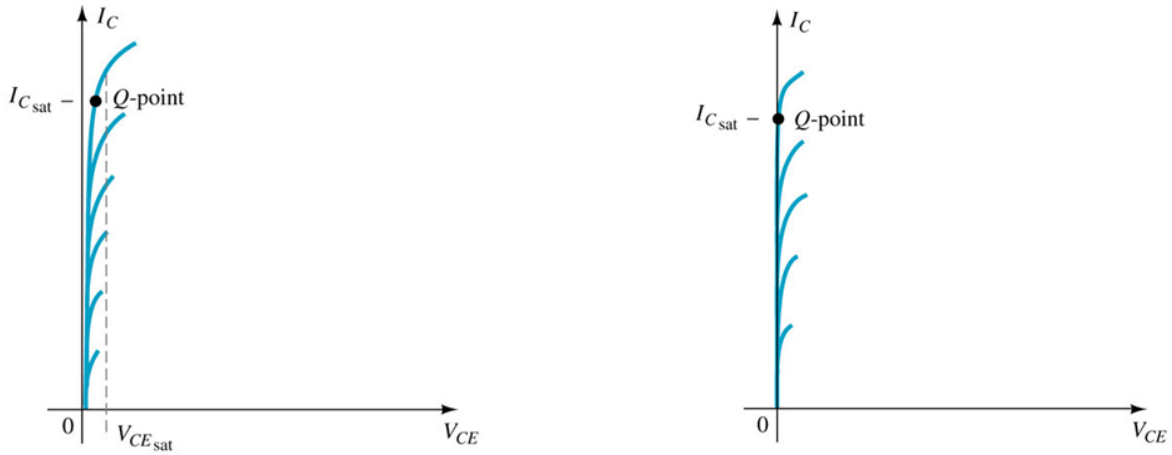



Figure 5.6: Saturation regions: (a) actual, (b) approximate.

For the fixed-bias configuration shown in Figure 5.7 below, the resulting saturation current (i.e., maximum current) $I_{C(sat)}$ is given by

$$I_{C(sat)} = I_{C(max)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \cong \frac{V_{CC}}{R_C} \tag{5.4.7}$$

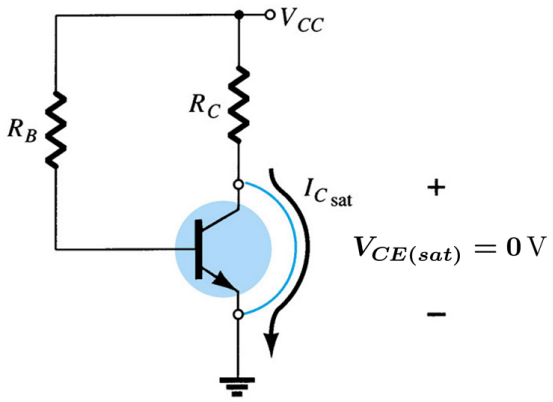



Figure 5.7: Determining $I_{C(sat)}$ for the fixed-bias configuration.Example 5.0.

**Example 5.1:** For the figure below, calculate all DC currents and voltages.

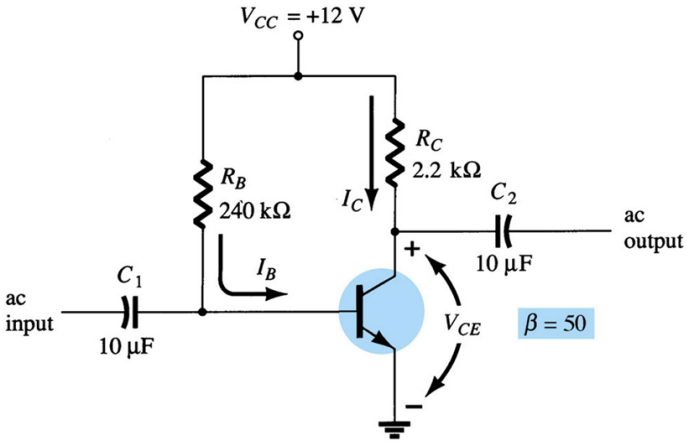



Figure 5.8: Fixed-bias circuit for Example 5.1.

**Solution:** Let us find $I_{BQ}$, $I_{CQ}$ and $V_{CEQ}$ as follows

$$I_{BQ} = \frac{V_{CC} - V_{BE(ON)}}{R_B} = \frac{12 - 0.7}{240k} = 47.08\,\mu\text{A},$$
$$I_{CQ} = \beta I_{BQ} = (50)(47.08\mu) = 2.35\,\text{mA},$$
$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 12 - (2.35m)(2.2k) = 6.83\,\text{V}.$$

As $V_{CEQ} > V_{CE(sat)} = 0\,\text{V}$, transistor is in the active state. Let us also prove it by showing $V_{BCQ} < V_{BC(ON)} = 0.7\,\text{V}$ as follows

$$V_{BCQ} = V_{BQ} - V_{CQ} = V_{BEQ} - V_{CEQ} = 0.7 - 6.83 = -6.13\,\text{V} < 0.7\,\text{V}.$$

#### 5.4.1.4 DC Load Line

DC load line equation comes from KVL equation in the $CE$ loop (i.e., output loop). For the fixed-bias circuit of Figure 5.2 DC load line equation is given by

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \tag{5.4.8}$$

Let us draw the load line over output characteristics curve as shown in Figure 5.9 below. The **intersection** of the load-line with the output characteristics curve (determined by the base current $I_{BQ}$) is the **operating point**, i.e., $Q$-point.

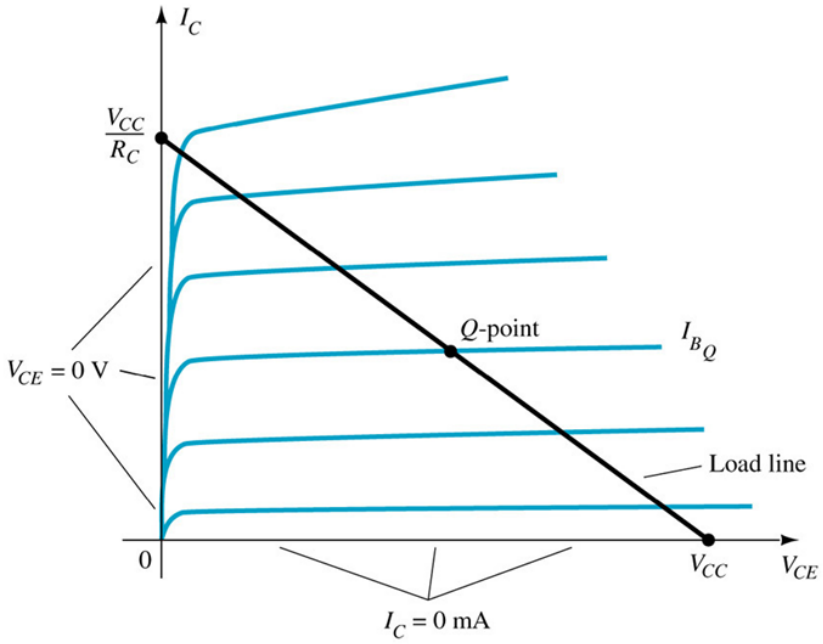



Figure 5.9: Load line of the fixed-bias circuit in Figure 5.2.

- The $Q$-point is the operating point where the value of $R_B$ sets the value of $I_{BQ}$ that controls the values of $V_{CEQ}$ and $I_{CQ}$.

  Fixed-bias load line equation: $V_{CE} = V_{CC} - I_C R_C$

  The load line end points are the SATURATION and CUTOFF points, i.e.,

- $I_{C(sat)}$ end point (on the current axis):

$$I_C = V_{CC}/R_C$$
$$V_{CE} = 0\,\text{V}$$

- $V_{CE(cutoff)}$ end point (on the voltage axis):

$$V_{CE} = V_{CC}$$
$$I_C = 0\,\text{mA}$$

### The Effect of $I_B$ on the $Q$-Point

Movement of the $Q$-point with increasing level of $I_B$ (or decreasing level of $R_B$) is shown in Figure 5.10 below.

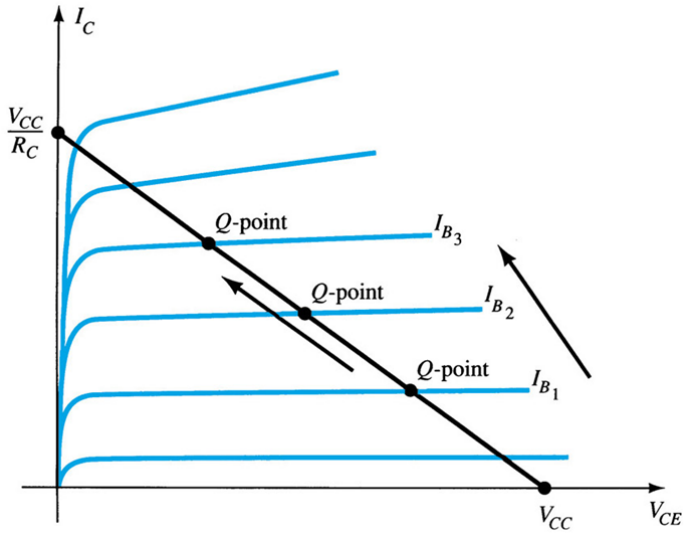



Figure 5.10: Movement of the $Q$-point with increasing level of $I_B$.

### The Effect of $R_C$ on the $Q$-Point

Effect of an increasing level of $R_C$ on the load line (slope decreases with increasing $R_C$) and the $Q$-point is shown in Figure 5.11 below.

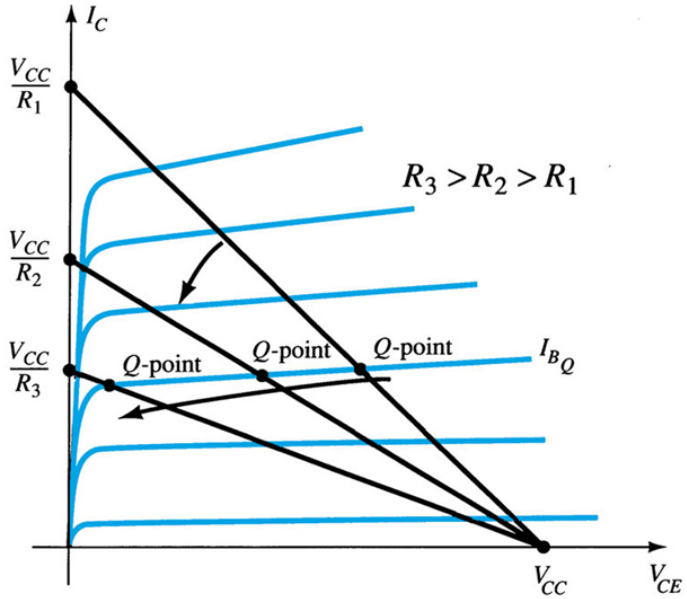



Figure 5.11: Effect of an increasing level of $R_C$ on the load line and the $Q$-point.

### The Effect of $V_{CC}$ on the $Q$-Point

Effect of an decreasing level of $V_{CC}$ on the load line (end points gets smaller with decreasing $V_{CC}$) and the $Q$-point is shown in Figure 5.12 below.

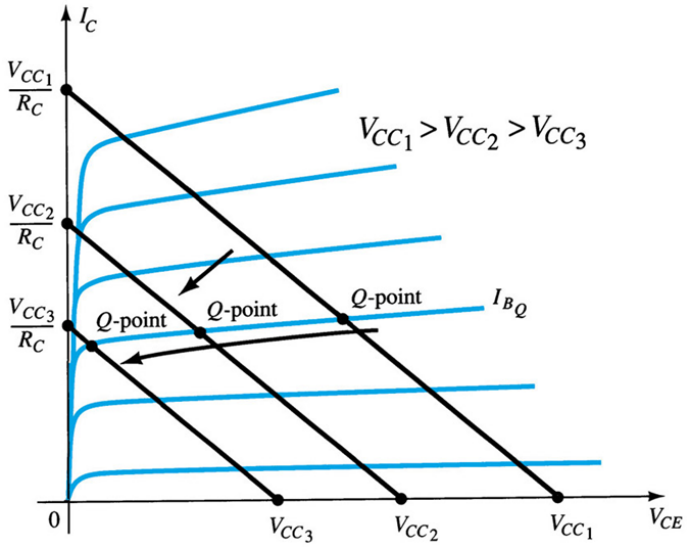



Figure 5.12: Effect of lower values of $V_{CC}$ on the load line and the $Q$-point.

**Example 5.2:** For the fixed-bias load line below, calculate $V_{CC}$, $R_C$ and $R_B$.

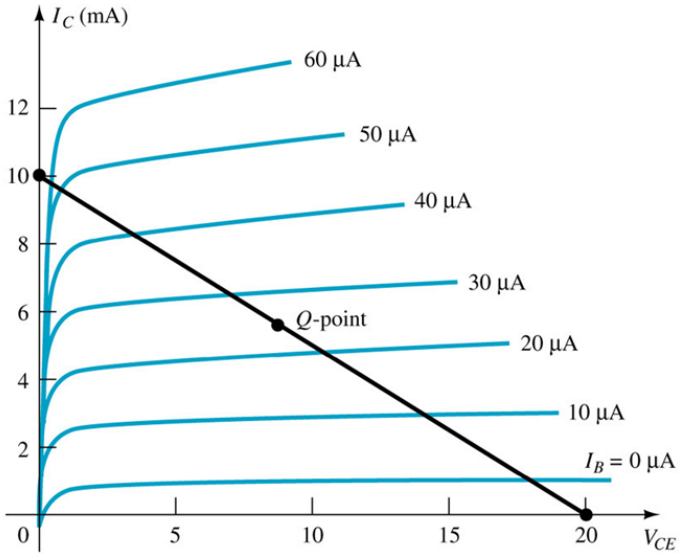



Figure 5.13: Fixed-bias load line for Example 5.2.

**Solution:** From the figure, $I_{BQ} = 25\,\mu$A. So, let us find $V_{CC}$, $R_C$ and $R_B$ as follows

$$V_{CC} = V_{CE(cutoff)} = 20\,\text{V},$$
$$R_C = \frac{V_{CC}}{I_{C(sat)}} = \frac{20}{10m} = 2\,\text{k}\Omega,$$
$$R_B = \frac{V_{CC} - V_{BE(ON)}}{I_{BQ}} = \frac{20 - 0.7}{25\mu} = 772\,\text{k}\Omega.$$

### 5.4.2 Emitter-Stabilized Bias Circuit

Adding a resistor to the emitter circuit stabilizes the bias circuit, as shown in Figure 5.14 below.

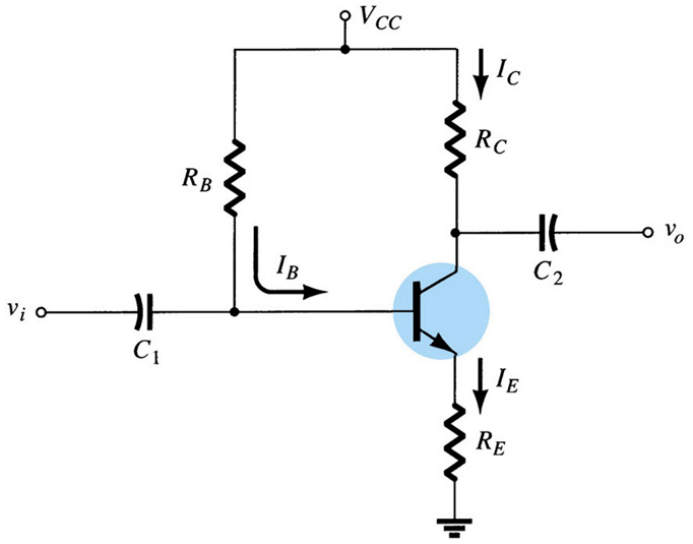



Figure 5.14: Emitter-stabilized bias circuit.

Let us start DC analysis by drawing the DC equivalent circuit as shown in Figure 5.15 below

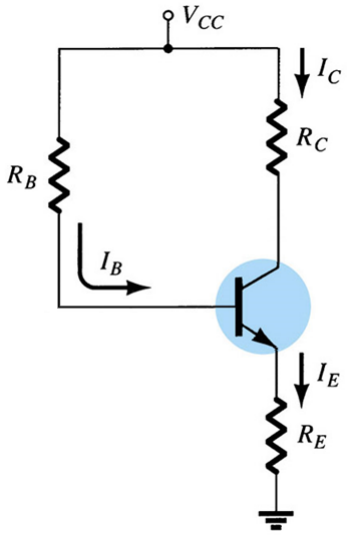
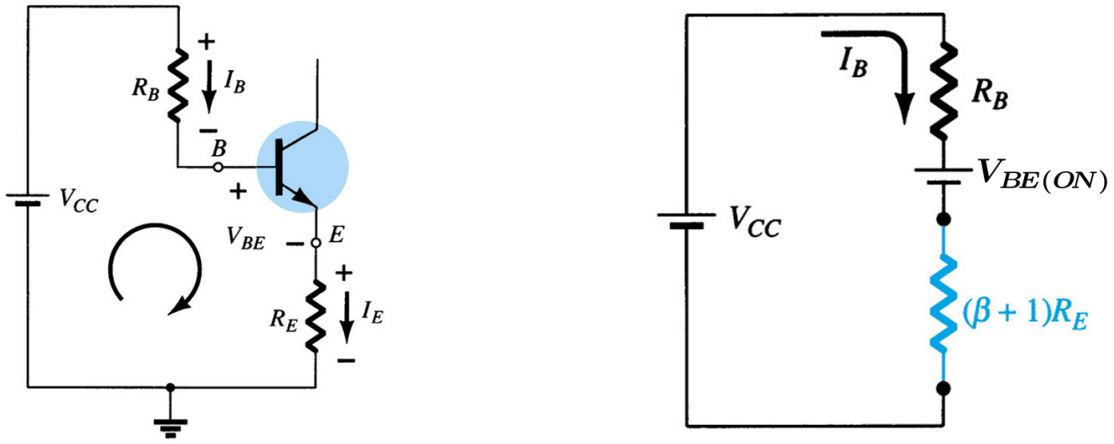



Figure 5.15: DC equivalent circuit of the emitter-stabilized bias circuit in Figure 5.14.

#### 5.4.2.1 Base-Emitter Loop

Let us continue with the $BE$ loop shown in Figure 5.16 below




(a) (b)

Figure 5.16: Base-emitter loop of the emitter-stabilized bias circuit in Figure 5.14: (a) normal circuit, (b) equivalent circuit for common base current.

Writing KVL on the $BE$ loop

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \tag{5.4.9}$$

$$V_{CC} - I_B R_B - V_{BE(ON)} - (\beta + 1) I_B R_E = 0, \quad \ldots \text{as } V_{BE} = V_{BE(ON)} \text{ and } I_E = (\beta + 1) I_B \text{ in active mode} \tag{5.4.10}$$

we obtain $I_{BQ}$ as

$$\boxed{I_{BQ} = \frac{V_{CC} - V_{BE(ON)}}{R_B + (\beta + 1) R_E}} \tag{5.4.11}$$

Similarly, we can obtain $I_{EQ}$ directly from Figure 5.17, or dividing the denominator of the $I_{BQ}$ in (5.4.12) by $(\beta + 1)$

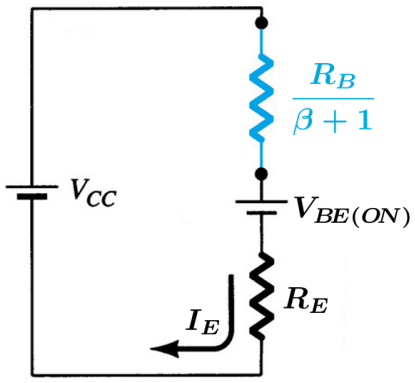



Figure 5.17: Equivalent circuit for common emitter current for the base-emitter loop of the emitter-stabilized bias circuit in Figure 5.14.

as follows

$$\boxed{I_{EQ} = \frac{V_{CC} - V_{BE(ON)}}{\frac{R_B}{\beta + 1} + R_E}} \tag{5.4.12}$$

- It is generally better to calculate $I_{EQ}$ directly to reduce the number of calculations, especially when there is an emitter resistor $R_E$ is connected.

#### 5.4.2.2 Collector-Emitter Loop

Let us continue with the $CE$ loop shown in Figure 5.18 below

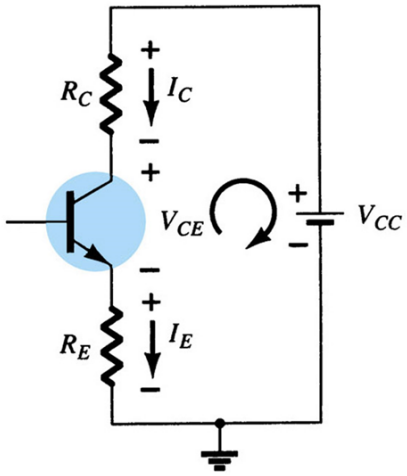



Figure 5.18: Collector-emitter loop of the emitter-stabilized bias circuit in Figure 5.14.

Let us write down the KVL equation on the $CE$ loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0 \tag{5.4.13}$$

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0 \qquad \ldots \text{as } I_C = \alpha I_E \cong I_E \text{ in active mode} \tag{5.4.14}$$

$$V_{CC} - I_C(R_C + R_E) - V_{CE} = 0 \qquad \ldots \text{DC load line equation} \tag{5.4.15}$$

As $I_{CQ} = \beta I_{BQ} \cong I_{EQ}$ in active mode, we obtain $V_{CEQ}$ as

$$\boxed{V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)} \tag{5.4.16}$$

Thus, we obtained the $Q$-point $(I_{CQ}, V_{CEQ})$, i.e., the operating point.

#### 5.4.2.3 DC Load Line

DC load line equation comes from KVL equation in the $CE$ loop (i.e., output loop). For the emitter-stabilized bias circuit of Figure 5.14 DC load line equation is given by

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \tag{5.4.17}$$

Let us draw the load line over output characteristics curve as shown in Figure 5.19 below.

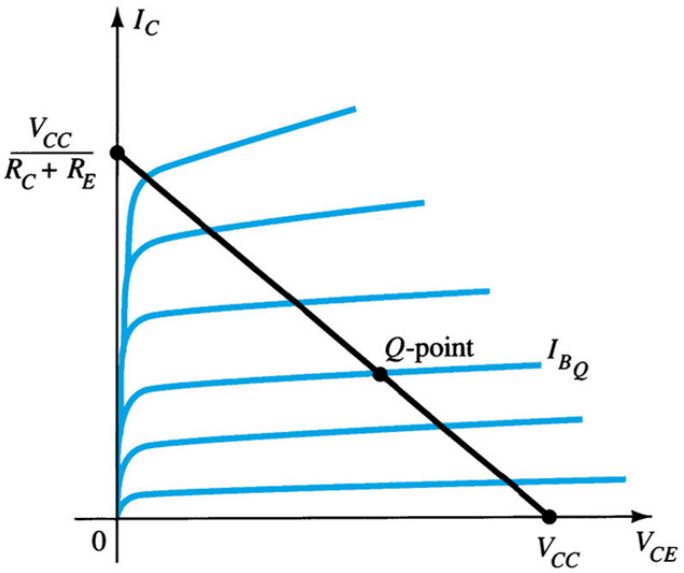



Figure 5.19: Load line of the emitter-stabilized bias circuit in Figure 5.14.

Here, $V_{CE(cutoff)} = V_{CC}$ and $I_{C(sat)}$ is given by

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} \tag{5.4.18}$$

- The $Q$-point is the operating point where the value of $R_B$ and $R_E$ sets the value of $I_{BQ}$ that controls the values of $V_{CEQ}$ and $I_{CQ}$.

#### 5.4.2.4 Improved Biased Stability

**Stability** refers to a condition in which the currents and voltages remain fairly constant over a wide range of temperatures and transistor beta ($\beta$) values.

- Adding $R_E$ resistor to the emitter improves the stability of a transistor.

**Example 5.3:** For the figure below, calculate all DC currents and voltages.

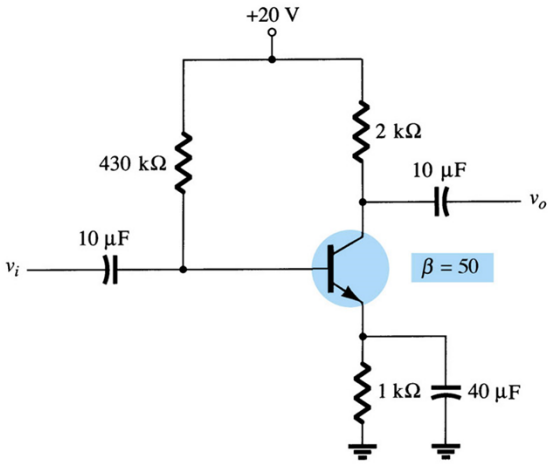



Figure 5.20: Emitter-stabilized bias circuit for Example 5.3.

**Solution:** Let us find $I_{BQ}$, $I_{CQ}$ and $V_{CEQ}$ as follows

$$\begin{aligned} I_{BQ} &= \frac{V_{CC} - V_{BE(ON)}}{R_B + (\beta+1)R_E} = \frac{20 - 0.7}{430k + (50+1)(1k)} = 40.13\,\mu\text{A}, \\ I_{CQ} &= \beta I_{BQ} = (50)(40.13\mu) = 2.01\,\text{mA}, \\ V_{CEQ} &\cong V_{CC} - I_{CQ}(R_C + R_E) = 20 - (2.01m)(2k + 1k) = 13.97\,\text{V}. \end{aligned}$$

As $V_{CEQ} > 0\,\text{V}$ ($V_{CE(sat)}$), transistor is in the active state. Let us also prove it by showing $V_{BCQ} < V_{BC(ON)} = 0.7\,\text{V}$ as follows

$$V_{BCQ} = V_{BQ} - V_{CQ} = V_{BEQ} - V_{CEQ} = 0.7 - 13.97 = -13.27\,\text{V} < 0.7\,\text{V}.$$

### 5.4.3 Voltage Divider Bias Circuit

Voltage divider bias circuit is given in Figure 5.21 below

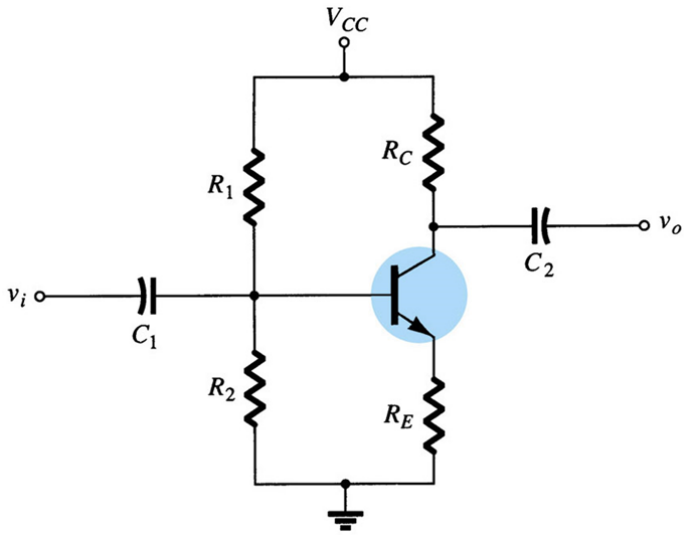



Figure 5.21: Voltage divider bias BJT circuit.

Let us start DC analysis by drawing the DC equivalent circuit as shown in Figure 5.22 below

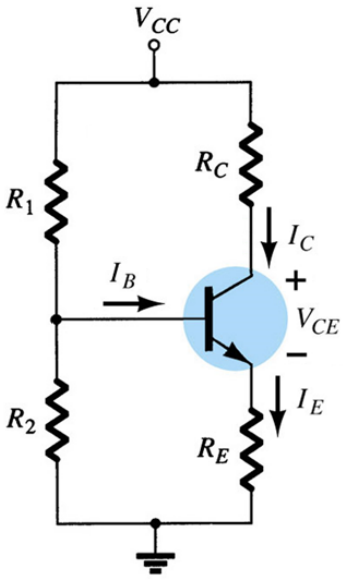



Figure 5.22: DC equivalent circuit of the voltage divider bias circuit in Figure 5.21.

#### 5.4.3.1 Base-Emitter Loop (Exact Analysis)

Let us transform the $BE$ loop circuit shown in Figure 5.23(a) below to the Thévenin simplified circuit in Figure 5.23(b) below

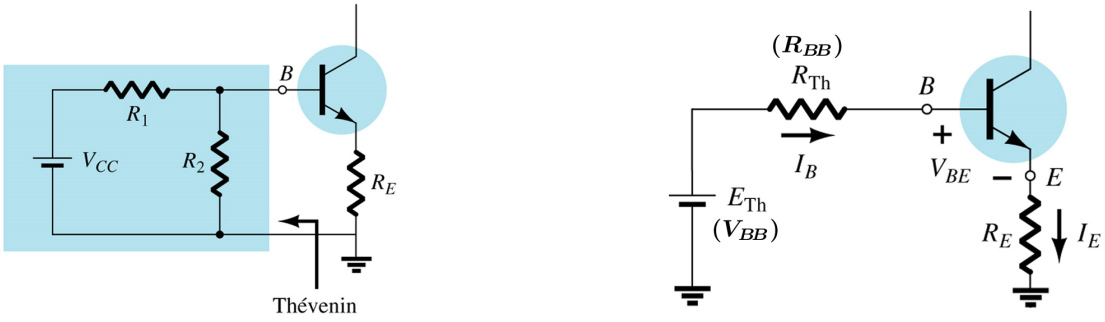



Figure 5.23: Base-emitter loop of the voltage divider bias circuit in Figure 5.21: (a) normal circuit, (b) Thévenin equivalent circuit.

where the Thévenin voltage $V_{BB}$ and Thévenin resistance $R_{BB}$ are calculated as follows

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \quad \text{... from Figure 5.24(a) below} \quad (5.4.19)$$

$$R_{BB} = R_1 || R_2 \quad \text{... from Figure 5.24(b) below} \quad (5.4.20)$$

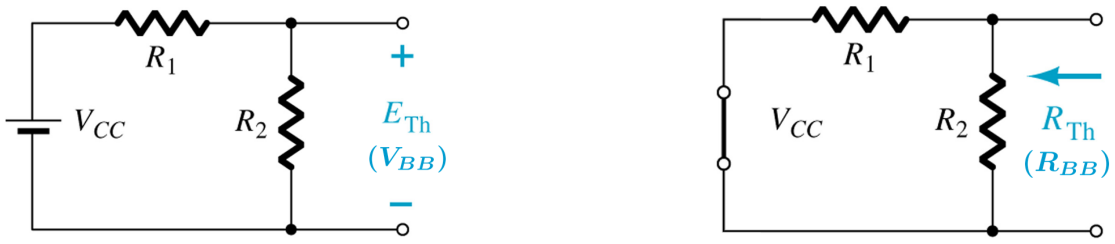



Figure 5.24: Thévenin analysis circuits for the circuit in Figure 5.23(a): (a) Open-circuit voltage calculation, (b) Test-voltage method for Thévenin resistance calculation.

Writing KVL on the Thévenin equivalent $BE$ loop shown in Figure 5.23(b)

$$V_{BB} - I_B R_{BB} - V_{BE} - I_E R_E = 0 \tag{5.4.21}$$

$$V_{BB} - I_B R_{BB} - V_{BE(ON)} - (\beta+1) I_B R_E = 0, \quad \ldots \text{as } V_{BE} = V_{BE(ON)} \text{ and } I_E = (\beta+1) I_B \text{ in active mode} \tag{5.4.22}$$

we obtain $I_{BQ}$ as

$$\boxed{I_{BQ} = \frac{V_{BB} - V_{BE(ON)}}{R_{BB} + (\beta+1) R_E}} \tag{5.4.23}$$

Similarly, we obtain $I_{EQ}$ as

$$\boxed{I_{EQ} = \frac{V_{BB} - V_{BE(ON)}}{\frac{R_{BB}}{\beta+1} + R_E}} \tag{5.4.24}$$

#### 5.4.3.2 Base-Emitter Loop (Approximate Analysis)

If we look at the $I_{EQ}$ equation in (5.4.24), we see that if $R_E \gg \frac{R_{BB}}{\beta+1}$, equation simplifies to

$$\boxed{I_{EQ} = \frac{V_{BB} - V_{BE(ON)}}{R_E}} \tag{5.4.25}$$

where $V_{BB} = \frac{R_2}{R_1+R_2} V_{CC}$.

- Approximate approach can be used when $(\beta+1)R_E \gg R_{BB}$. Approximate analysis condition can be rewritten as

$$\boxed{(\beta+1)R_E \geq 10(R_1 || R_2).} \tag{5.4.26}$$

Assuming $R_1 > R_2$, we know that $(R_1||R_2) \leq R_2$. So, the condition above can be further simplified to

$$\boxed{\beta R_E \geq 10 R_2.} \tag{5.4.27}$$

- Satisfying this condition means that we can safely ignore the base current $I_B$ in the DC equivalent circuit shown in Figure 5.22 and apply the voltage divider rule between $R_2$ and $R_1$.
- Finally, if $\beta$ times the value of $R_E$ is at least 10 times the value of $R_2$, the approximate approach can be applied with a high degree of accuracy.

#### 5.4.3.3 Collector-Emitter Loop and DC Load line

- Analysis on the $CE$ loop (i.e., output loop), is the same as the $CE$ loop analysis of the emitter-stabilized circuit given in Section 5.4.2.2. So, $V_{CEQ}$ is given by

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$$

where $I_{CQ} \cong I_{EQ}$.

- Similarly, DC load line analysis is also the same as the DC load line of the emitter-stabilized circuit given in Section 5.4.2.3. So, DC load line equation is given by

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

**Example 5.4:** For the figure below, calculate all DC currents and voltages using both exact and approximate analysis.

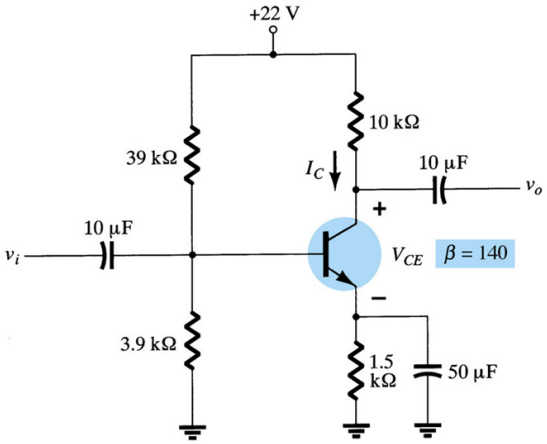



Figure 5.25: Voltage-divider bias circuit for Example 5.4.

**Solution:** Let us first find the Thévenin voltage $V_{BB}$ and resistance $R_{BB}$ as follows

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{3.9k}{39k + 3.9k} 22 = 2\,\text{V},$$
$$R_{BB} = R_1 || R_2 = 3.9k || 39k = 3.55\,\text{k}\Omega.$$

Now, let us calculate $I_{BQ}$, $I_{CQ}$ and $V_{CEQ}$ as follows

$$I_{EQ} = \frac{V_{BB} - V_{BE(ON)}}{R_{BB}/(\beta + 1) + R_E} = \frac{2 - 0.7}{3.55k/(140 + 1) + 1.5k} = 0.85\,\text{mA},$$
$$I_{CQ} \cong I_{EQ} = 0.85\,\text{mA},$$
$$V_{CEQ} \cong V_{CC} - I_{CQ}(R_C + R_E) = 22 - (0.85m)(10k + 1.5k) = 12.23\,\text{V}.$$

As $\beta R_E \geq 10R_2$ (i.e., $210\,\text{k}\Omega \geq 39\,\text{k}\Omega$), we can use the approximate analysis and ignore $R_{BB}$ and voltage drop across $R_{BB}$ as follows

$$I_{EQ} = \frac{V_{BB} - V_{BE(ON)}}{R_E} = \frac{2 - 0.7}{1.5k} = 0.87\,\text{mA},$$
$$I_{CQ} \cong I_{EQ} = 0.87\,\text{mA},$$
$$V_{CEQ} \cong V_{CC} - I_{CQ}(R_C + R_E) = 22 - (0.87m)(10k + 1.5k) = 12\,\text{V}.$$

We see that approximate analysis provides close values to the exact analysis. The differences in $I_{CQ}$ and $V_{CEQ}$ are only 0.02 mA and 0.23 V, respectively.

### 5.4.4 Collector Feedback Bias Circuit

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base as shown in Figure 5.26 below

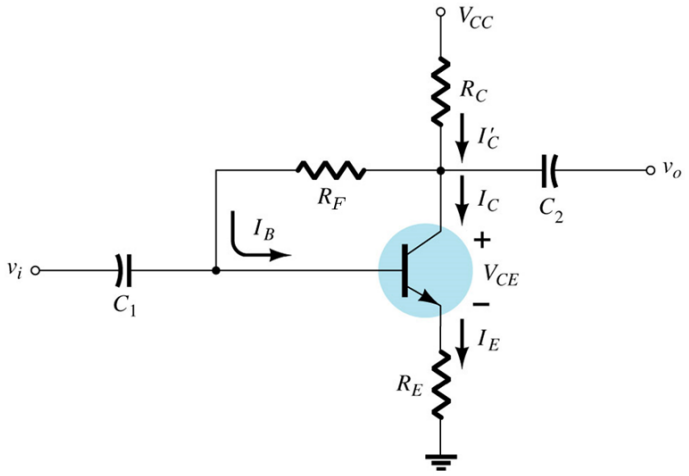



Figure 5.26: Collector feedback bias circuit.

Let us start DC analysis by drawing the DC equivalent circuit as shown in Figure 5.27 below

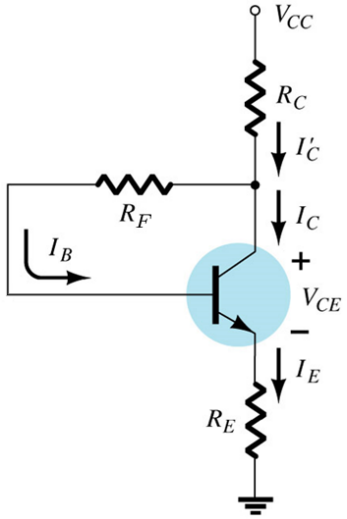



Figure 5.27: DC equivalent circuit of the collector feedback circuit in Figure 5.26.

#### 5.4.4.1 Base-Emitter Loop

Let us continue with the $BE$ loop shown in Figure 5.28 below

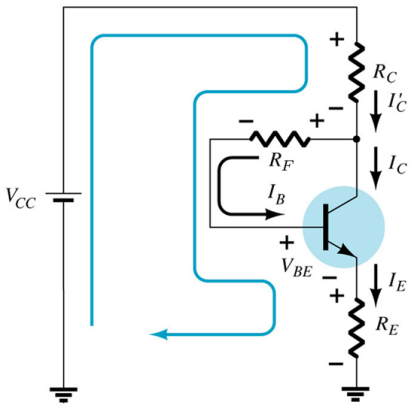



Figure 5.28: Base-emitter loop of the collector feedback circuit in Figure 5.26.

We can write KVL equation on the $BE$ loop noting that $I'_C = I_C + I_B = I_E$

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0 \tag{5.4.28}$$

$$V_{CC} - I_E R_C - \frac{I_E}{\beta + 1} R_F - V_{BE(ON)} - I_E R_E = 0, \quad \ldots \text{as } V_{BE} = V_{BE(ON)} \text{ and}$$

$$I_B = \frac{I_E}{\beta + 1} \text{ in active mode} \tag{5.4.29}$$

and we obtain $I_{EQ}$ as

$$\boxed{I_{EQ} = \frac{V_{CC} - V_{BE(ON)}}{\frac{R_F}{\beta + 1} + (R_C + R_E)}} \tag{5.4.30}$$

#### 5.4.4.2 Collector-Emitter Loop

Let us continue with the $CE$ loop shown in Figure 5.29 below

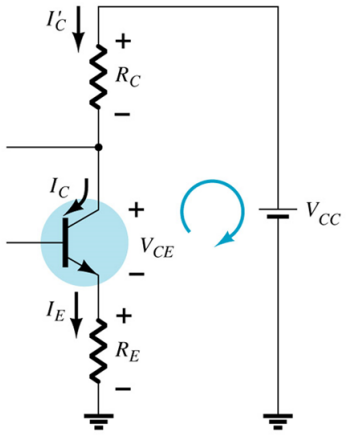



Figure 5.29: Collector-emitter loop of the collector feedback circuit in Figure 5.26.

Let us write down the KVL equation on the $CE$ loop noting that $I'_C = I_C + I_B$

$$V_{CC} - I'_C R_C - V_{CE} - I_E R_E = 0 \tag{5.4.31}$$
$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0 \qquad \ldots \text{as } I_C \cong I_E \text{ and } I_C \cong I'_C \text{in active mode} \tag{5.4.32}$$
$$V_{CC} - I_C(R_C + R_E) - V_{CE} = 0 \qquad \ldots \text{DC load line equation} \tag{5.4.33}$$

As $I_{CQ} \cong I_{EQ}$ in active mode, we obtain $V_{CEQ}$ as

$$\boxed{V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)} \tag{5.4.34}$$

Thus, we obtained the $Q$-point $(I_{CQ}, V_{CEQ})$, i.e., the operating point.

#### 5.4.4.3 DC Load line

- Note that $I'_C = I_E$, and
$$I_C \cong I_E$$
in active mode (and $\beta$ is high).
- So, DC load line analysis is the same as the DC load line of the emitter-stabilized circuit given in Section 5.4.2.3. So, DC load line equation is given by
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

### 5.4.5 Various Different Bias Circuits

**Example 5.5:** For the figure below, calculate all DC currents and voltages.

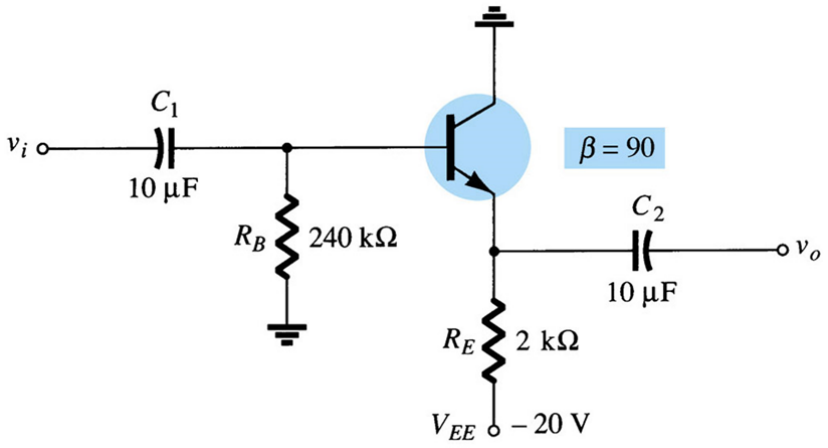



Figure 5.30: Common-collector bias circuit for Example 5.5.

**Solution:** Let us find $I_{EQ}$, $I_{CQ}$ and $V_{CEQ}$ as follows

$$I_{EQ} = \frac{0 - V_{BE(ON)} - V_{EE}}{R_B/(\beta+1) + R_E} = \frac{20 - 0.7}{240k/(90+1) + 2k} = 4.16\,\text{mA},$$
$$I_{CQ} \cong I_{EQ} = 4.16\,\text{mA},$$
$$V_{CEQ} = 0 - I_{EQ}R_E - V_{EE} = 20 - (4.16m)(2k) = 11.68\,\text{V}.$$

As $V_{CEQ} > V_{CE(sat)} = 0\,\text{V}$, transistor is in the active state.

### 5.4.6 *pnp* Transistors

The analysis for *pnp* bias transistor circuits is the same as that for *npn* transistor circuits.

The only differences are that

1. Currents are flowing in the opposite direction.
2. Voltages have opposite polarity, e.g., $V_{EB} = V_{BE(ON)} = 0.7\,\text{V}$ in the active mode.

**Example 5.6:** For the figure below, calculate all DC currents and voltages.

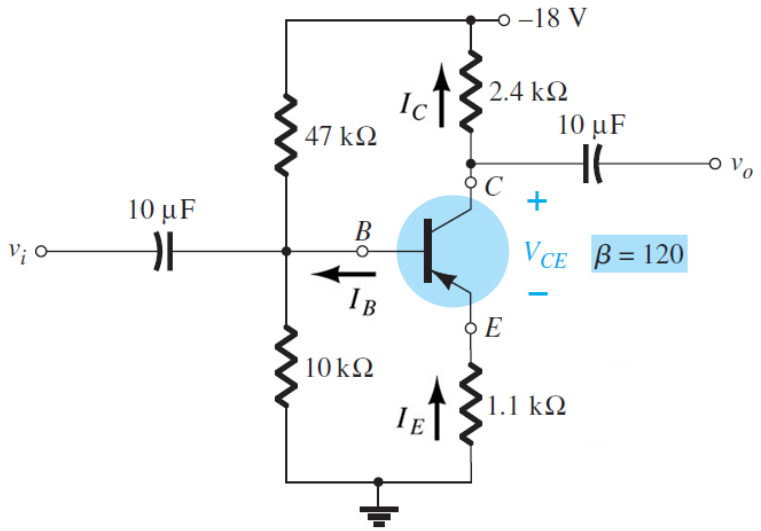



Figure 5.31: *pnp* transistor in a voltage-divider bias configuration Example 5.6.

**Solution:** As $\beta R_E \geq 10R_2$, i.e., $132\,\text{k}\Omega \geq 100\,\text{k}\Omega$, we can ignore $R_{BB}$ and use the approximate approach. Thus, we can find $V_{BB}$, $I_{EQ}$, $I_{CQ}$ and $V_{ECQ}$ as follows

$$
\begin{aligned}
V_B &\cong \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10k}{47k + 10k}(-18) = -3.16\,\text{V} \\
I_{EQ} &\cong \frac{0 - V_{EB} - V_B}{R_E} = \frac{0 - 0.7 - (-3.16)}{1.1k} = \frac{2.46}{1.1k} = 2.24\,\text{mA}, \\
I_{CQ} &\cong I_{EQ} = 2.24\,\text{mA}, \\
V_{ECQ} &= 0 - I_{CQ}(R_C + R_E) - V_{CC} = -(2.24m)(2.4k + 1.1k) - (-18) = 10.16\,\text{V}.
\end{aligned}
$$

As $V_{ECQ} > V_{CE(sat)} = 0\,\text{V}$, transistor is in the active state.

## 5.5 Bias Stabilization

Variation of three BJT (Si) parameters ($I_{CO}$, $\beta$ and $V_{BE(ON)}$) with temperature are summarized below

$$
\boxed{T \uparrow \qquad I_{CO} \uparrow \qquad \beta \uparrow \qquad V_{BE(ON)} \downarrow} \tag{5.5.35}
$$

- $I_{CO}$ (reverse saturation current)

- doubles in value for every 10 °C
- $\beta$ (transistor current gain)
  - increases with increasing temperature
- $V_{BE(ON)}$ (forward bias potential of the base-emitter junction)
  - decreases about 2.5 mV per 1 °C increase in temperature

Variation of the transistor parameters with temperature causes a shift in the operating point (i.e., $Q$-point).

Figures below (at 25 °C on the left and at 100 °C on the right) show the shift of the $Q$-point (or DC bias point) due to temperature change for a fixed-bias circuit.

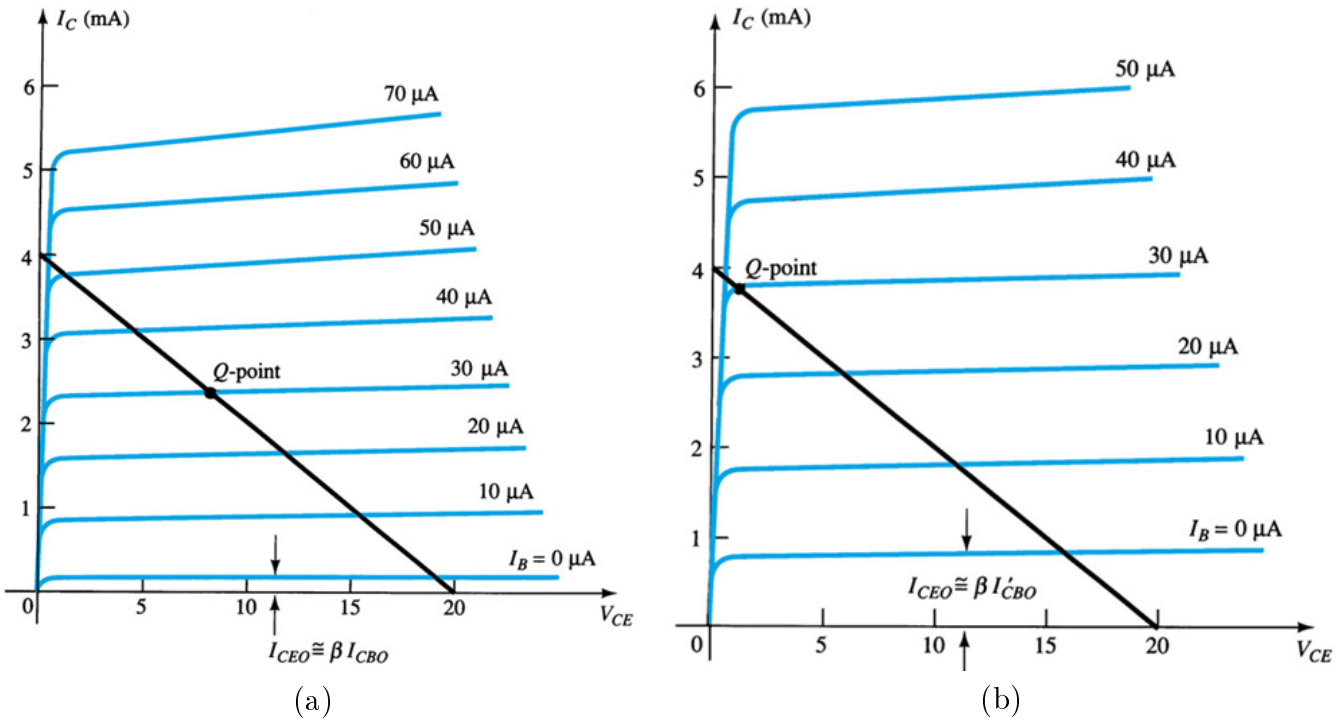



Figure 5.32: Shift in operating point ($Q$-point) due to change in temperature: (a) 25 °C, (b) 100 °C.

### 5.5.1 Stability Factors

Stability of the collector current $I_C$ depends on the stability of several parameters like $I_{CO}$, $\beta$, $V_{BE(ON)}$, $V_{CC}$, $R_B$, $R_C$, etc.

A stability factor $S$ is defined for **each** of the parameters affecting bias stability as follows:

$$S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}} = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{\beta, V_{BE(ON)}, \ldots \text{ constant}} \tag{5.5.36}$$

$$S_{\beta} = \frac{\partial I_C}{\partial \beta} = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO}, V_{BE(ON)}, \ldots \text{ constant}} \tag{5.5.37}$$

$$S_{V_{BE(ON)}} = \frac{\partial I_C}{\partial V_{BE(ON)}} = \left.\frac{\Delta I_C}{\Delta V_{BE(ON)}}\right|_{I_{CO}, \beta, \ldots \text{ constant}} \tag{5.5.38}$$

We know that differential $dI_C$ is given by the linear map of parameter differentials as follows

$$dI_C = \frac{\partial I_C}{\partial I_{CO}} dI_{CO} + \frac{\partial I_C}{\partial \beta} d\beta + \frac{\partial I_C}{\partial V_{BE(ON)}} dV_{BE(ON)} + \cdots \tag{5.5.39}$$

- Thus, we obtain the collector-current change $\Delta I_C$ using the stability factors as follows

$$\boxed{\Delta I_C \cong S_{I_{CO}} \Delta I_{CO} + S_\beta \Delta\beta + S_{V_{BE(ON)}} \Delta V_{BE(ON)}} \tag{5.5.40}$$

#### 5.5.1.1 Derivation of Stability Factors (Voltage-Divider Bias Circuit)

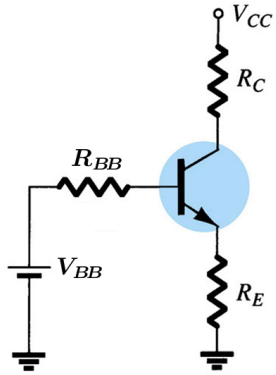



Figure 5.33: Equivalent circuit for the voltage-divider configuration.

Let us write down the active mode collector current and $BE$-loop KVL equations for the circuit shown in Figure 5.33 above,

$$I_C = \beta I_B + (\beta + 1)\, I_{CO} \tag{5.5.41}$$

$$V_{BB} = I_B R_{BB} + V_{BE(ON)} + (I_B + I_C) R_E \tag{5.5.42}$$

Combining the two equations (5.5.41) and (5.5.42) above, we obtain the expression for $I_C$ as

$$\boxed{I_C = \frac{\beta}{R_{BB} + (\beta + 1)\, R_E} \left(V_{BB} - V_{BE(ON)}\right) + \frac{(\beta + 1)\,(R_{BB} + R_E)}{R_{BB} + (\beta + 1)\, R_E} I_{CO}} \tag{5.5.43}$$

1. From equation (5.5.43), let us derive $S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}}$ as

$$\boxed{S_{I_{CO}} = (\beta + 1)\, \frac{R_{BB} + R_E}{R_{BB} + (\beta + 1)\, R_E}} \tag{5.5.44}$$

2. From equation (5.5.43), let us derive $S_{V_{BE(ON)}} = \frac{\partial I_C}{\partial V_{BE(ON)}}$ as

$$\boxed{S_{V_{BE(ON)}} = \frac{-\beta}{R_{BB} + (\beta + 1)\, R_E}} \tag{5.5.45}$$

3. In order to derive $S_\beta = \frac{\partial I_C}{\partial \beta}$, let us first simplify (5.5.43) by letting $I_{CO} \cong 0$

$$I_C \cong \frac{\beta}{R_{BB} + (\beta + 1) R_E} \left(V_{BB} - V_{BE(ON)}\right) \tag{5.5.46}$$

Using the simplified $I_C$ equation (5.5.46) we can express $I_{C_1}$ and $I_{C_2}$ as follows

$$I_{C_1} \cong \frac{\beta_1}{R_{BB} + (\beta_1 + 1) R_E} \left(V_{BB} - V_{BE(ON)}\right) \tag{5.5.47}$$

$$I_{C_2} \cong \frac{\beta_2}{R_{BB} + (\beta_2 + 1) R_E} \left(V_{BB} - V_{BE(ON)}\right) \tag{5.5.48}$$

Thus, using (5.5.47) and (5.5.48), let us obrain the ratio $\frac{I_{C_2} - I_{C_1}}{I_{C_1}}$ as

$$\frac{I_{C_2} - I_{C_1}}{I_{C_1}} = \frac{\beta_2 - \beta_1}{\beta_1} \frac{R_{BB} + R_E}{R_{BB} + (\beta_2 + 1) R_E} \tag{5.5.49}$$

From equation (5.5.50), we can obtain the ratio $\frac{\Delta I_C}{\Delta \beta}$ by using $\Delta I_C = I_{C_2} - I_{C_1}$ and $\Delta \beta = \beta_2 - \beta_1$ as

$$\frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}}{\beta_1} \frac{R_{BB} + R_E}{R_{BB} + (\beta_2 + 1) R_E} \tag{5.5.50}$$

Thus, as $S_\beta = \frac{\partial I_C}{\partial \beta} \cong \frac{\Delta I_C}{\Delta \beta}$

$$\boxed{S_\beta = \frac{I_{C_1}}{\beta_1} \frac{R_{BB} + R_E}{R_{BB} + (\beta_2 + 1) R_E}} \tag{5.5.51}$$

#### 5.5.1.2 Stability Factors for Other Bias Circuits

A. For the **fixed-bias** circuit, i.e., by substituting $R_E = 0$ and $R_{BB} = R_B$ into (5.5.44), (5.5.45) and (5.5.51), the stability factors are given by

$$S_{I_{CO}} = \beta + 1 \tag{5.5.52}$$

$$S_{V_{BE(ON)}} = \frac{-\beta}{R_B} \tag{5.5.53}$$

$$S_\beta = \frac{I_{C_1}}{\beta_1} \tag{5.5.54}$$

B. For the **emitter-stabilized bias** circuit, i.e., $R_{BB} = R_B$ and $R_B \gg R_E$, the stability factors are given by

$$S_{I_{CO}} = (\beta + 1) \frac{R_B + R_E}{R_B + (\beta + 1) R_E} \cong \frac{\beta + 1}{1 + \frac{(\beta + 1) R_E}{R_B}} \tag{5.5.55}$$

$$S_{V_{BE(ON)}} = \frac{-\beta}{R_B + (\beta + 1) R_E} \tag{5.5.56}$$

$$S_\beta = \frac{I_{C_1}}{\beta_1} \frac{R_B + R_E}{R_B + (\beta_2 + 1) R_E} \cong \frac{I_{C_1}}{\beta_1} \frac{1}{1 + \frac{(\beta_2 + 1) R_E}{R_B}} \tag{5.5.57}$$

C. For the **voltage-divider bias** circuit with $(\beta+1)R_E \geq 10R_{BB}$, the stability factors are given by

$$S_{I_{CO}} = (\beta+1)\,\frac{R_{BB}+R_E}{R_{BB}+(\beta+1)\,R_E} \cong 1+\frac{R_{BB}}{R_E} \tag{5.5.58}$$

$$S_{V_{BE(ON)}} = \frac{-\beta}{R_{BB}+(\beta+1)\,R_E} \cong \frac{-1}{R_E} \tag{5.5.59}$$

$$S_\beta = \frac{I_{C_1}}{\beta_1}\,\frac{R_{BB}+R_E}{R_{BB}+(\beta_2+1)\,R_E} \cong \frac{I_{C_1}}{\beta_1\beta_2}\left(1+\frac{R_{BB}}{R_E}\right) \tag{5.5.60}$$

D. For the **collector feedback bias** circuit, i.e., $R_{BB}=R_F$, replacing $R_E$ with $R_{CE}=R_C+R_E$ and $R_F \gg R_{CE}$, the stability factors are given by

$$S_{I_{CO}} = (\beta+1)\,\frac{R_F+R_{CE}}{R_F+(\beta+1)\,R_{CE}} \cong \frac{\beta+1}{1+\dfrac{(\beta+1)\,R_{CE}}{R_F}} \tag{5.5.61}$$

$$S_{V_{BE(ON)}} = \frac{-\beta}{R_F+(\beta+1)\,R_{CE}} \tag{5.5.62}$$

$$S_\beta = \frac{I_{C_1}}{\beta_1}\,\frac{R_F+R_{CE}}{R_F+(\beta_2+1)\,R_{CE}} \cong \frac{I_{C_1}}{\beta_1}\,\frac{1}{1+\dfrac{(\beta_2+1)\,R_{CE}}{R_F}} \tag{5.5.63}$$

**Example 5.7:** Find and compare the collector current change $\Delta I_C$ when the temperature rises from 25 °C to 100 °C for the transistor defined by the table below for the following bias arrangements.

a. Fixed-bias with $R_B = 240\,\text{k}\Omega$ and $I_{C_1} = 2\,\text{mA}$,

b. Voltage-divider bias with $R_E = 4.7\,\text{k}\Omega$, $R_{BB}/R_E = 2$ and $I_{C_1} = 2\,\text{mA}$.

| **Temperature** | $\boldsymbol{I_{CO}}$ | $\boldsymbol{\beta}$ | $\boldsymbol{V_{BE(ON)}}$ |
|---|---|---|---|
| −65 °C | 0.02 nA | 20 | 0.85 V |
| 25 °C | 0.1 nA | 50 | 0.65 V |
| 100 °C | 20 nA | 80 | 0.48 V |
| 175 °C | 3.3 μA | 120 | 0.30 V |

**Solution:** From the table above, let us first calculate $\Delta I_{CO}$, $\Delta\beta$ and $\Delta V_{BE(ON)}$

$$\Delta I_{CO} = I_{CO_2} - I_{CO_1} = 20n - 0.1n = 19.9\,\text{nA}$$
$$\Delta\beta = \beta_2 - \beta_1 = 80 - 50 = 30$$
$$\Delta V_{BE(ON)} = V_{BE(ON)_2} - V_{BE(ON)_1} = 0.48 - 0.65 = -0.17\,\text{V}$$

We are goiung to calculate $\Delta I_C$ using

$$\Delta I_C \cong S_{I_{CO}}\Delta I_{CO} + S_\beta\Delta\beta + S_{V_{BE(ON)}}\Delta V_{BE(ON)}$$

a. Let us calculate the stability factors for the fixed-bias circuit using (5.5.52), (5.5.54) and (5.5.53)

$$\begin{aligned} S_{I_{CO}} &= \beta + 1 = 51 \\ S_\beta &= \frac{I_{C_1}}{\beta_1} = \frac{2m}{50} = 0.04\,\text{mA} \\ S_{V_{BE(ON)}} &= \frac{-\beta}{R_B} = \frac{-50}{240k} = -0.21\,\text{m}\Omega^{-1} \end{aligned}$$

Thus, $\Delta I_C$ is given by

$$\begin{aligned} \Delta I_C &\cong (51)(19.9n) + (0.04m)(30) + (-0.21m)(-0.17) \\ &= 1.02\mu + 1.2m + 0.036m \\ &= 1.236\,\text{mA} \end{aligned}$$

That means, for the fixed-bias circuit $I_C$ increases to 3.236 mA at 100 °C from 2 mA.

b. Let us calculate the stability factors for the voltage-divider bias circuit using (5.5.58), (5.5.60) and (5.5.59)

$$\begin{aligned} S_{I_{CO}} &\cong 1 + \frac{R_{BB}}{R_E} = 1 + 2 = 3 \\ S_\beta &\cong \frac{I_{C_1}}{\beta_1\beta_2}\left(1 + \frac{R_{BB}}{R_E}\right) = \frac{2m}{(50)(80)}(1+2) = 1.5\,\mu\text{A} \\ S_{V_{BE(ON)}} &= \frac{-1}{R_E} = \frac{-1}{4.7k} = -0.21\,\text{m}\Omega^{-1} \end{aligned}$$

Thus, $\Delta I_C$ is given by

$$\begin{aligned} \Delta I_C &\cong (3)(19.9n) + (1.5\mu)(30) + (-0.21m)(-0.17) \\ &= 0.060\mu + 0.045m + 0.036m \\ &= 0.081\,\text{mA} \end{aligned}$$

That means, for the voltage-divider bias circuit $I_C$ increases to 2.08 mA at 100 °C from 2 mA. Most of the improvement comes from the reduction in $S_\beta$.

- These two results show that voltage-divider bias circuit is much more stable than the fixed-bias circuit. In other words, adding $R_E$ resistor to the emitter leg of the transistor stabilizes the bias circuit.

### 5.5.2 Stability of Transistor Circuits with Active Components

- $V_{BE}$ compensation
  - by using a reverse-biased diode at the emitter

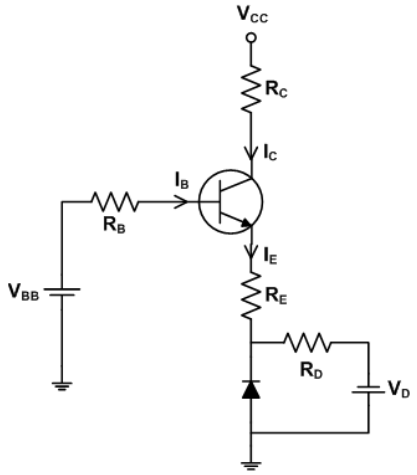



Figure 5.34: Active $V_{BE}$ compensation using a reverse-biased diode at the emitter.

- $I_{CO}$ compensation
  - by replacing $R_2$ with a reverse-biased diode

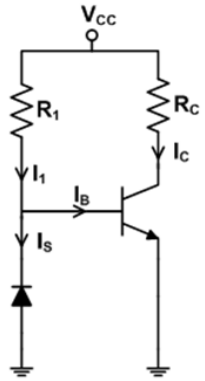



Figure 5.35: Active $I_{CO}$ compensation replacing $R_2$ with a reverse-biased diode.

- $I_C$ compensation (without $R_E$)
  - by using a current mirror

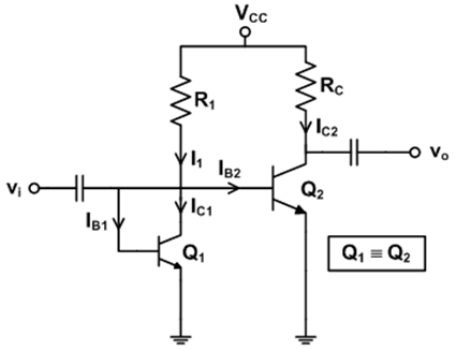



Figure 5.36: Active $I_C$ compensation using a current mirror.

## 5.6 Practical Applications

### 5.6.1 Relay Driver

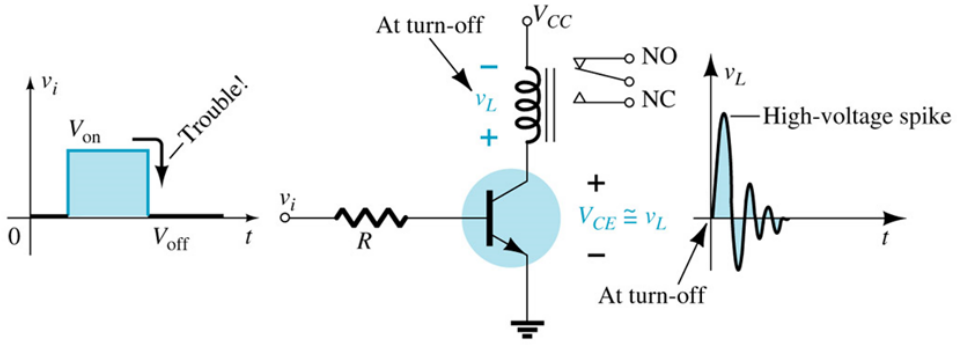



Figure 5.37: Relay driver in the absence of protective device.

When the transistor turns OFF, a high voltage (given by $v_L = L\,(di_L/dt)$) is induced across the coil as shown in Figure 5.38 above. If its magnitude exceeds the maximum ratings of the transistor, then the semiconductor device will be permanently damaged.

This destructive action can be subdued by placing a diode across the coil as shown in Figure 5.38 below. During the ON state of the transistor, the diode is reverse-biased (i.e., open circuit) and doesn't affect a thing. However, when the transistor turns off, the voltage across the coil will reverse and will forward-bias the diode, placing the diode in its ON state (hence protecting the transistor).

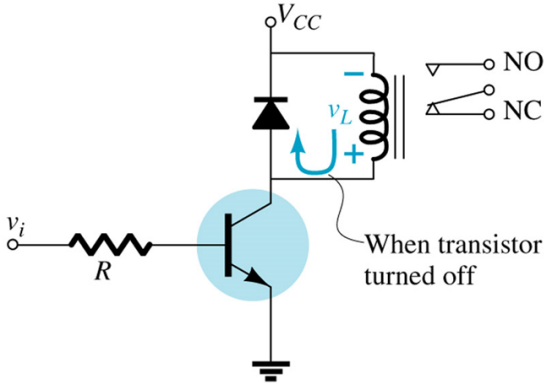



Figure 5.38: Relay driver protected with a diode across the relay coil.

### 5.6.2 Transistor Switch

A transistor can be used as a switch to control the ON and OFF states of the light-bulb in the collector branch of the circuit as shown in Figure 5.39 below.

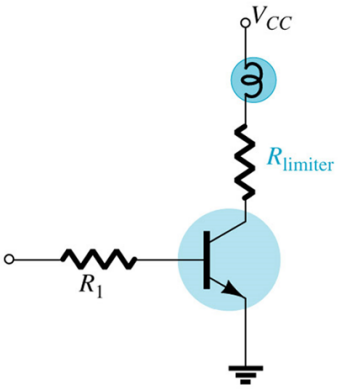



Figure 5.39: Using the BJT as a switch to control the onâĂŞoff states of a bulb with a limiting resistor.

### 5.6.3 Transistor Switching Networks

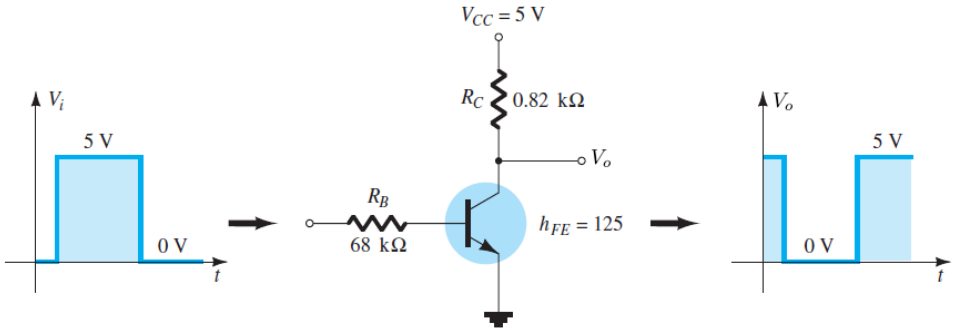



Figure 5.40: A BJT inverter circuit and its operation.

The application of transistors is not limited solely to the amplification of signals. Through proper design, transistors can also be used as switches for computer and control applications. The circuit shown in Figure 5.40 above can be employed an inverter in computer logic circuitry.

Inversion process requires that the $Q$-point switch from **cutoff** ($V_o = V_{CE(cutoff)} = 5\,\text{V}$) to **saturation** ($V_o = V_{CE(sat)} = 0\,\text{V}$) along the load line depicted in Figure 5.41 below.

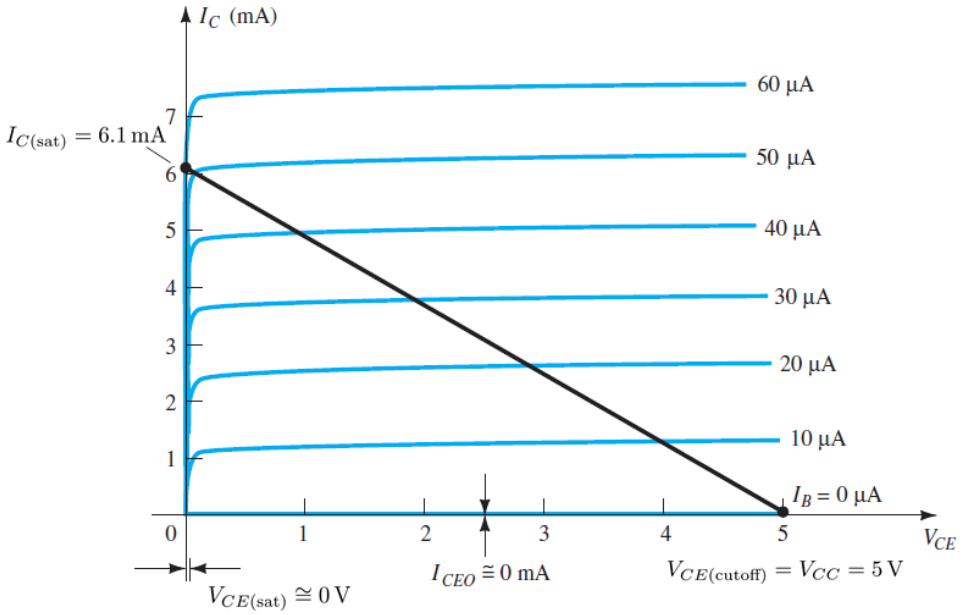



Figure 5.41: Load-line of the inverter circuit in Figure 5.40.

The total time required for the transistor to switch from the OFF to the ON state is designated as $t_{on}$, and he total time required for a transistor to switch from the ON to the OFF state is referred to as $t_{off}$ as shown in Figure 5.42 below. $t_{on}$ and $t_{off}$ are defined by

$$t_{on} = t_r + t_d \tag{5.6.64}$$

$$t_{off} = t_s + t_f \tag{5.6.65}$$

where $t_r$ is the rise time from 10% to 90% of the output, $t_d$ is the delay time between the changing state of the input and the beginning of a response at the output, $t_s$ is the storage time and and $t_f$ the fall time from 90% to 10% of the output.

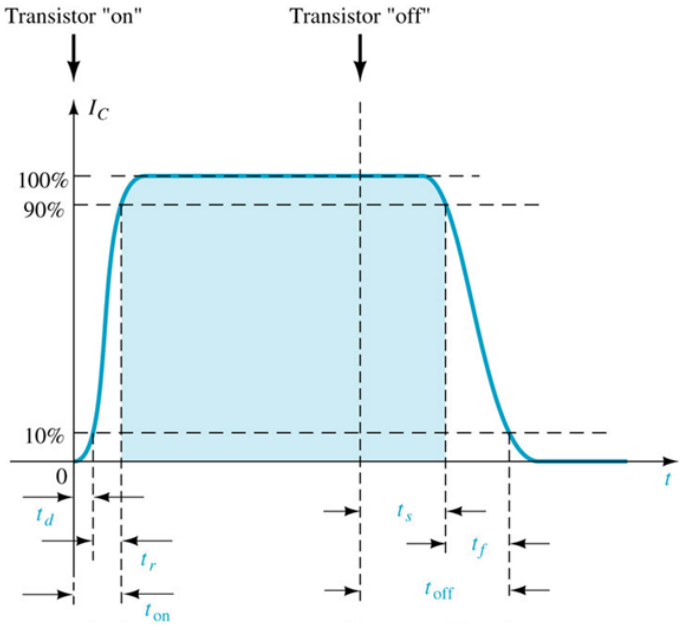
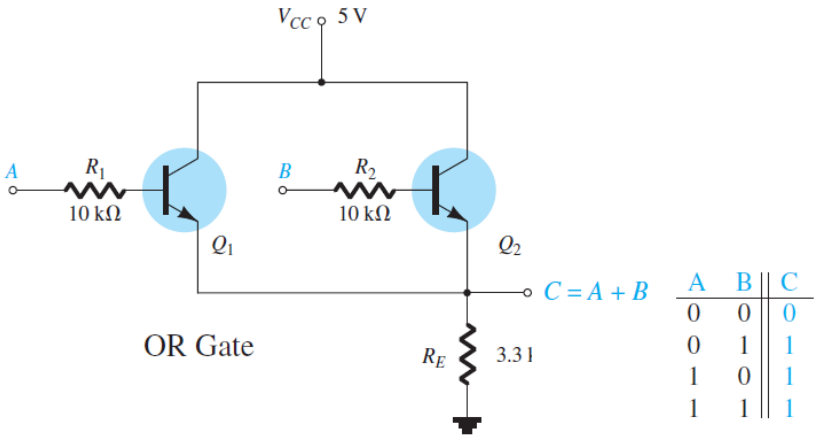



Figure 5.42: Defining the time intervals of a pulse waveform.

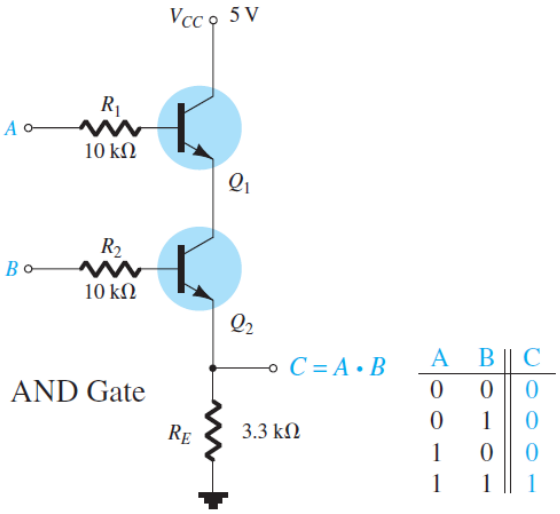
### 5.6.4 Logic Gates




| A | B | C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Figure 5.43: BJT logic OR gate.

Figure 5.43 above shows a BJT logic OR gate, and similarly Figure 5.44 below shows a BJT logic AND gate.




| A | B | C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Figure 5.44: BJT logic AND gate.

### 5.6.5 Current Mirror

The **current mirror** shown in Figure 5.45 below is a DC circuit in which the current through a **load** is controlled by a current at another point in the circuit. That is, the current through the load is indepedent of the load.

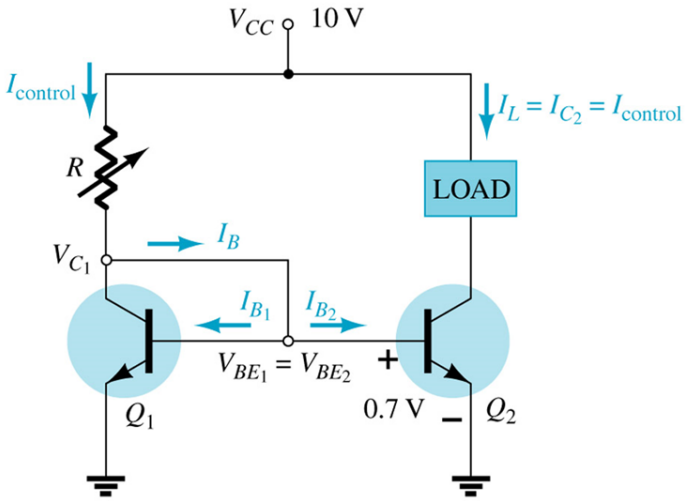



Figure 5.45: BJT logic OR gate.

**Homework 5.1:** For Figure 5.45 above, show that the load current is equal to the load control current and given by

$$I_L \cong I_{control} = \frac{V_{CC} - V_{BE(ON)}}{R} \tag{5.6.66}$$

where the transistors are identical ($Q_1 \equiv Q_2$), i.e., $V_{BE_1(ON)} = V_{BE_2(ON)} = V_{BE(ON)}$ and $\beta_1 = \beta_2 = \beta$, and current gain $\beta$ is high, e.g., $\beta \geq 100$.

### 5.6.6 Voltage Level Indicator

The voltage level indicator circuit uses a green LED to indicate when the source voltage is close to its monitoring level of 9 V. The potentiometer is set to establish 5.4 V at the point indicated in Figure 5.46 below. The result is sufficient voltage to turn on both the 4.7 V Zener and the transistor and establish a collector current through the LED sufficient in magnitude to turn on the green LED. The LED will immediately turn off, revealing that the supply voltage has dropped below 9 V or that the power source has been disconnected (i.e., when the voltage set up by the voltage divider circuit drops below 5.4 V).

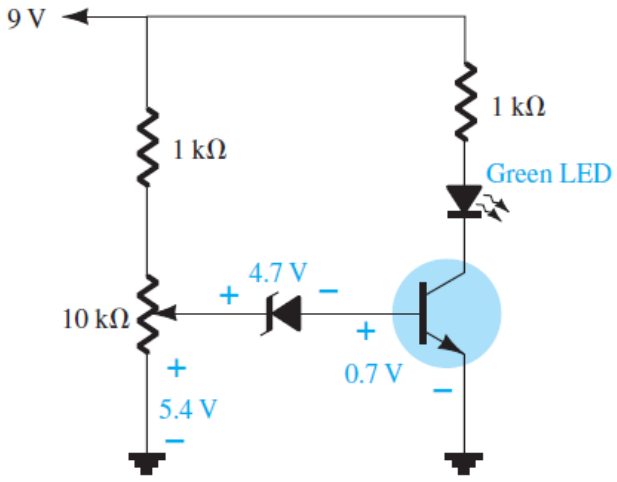



Figure 5.46: Voltage level indicator.

# Chapter 6

# AC-DC Load Lines of BJT Circuits

## 6.1 BJT AC Analysis

1. Draw the AC equivalent circuit (signal frequency is infinity, i.e., $f = \infty$)
   a) Capacitors are short circuit, i.e., $X_C \to 0$.
   b) Kill the DC power sources (short-circuit DC voltage sources and open-circuit DC current sources).
2. Write KVL for the loop which contains $CE$ terminals
   a) Develop AC load-line equation.
3. Draw AC-DC load lines
   a) Find available swings for a given input or find maximum undistorted swings.

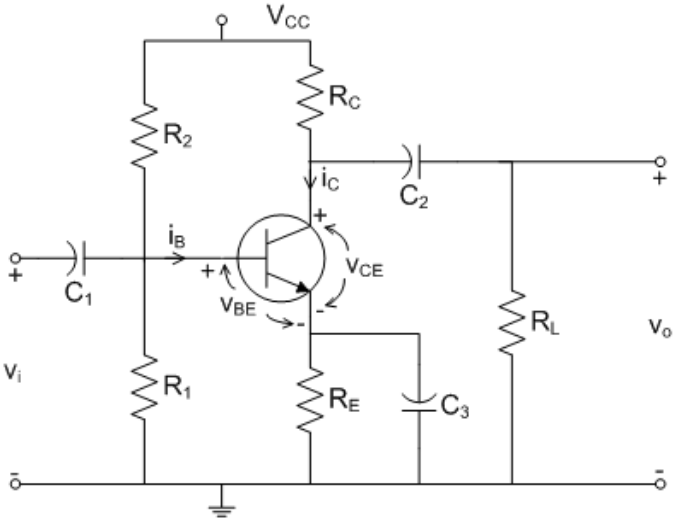



Figure 6.1: A voltage-divider common-emitter BJT circuit.

Consider the common-emitter BJT circuit shown in Figure 6.1 above where $v_i = V_m \sin(\omega t)$. Its DC and AC equivalent circuits are shown in Figure 6.2 below.

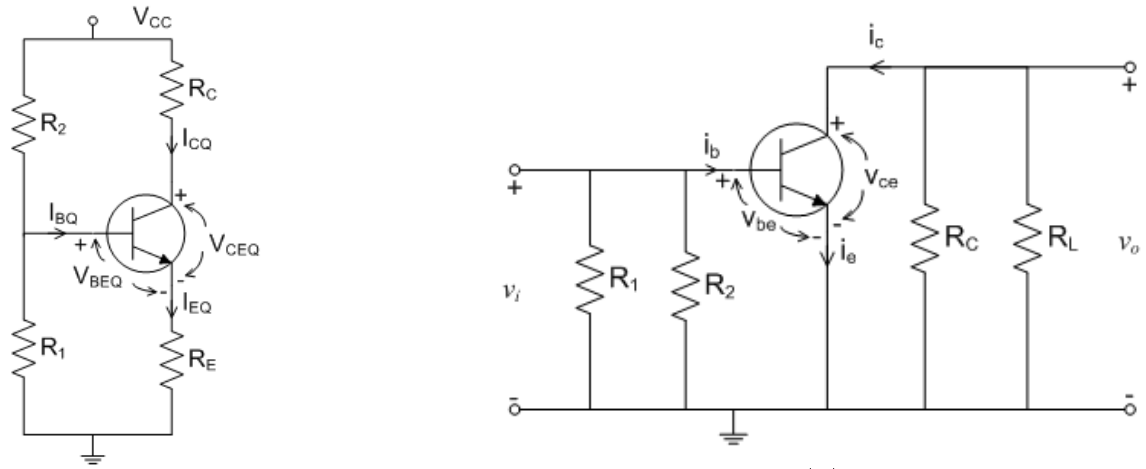



Figure 6.2: DC and AC equivalent circuits of the common-emitter circuit in Figure 6.1: (a) DC equivalent circuit (b) AC equivalent circuit.

### 6.1.1 DC Load Line

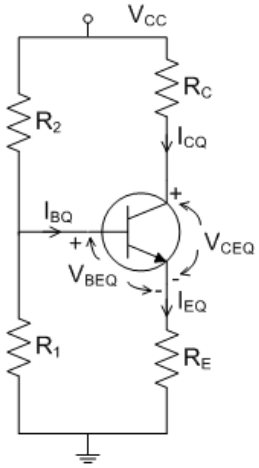



Figure 6.3: DC equivalent circuit of Figure 6.1.

DC equivalent circuit shown in Figure 6.3 above, let us first define the equivalent output-loop ($CE$-loop) DC resistance $R_{DC}$ and $V_{CE}$ as follows

$$R_{DC} = R_C + R_E \tag{6.1.1}$$

$$V_{CE} = V_{CC} - I_C R_{DC} \tag{6.1.2}$$

Thus, the rearranged **DC load line equation** (DC output equation) is given by

$$\boxed{I_C = \frac{-1}{R_{DC}} V_{CE} + \frac{V_{CC}}{R_{DC}}} \tag{6.1.3}$$

Note that, AC swings are around the $Q$-points. Here, input swing $v_{be} = v_i$ in Figure 6.4(a) below is around the input $Q$-point ($I_{BQ}$, $V_{BEQ}$), and output swing $v_o = v_{ce}$ in Figure 6.4(b) below is around the output $Q$-point ($I_{CQ}$, $V_{CEQ}$).

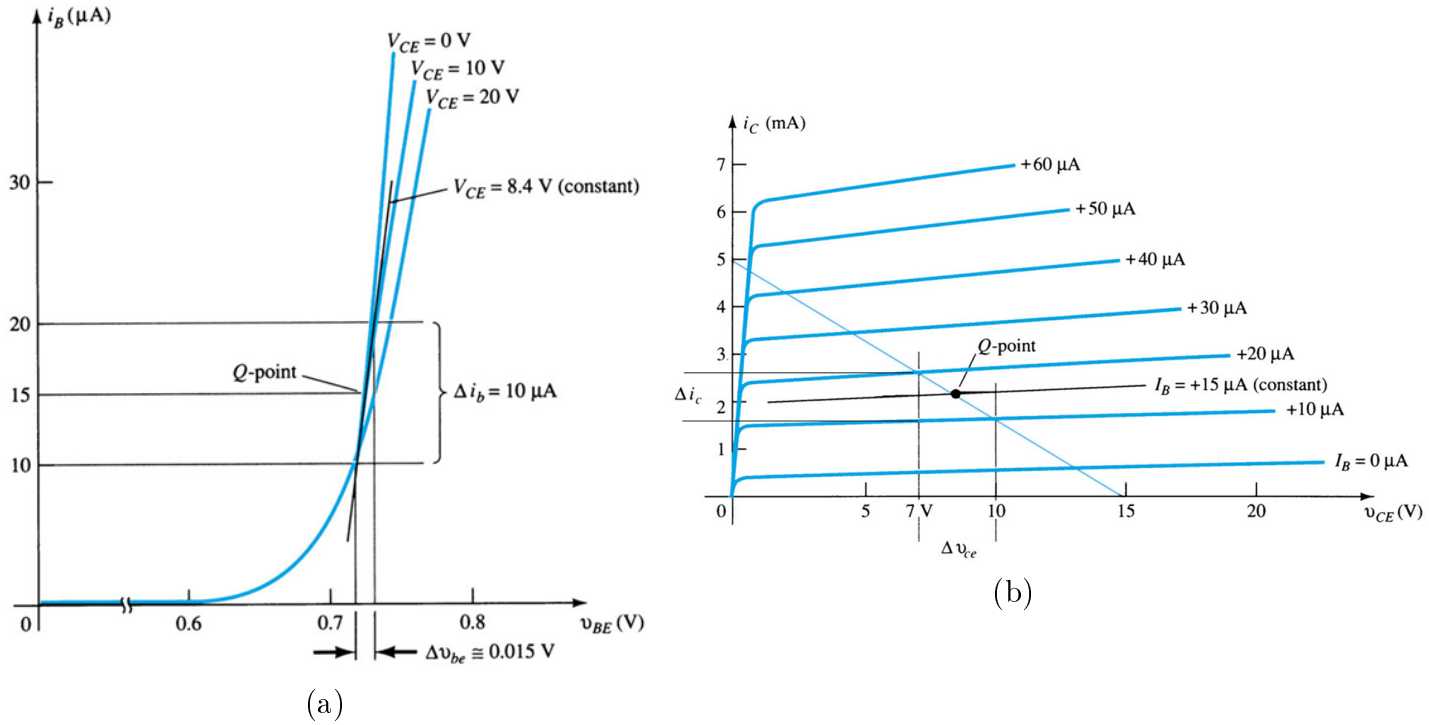
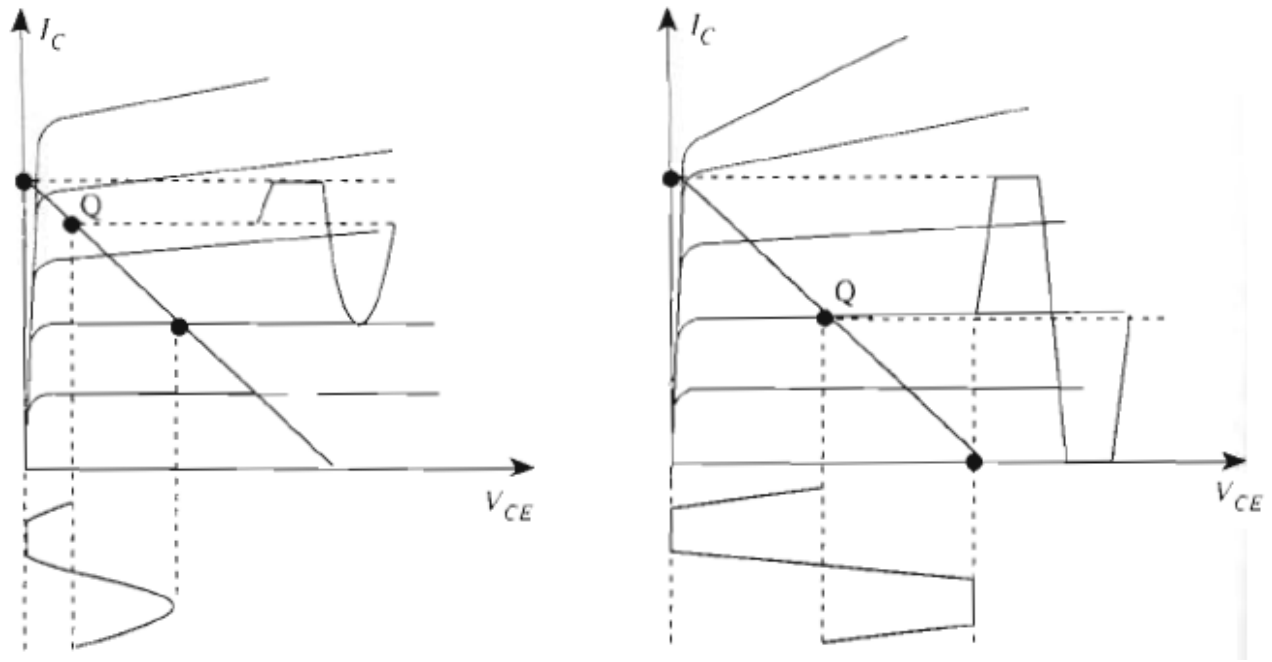



Figure 6.4: Input and output swings around the $Q$-points: (a) input swing (b) output swing.

### 6.1.2 Distortion

If the $Q$-point is incorrect as shown in Figure 6.5(a) below, or if the input is too high as shown in Figure 6.5(b) below, then the output swings (for a sinusoidal input) as shown in the figures below will be **distorted**, i.e., not the same shape as the input waveform.

NOTE: Load-lines shown in the figures below are the AC load-lines which we will derive in the next section.




(a) (b)

Figure 6.5: Distorted output swings: (a) incorrect $Q$-point (b) incorrect input (i.e., high input).

### 6.1.3 AC Load Line

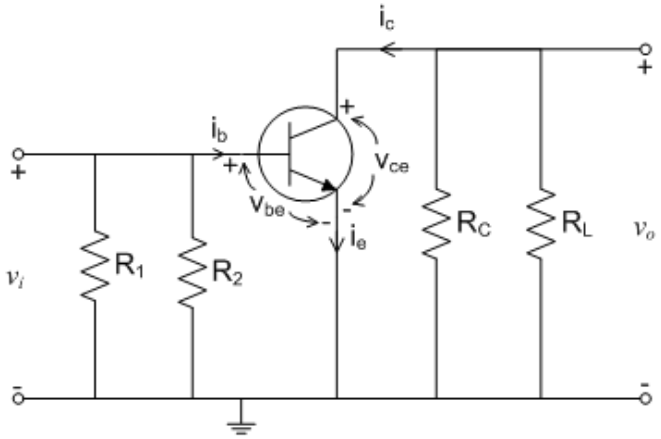



Figure 6.6: AC-equivalent circuit of Figure 6.1.

AC equivalent circuit shown in Figure 6.6 above, let us first define the equivalent output-loop ($CE$-loop) AC resistance $R_{ac}$ and output $v_o$ as follows

$$R_{ac} = R_C || R_L \tag{6.1.4}$$

$$v_o = v_{ce} = -i_c R_{ac} \tag{6.1.5}$$

Let us now define the AC+DC output signals $i_C$ and $v_{CE}$ as follows

$$i_C = i_c + I_{CQ} \tag{6.1.6}$$

$$v_{CE} = v_{ce} + V_{CEQ} \tag{6.1.7}$$

Now let us express the AC output equation $v_{ce} = -i_c R_{ac}$ in terms of $v_{CE}$ and $i_C$ so that we can draw this equation over the output characteristics curve as the AC load line equation.

$$v_{ce} = -i_c R_{ac} \tag{6.1.8}$$

$$v_{CE} - V_{CEQ} = -(i_C - I_{CQ}) R_{ac} \tag{6.1.9}$$

$$v_{CE} = -i_C R_{ac} + V_{CEQ} + I_{CQ} R_{ac} \tag{6.1.10}$$

Thus, the rearranged **AC load line equation** (AC output equation) is given by

$$\boxed{i_C = \frac{-1}{R_{ac}} v_{CE} + I_{CQ} + \frac{V_{CEQ}}{R_{ac}}} \tag{6.1.11}$$

### 6.1.4 AC-DC Load Lines

Let us draw DC ($V_{CE} = v_{ce} + V_{CEQ}$) and AC ($v_{CE} = -i_C R_{ac} + V_{CEQ} + I_{CQ} R_{ac}$) load lines together as shown in Figure 6.7 below.

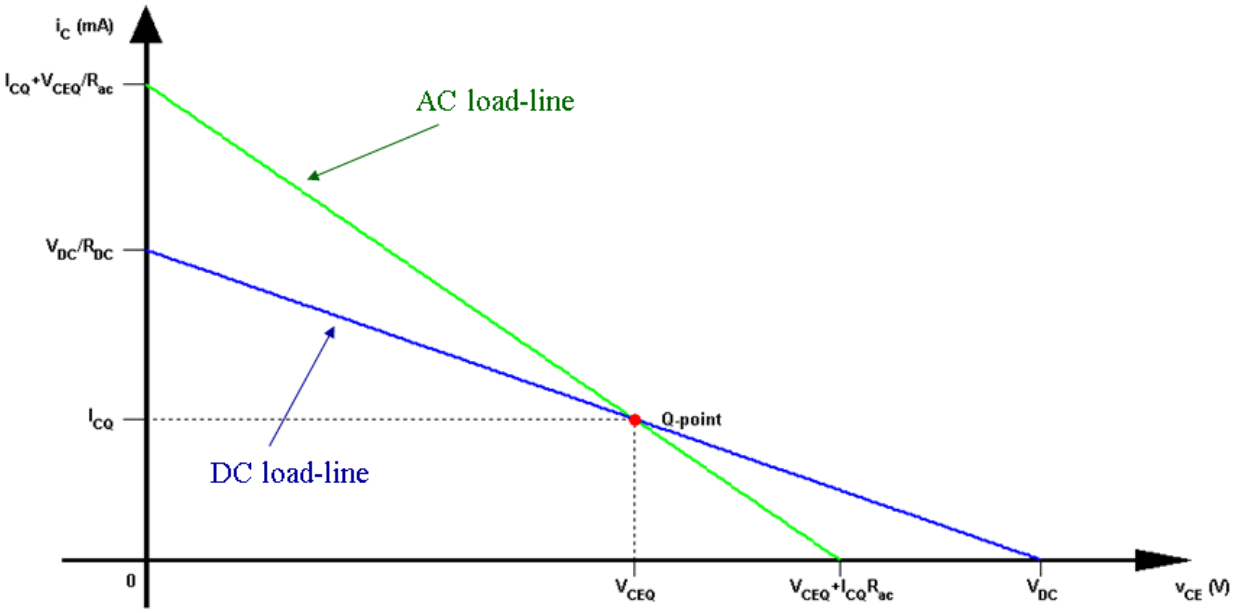



Figure 6.7: AC-DC load lines.

**Output swings** are defined with respect to the ***Q*-point** $(I_{CQ}, V_{CEQ})$ and the **AC load line end points** on the axes.

**Homework 6.1:** Show that AC and DC load lines are the **same** if $R_{DC} = R_{ac}$.

Once the $Q$-point is known, i.e., the resistor values are given, **peak** values of the **maximum undistorted** voltage and current **swings** $v_{ce(p)(\max)}$ and $i_{c(p)(\max)}$ are given by

$$\boxed{v_{ce(p)(\max)} = \min\left(V_{CEQ}, I_{CQ} R_{ac}\right)} \tag{6.1.12}$$

and

$$i_{c(p)(\max)} = \min\left(I_{CQ}, \frac{V_{CEQ}}{R_{ac}}\right) \tag{6.1.13}$$

respectively

#### 6.1.4.1 Maximum Symmetric Undistorted Swing Design

If we want design our circuit (i.e., select appropriate values for the resistors) in order to obtain the maximum available undistorted swing, i.e., to obtain $\max(\min(V_{CEQ}, I_{CQ}R_{ac}))$, then we obtain the following condition

$$\boxed{V_{CEQ} = I_{CQ}R_{ac}} \tag{6.1.14}$$

Thus, ***Q*-point** must be in the **middle** of the **AC load line**. In other words, maximum available negative and positive swings are symmetric.

Combining this AC load line requirement in (6.1.14) with the DC load-line equation given in (6.1.2), we find that we have to select the $Q$-point collector current as

$$\boxed{I_{CQ} = \frac{V_{CC}}{R_{DC} + R_{ac}}} \tag{6.1.15}$$

In order to attain this $Q$-point, we need to select appropriate values for the resistors in the $BE$ loop to obtain $I_{BQ} = \frac{I_{CQ}}{\beta}$.

Once we obtained the desired $Q$-point in the middle of the AC load line, then the maximum available undistorted output swings will be obtained as shown in Figure 6.8 below.

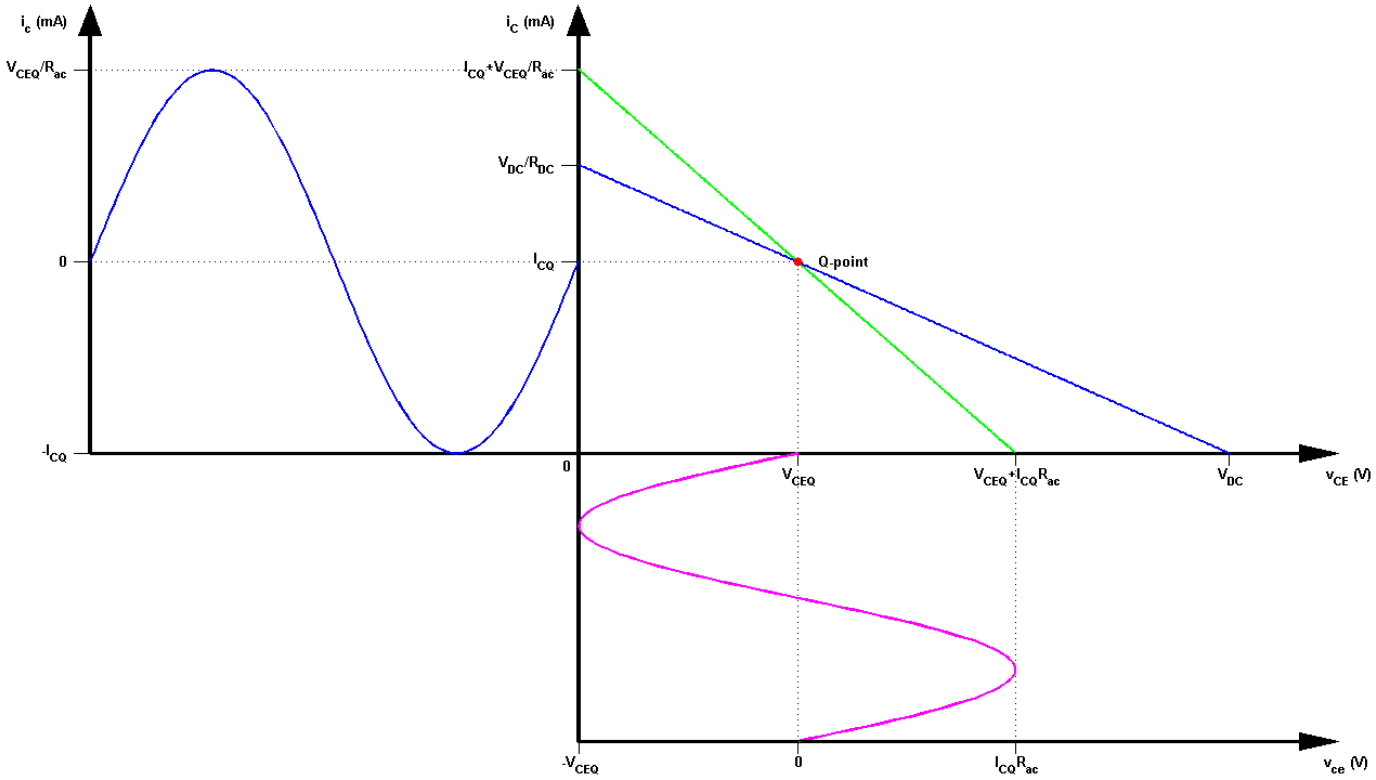



Figure 6.8: Maximum undistorted swing design with $Q$-point in the middle of the AC load line.

#### 6.1.4.2 Other Amplifier Configurations

We developed and plotted AC-DC load lines for the common-emitter configuration. Now, let us look at other configurations.

- Common-base (CB) configuration
  1. Obtain $R_{ac}$ from the $CB$ loop.
  2. Obtain $R_{DC}$ from the $CE$ loop.
  3. Draw the AC-DC load lines $i_C$ vs. $v_{CE}$ as before.

     NOTE: You can also draw the AC-DC load lines as $i_C$ vs. $v_{CB}$ by shifting the voltage axis by $V_{BE(ON)}$ volts to the left as $V_{CBQ} = V_{CEQ} - V_{BE(ON)}$. Thus, current axis will be drawn at $V_{CB(sat)} = V_{CE(sat)} - V_{BE(ON)} = 0 - V_{BE(ON)} = -V_{BE(ON)}$ volts not at 0 V.
- Common-collector (CC) configuration (also known as emitter-follower)
  1. Obtain $R_{ac}$ and $R_{DC}$ from the $CE$ loop as before.
  2. Draw the AC-DC load lines $i_E$ vs. $v_{CE}$.

     NOTE: As $i_E \cong i_C$, it will be the same as drawing $i_C$ vs. $v_{CE}$.
- For *pnp* transistors, we express the currents in the reverse direction (i.e., having positive current values) and reverse the polarity of the terminal voltages (i.e., having positive voltage values), and then draw the AC-DC load lines, e.g., $i_C$ vs. $v_{EC}$.

**Example 6.1:** Consider the circuit below with $I_{BQ} = 50\,\mu\text{A}$, $I_{CQ} = 13\,\text{mA}$ and $\alpha \cong 1$.

a) If $i_i = 50\,\mu\text{A}\sin(\omega t)$, find $i_C$ and $v_{CE}$.

b) Plot AC and DC load lines together with the output voltage and current swings.

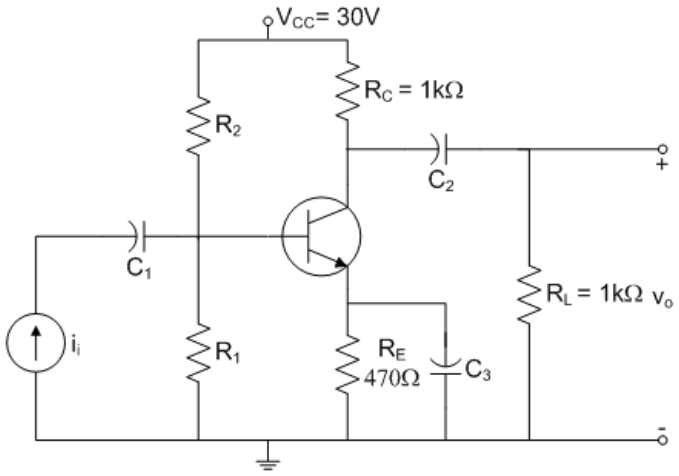



Figure 6.9: BJT amplifier circuit for Example 6.1.

**Solution:** Here $\beta_{ac} = \beta_{DC} = \beta = \frac{I_{CQ}}{I_{BQ}} = \frac{13m}{50\mu} = 260$, $R_{DC} = R_C + R_E = 1k + 0.47k = 1.47\,\text{k}\Omega$ and $R_{ac} = R_C||R_L = 1k||1k = 0.5\,\text{k}\Omega$. So, we can find $V_{CEQ}$ as

$$V_{CEQ} = V_{CC} - I_{CQ}R_{DC} = 30 - (13m)(1.47k) = 10.89\,\text{V}\sin(\omega t).$$

As $i_b \cong i_i$, we can find $i_c$ and $v_{ce}$ as

$$i_c = \beta_{ac} i_b \cong \beta i_i = (260)(50\mu) = 13\,\text{mA}\sin(\omega t)$$
$$v_{ce} = -i_c R_{ac} = -(13m)(0.5k) = -6.5\,\text{V}\sin(\omega t)).$$

We find $i_C$ and $v_{CE}$ as

$$i_C = I_{CQ} + i_c = 13\,\text{mA} + 13\,\text{mA}\sin(\omega t)$$
$$v_{CE} = V_{CEQ} + v_{ce} = 10.89\,\text{V} - 6.5\,\text{V}\sin(\omega t)$$

Thus, the AC-DC load-lines are shown in Figure 6.10 below

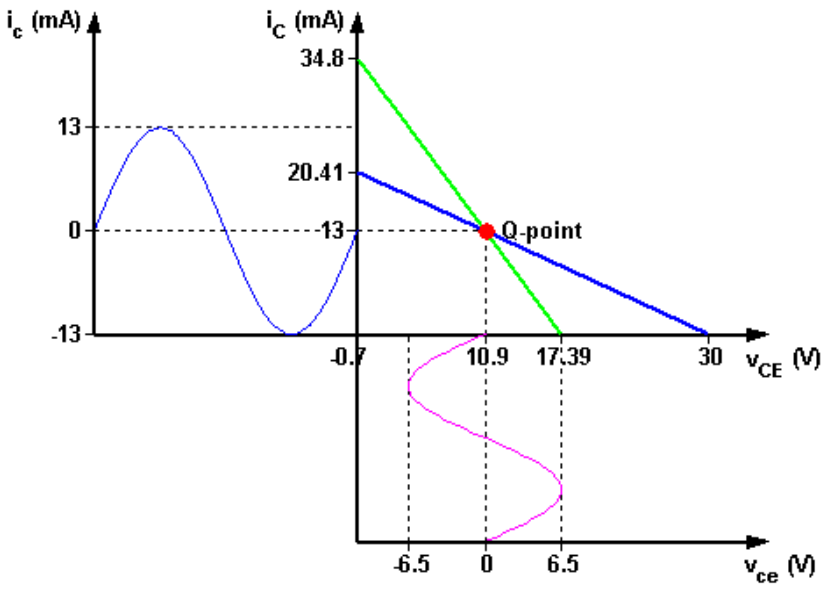



Figure 6.10: AC-DC load-lines for Example 6.1.

**Example 6.2:** Consider the circuit below with $\alpha \cong 1$.

a) Determine the $Q$-point in order to obtain maximum undistorted current swing.

b) Draw AC and DC load lines.

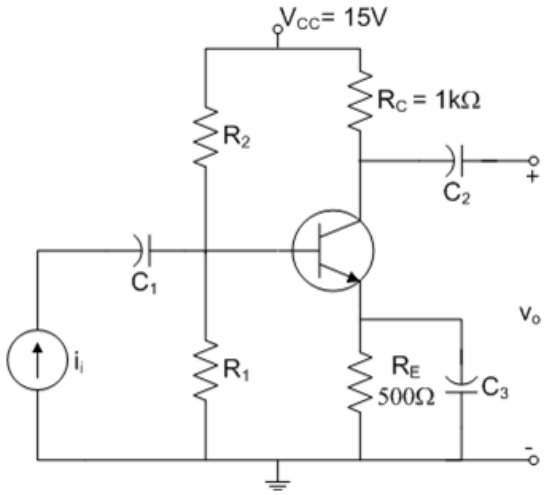



Figure 6.11: BJT amplifier circuit for Example 6.2.

**Solution:** We can design this circuit to have maximum symmetric undistorted output swing and select $R_1$ and $R_2$ values accordingly. So, from the figure $R_{DC} = R_C + R_E = 1k + 0.5k = 1.5\,\text{k}\Omega$ and $R_{ac} = R_C = 1\,\text{k}\Omega$. Thus,

$$I_{CQ} = \frac{V_{CC}}{R_{DC} + R_{ac}} = \frac{15}{1.5k + 1k} = 6\,\text{mA}$$
$$V_{CEQ} = V_{CC} - I_{CQ}R_{DC} = 15 - (6m)(1.5k) = 6\,\text{V}$$

Maximum available swings $i_c$ and $v_{ce}$ are given as

$$i_c = 6\,\text{mA}\sin(\omega t)$$
$$v_{ce} = -6\,\text{V}\sin(\omega t)$$

Consequently, the AC-DC load-lines are shown in Figure 6.12 below

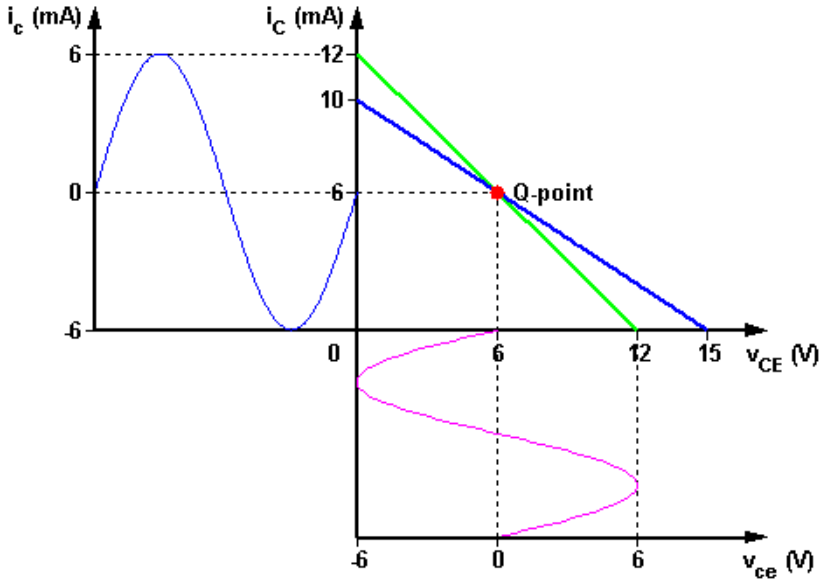



Figure 6.12: AC-DC load-lines for Example 6.2.

**Example 6.3:** (2004-2005 MI) Consider the common-emitter BJT amplifier in the figure below.

a) Explain briefly the effects of the capacitors $C_1$, $C_2$ and $C_3$ on DC biasing and AC operation.

b) Design the DC bias ($I_{CQ}$ and $V_{CEQ}$) for the **maximum undistorted output swing** and then find the values of $R_1$ and $R_2$ which satisfies this condition. Take $\beta R_E \geq 10(R_1||R_2)$, $V_{BE(ON)} = 0.7\,\text{V}$ and $\beta = 100$.

c) Draw the DC and AC load lines for this circuit and show the maximum voltage and current swings on the graph. Also, express these current and voltage swings in written form with their AC and DC components.

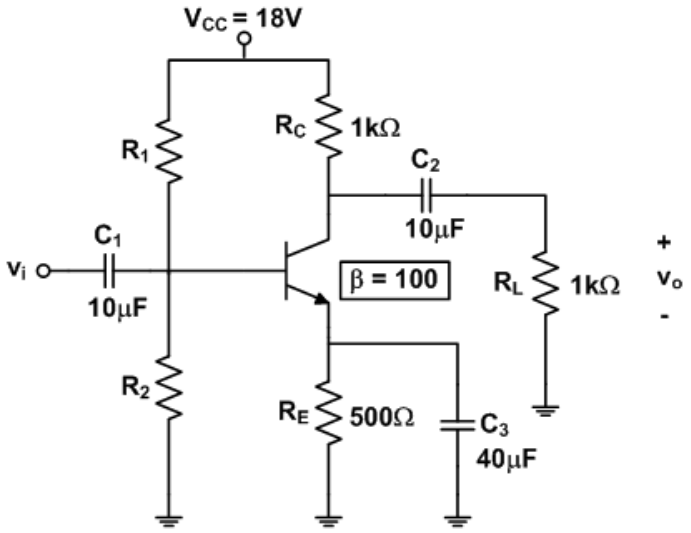



Figure 6.13: BJT amplifier circuit for Example 6.3.

**Solution:** a. Capacitors are open-circuit in DC operation. Thus, $C_1$ and $C_2$ are called the coupling capacitors for the protection of the $Q$-point of the amplifier from the input and output circuitries by preventing the circulation/leakage of DC signals and enabling only AC signals in and out. $C_3$ is called the emitter bypass capacitor ensuring the stability of the $Q$-point by enabling the emitter resistor to be in effect in DC operation and increasing the AC gain by bypassing the emitter resistor in AC operation.

b. We can design this circuit to have maximum symmetric undistorted output swing and select $R_1$ and $R_2$ values accordingly. So, from the figure $R_{DC} = R_C + R_E = 1k + 0.5k = 1.5\,\text{k}\Omega$ and $R_{ac} = R_C||R_L = 1k||1k = 0.5\,\text{k}\Omega$. Thus,

$$I_{CQ} = \frac{V_{CC}}{R_{DC} + R_{ac}} = \frac{18}{1.5k + 0.5k} = 9\,\text{mA}$$
$$V_{CEQ} = V_{CC} - I_{CQ}R_{DC} = 18 - (9m)(1.5k) = 4.5\,\text{V}$$

As $I_{EQ} \cong I_{CQ} = 9\,\text{mA}$, base voltage $V_{BQ}$ is given by

$$V_{BQ} = V_{BE(ON)} + I_{EQ}R_E = 0.7 + (9m)(0.5k) = 5.2\,\text{V}.$$

By making the assumption $\beta R_E \geq 10(R_1||R_2)$, we can ignore the base current $I_{BQ}$ and directly apply the voltage divider rule as

$$\begin{aligned}\frac{R_2}{R_1+R_2}V_{CC} &\cong V_{BQ}\\ \frac{R_1+R_2}{R_2} &= \frac{V_{CC}}{V_{BQ}}\\ \frac{R_1}{R_2} &= \frac{V_{CC}}{V_{BQ}} - 1 = \frac{18}{5.2} - 1 = 2.46.\end{aligned}$$

Let us take the highest value of $R_{BB} = R_1||R_2$ in order to reduce the currents through $R_1$ and $R_2$ as

$$R_{BB} = R_1||R_2 = \beta R_E/10 = 100 \times 0.5k/10 = 5\,\text{k}\Omega$$

If we take $a = \frac{R_1}{R_2} = 2.46$, then $R_{BB} = \frac{a}{a+1}R_2$. So, $R_2$ is given by

$$R_2 = \frac{a+1}{a}R_{BB} = \frac{2.46+1}{2.46}5k = 7.03\,\text{k}\Omega$$

Thus, $R_1$ is given by

$$R_1 = aR_2 = (2.46)(7.03k) = 17.29\,\text{k}\Omega$$

c. AC+DC output current $i_C$ and output voltage $v_{CE}$ are given by

$$\begin{aligned}i_C &= I_{CQ} + i_c = 9\,\text{mA} + 9\,\text{mA}\sin(\omega t)\\ v_{CE} &= V_{CEQ} + v_{ce} = 4.5\,\text{V} - 4.5\,\text{V}\sin(\omega t)\end{aligned}$$

Consequently, the AC-DC load-lines are shown in Figure 6.14 below

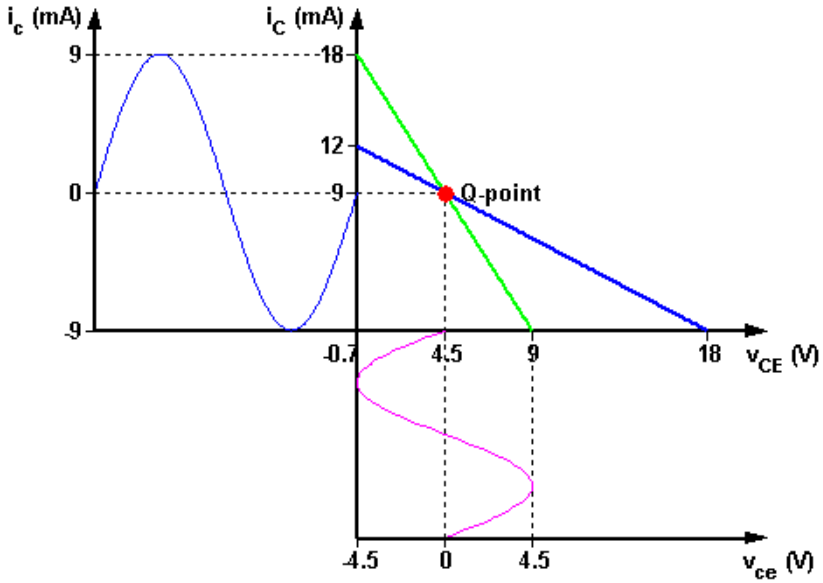



Figure 6.14: AC-DC load-lines for Example 6.3.

# Chapter 7

# Field Effect Transistors (FETs)

## 7.1 Similarities and Differences with BJTs

Field-effect transistors (FETs) are three-terminal devices used for a variety of applications that match, to a large extent, those of the BJTs.

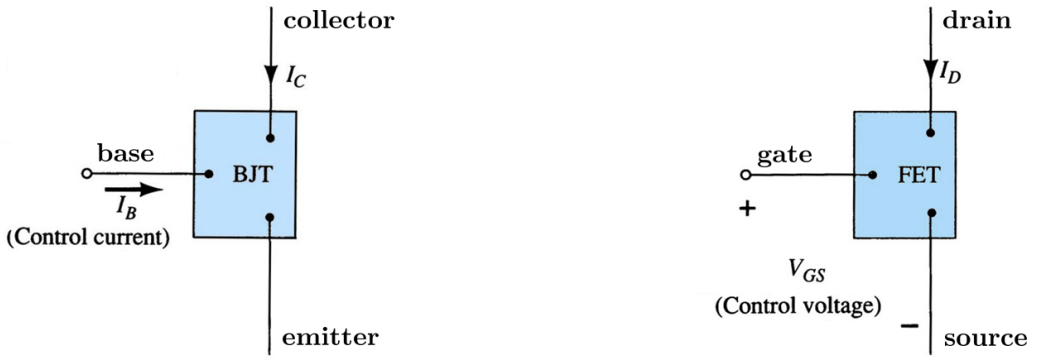
**Similarities:**

- Amplifiers
- Switching devices
- Impedance matching circuits

**Differences:**

- FETs are voltage controlled devices whereas BJTs are current controlled devices
- FETs also have a higher input impedance, but BJTs have higher gains
- FETs are less sensitive to temperature variations and because of their construction they are more easily integrated on ICs
- FETs are also generally more static sensitive than BJTs
- FETs have a poorer frequency response (i.e., lower gain-bandwidth product) than BJTs
- FETs have a higher output impedance than BJTs

BJT is a current-controlled device as depicted in Figure 7.1(a) below, whereas FET is a voltage-controlled device as shown in Figure 7.1(b) below.




(a) (b)

Figure 7.1: BJT (*npn*) and FET (*n*-channel) comparison: (a) current-controlled device (BJT), (b) voltage-controlled device (FET).

## 7.2 FET Types

We are going to cover three types (JFET, DMOSFET and EMOSFET) of field effect transistors (FETs)

- **JFET:** Junction Field-Effect Transistor
- **MOSFET:** Metal-Oxide-Semiconductor Field-Effect Transistor
  - **DMOSFET:** Depletion-type MOSFET
  - **EMOSFET:** Enhancement-type MOSFET

## 7.3 FET Operation

FET operation can be compared to a water spigot shown in Figure 7.2 below. Water flow signifies the charge flow. In *n*-channel FETs charge flow is the electron flow, and in *p*-channel FETs charge flow is the hole flow.

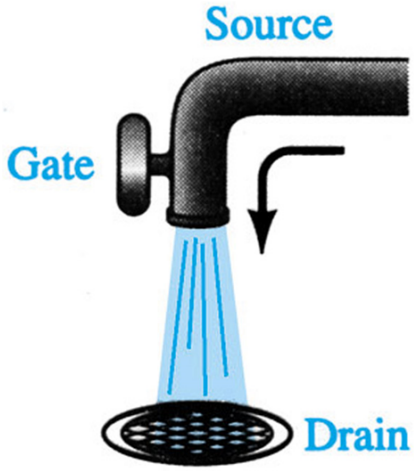



Figure 7.2: Water analogy for the FET control mechanism.

- The source of water pressure can be likened to the applied voltage from drain to source, which establishes a flow of water (charge) from the spigot (source) to the drain.
- The valve (gate), controls the flow of water (charge) to the drain by adjusting the width of the pipe (channel). In a FET, gate adjusts the width of the channel via the applied potential between gate and the source terminals.

## 7.4 Junction Field-Effect Transistor (JFET)

### 7.4.1 Construction

There are two types of JFETs: $n$-channel and $p$-channel. The $n$-channel whose construction is shown in Figure 7.3 below is more widely used. There are three terminals: Drain, Source and Gate.

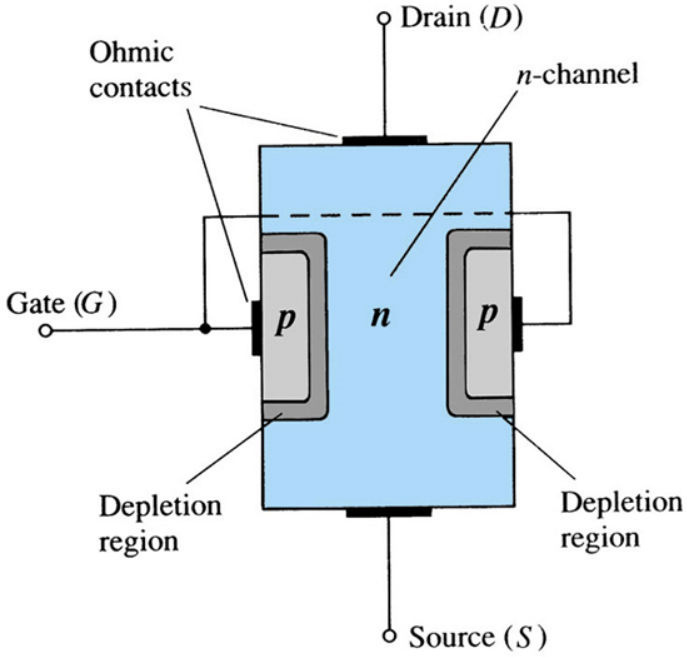



Figure 7.3: $n$-channel junction field-effect transistor (JFET) construction.

Here,

- Drain ($D$) and Source ($S$) are connected to $n$-channel.
- Gate ($G$) is connected to the $p$-type material.
- For correct operation, gate-channel $pn$ junction must be **reverse-biased**, i.e., $V_{GS} \leq 0$.

### 7.4.2 Operating Characteristics

There are three basic operating conditions for a JFET:

A. $V_{GS} = 0$ and $V_{DS} > 0$

B. $V_{GS} < 0$ and $V_{DS} > 0$

C. Voltage-controlled resistor

#### 7.4.2.1 $V_{GS} = 0$ and $V_{DS} > 0$

A positive voltage $V_{DS}$ is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0\,\text{V}$ as shown in Figure 7.4(a) below. Under these conditions the flow of charge is relatively uninhibited and is limited solely by the resistance of the $n$-channel between drain and source.

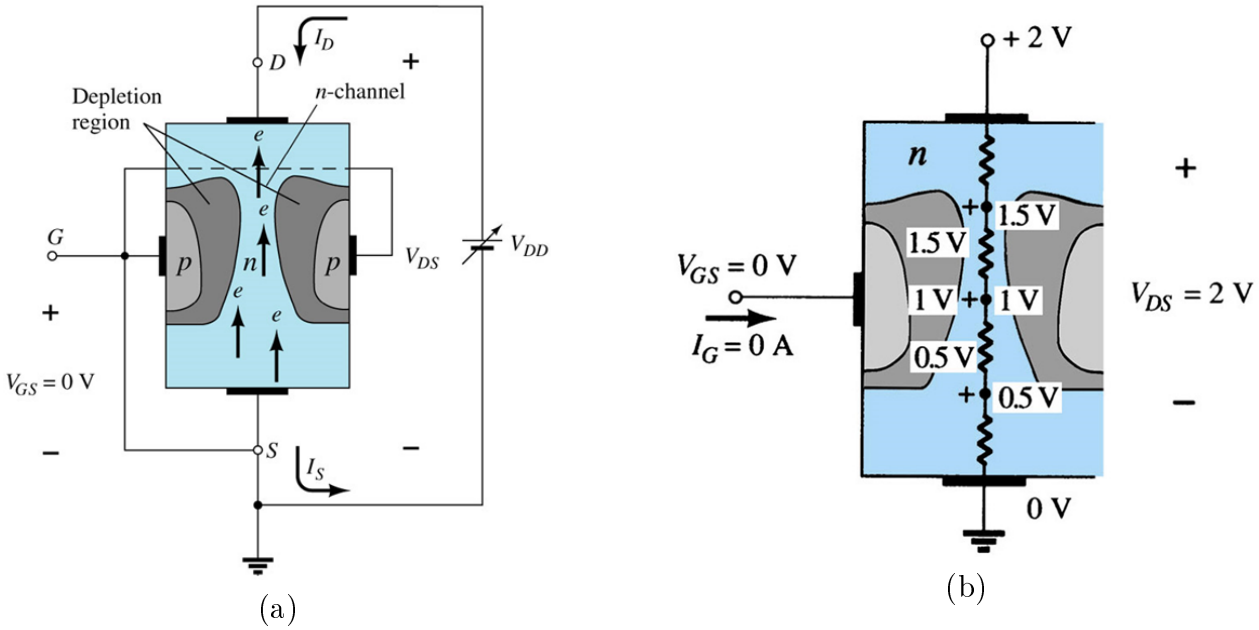



Figure 7.4: JFET at $V_{GS} = 0\,\text{V}$ and $V_{DS} > 0\,\text{V}$: (a) DC biasing, (b) variation of the gate-channel junction reverse-bias voltages through the channel.

It is important to note that the depletion region is wider near the top of both $p$-type materials. The reason for the change in width of the region is best described through the help of Figure 7.4(b) above. The result is that the upper region of the $p$-type material will be reverse-biased by around 1.5 V, with the lower region only reverse-biased by 0.5 V.

**Pinch-off**

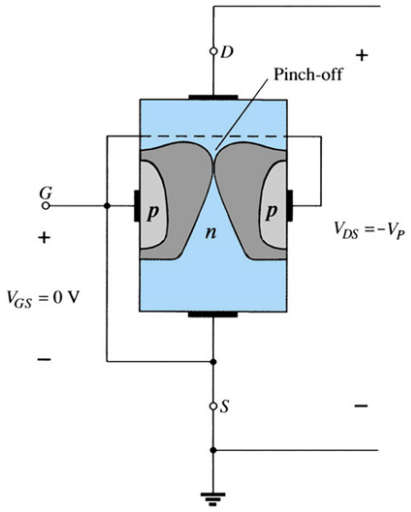



Figure 7.5: Pinch-off ($V_{GS} = 0\,\text{V}$, $V_{DS} = -V_P$).

If $V_{GS} = 0$ and $V_{DS}$ is further increased to a more positive voltage, then the depletion zone gets so large that it **pinches off** the $n$-channel as shown in Figure 7.5 above.

The level of $V_{DS}$ that establishes this condition is referred to as the **pinch-off voltage** and is denoted by $-V_P$.

At pinch-off, $I_D$ maintains a **saturation level** defined as $I_{DSS}$.

As $V_{DS}$ is increased beyond $-V_P$, the region of close encounter between the two depletion regions increases in length along the channel, but the level of $I_D$ remains essentially the same.

**Output characteristics for $V_{GS} = 0$**

The resultant output characteristics curve for $V_{GS} = 0\,\text{V}$ is shown in Figure 7.6 below.

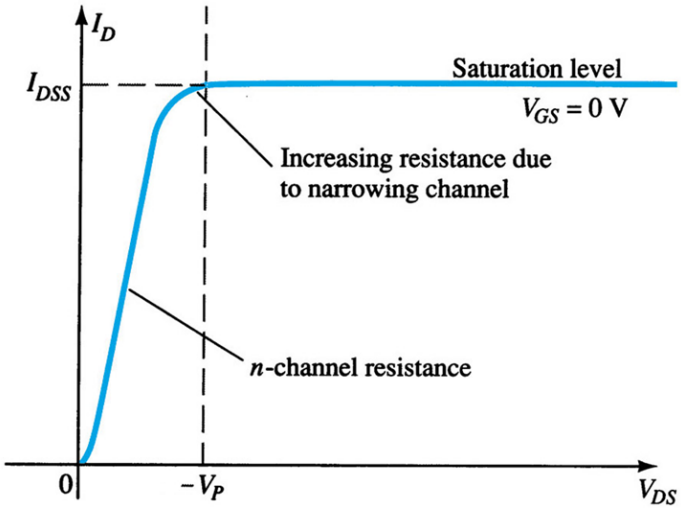



Figure 7.6: Output characteristics, i.e., $I_D$ versus $V_{DS}$, for $V_{GS} = 0\,\text{V}$.

#### 7.4.2.2 $V_{GS} < 0$ and $V_{DS} > 0$

As $V_{GS}$ is negative the depletion regions are larger from the beginning, thus channel is narrower from the beginning. So, the pinch-off will occur at lower voltage of $V_{DS(\text{sat})} = V_{GS} - V_P$, and the saturation current will be smaller than $I_{DSS}$. Once $V_{GS} = V_P$, the channel is blocked from the start, and no current flows, i.e., $I_D = 0$.

Consequently, when we draw the corresponding $IV$ curves for each $V_{GS}$, we obtain the complete **output characteristics** shown in Figure 7.7 below.

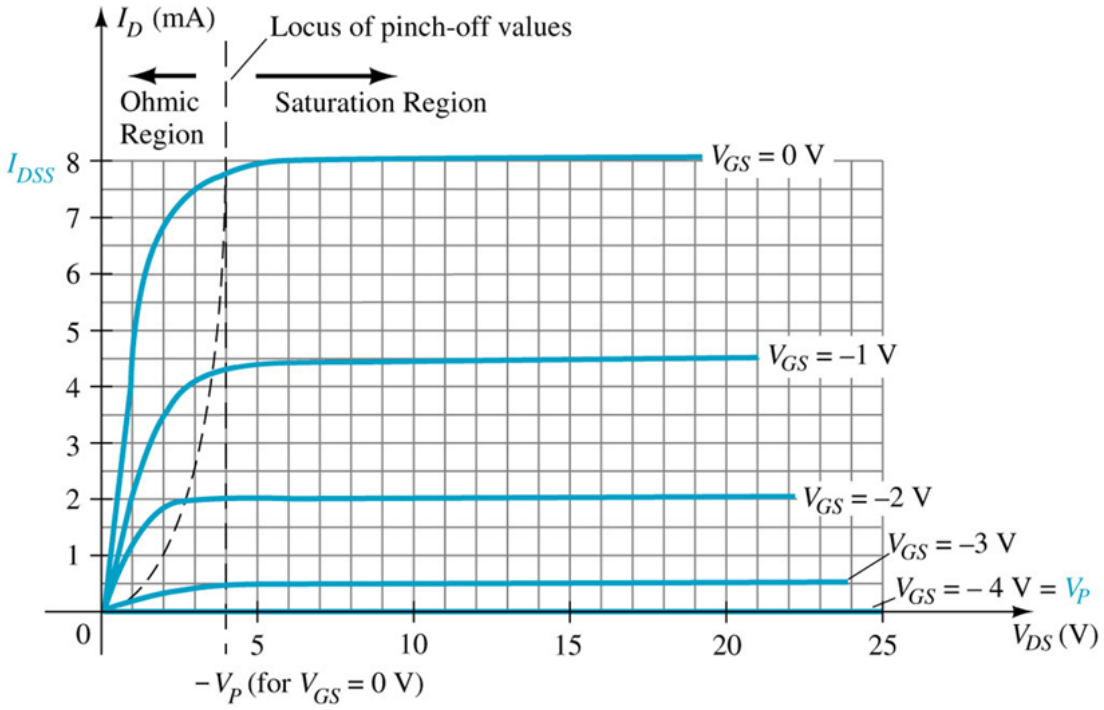



Figure 7.7: Output characteristics of an $n$-Channel JFET with $I_{DSS} = 8\,\text{mA}$ and $V_P = -4\,\text{V}$.

The region to the **right** of the pinch-off point of Figure 7.7 is the region employed in amplifiers and is commonly referred to as the **constant-current**, **saturation**, or linear amplification region.

The region to the **left** of the locus (curve) of pinch-off values of Figure 7.7 is called the **ohmic** or **linear** region.

On most specification sheets the pinch-off voltage is specified as $V_{GS(off)}$ rather than $V_P$.

The saturation current values (constant current values after pinch-off) Figure 7.7 can be expressed in terms of the control voltage $V_{GS}$ as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{7.4.1}$$

This equation is called the **transfer characteristics** equation and will be investigated in detail later in the transfer characteristics section.

#### 7.4.2.3 Voltage-Controlled Resistor (Ohmic Region)

The region to the **left** of the locus (curve) of pinch-off values of Figure 7.7 is called the **ohmic** or **linear** region.

In this region, JFET can be used as a variable resistor, where $V_{GS}$ controls the drain-source resistance ($r_d$)

As $V_{GS}$ becomes more negative, the resistance ($r_d$) increases.

$$r_d = \frac{r_0}{\left(1 - \frac{V_{GS}}{V_P}\right)^2} \tag{7.4.2}$$

where $r_0$ is the resistance with $V_{GS} = 0\,\text{V}$ given in the specification sheets.

### 7.4.3 *p*-channel JFET

*p*-channel JFET acts the same as the *n*-channel JFET, except the polarities and currents are reversed as shown in Figure 7.8 below.

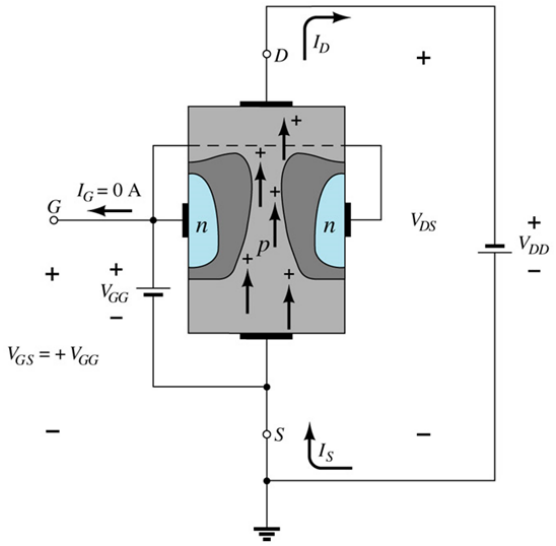



Figure 7.8: *p*-Channel JFET biasing.

#### 7.4.3.1 Characteristics

Output characteristics of a *p*-channel JFET is shown in Figure 7.9 below. Note that Also at high levels of $V_{DS}$ the JFET reaches a breakdown situation where $I_D$ increases uncontrollably if $V_{DS} > V_{DS(\text{max})}$. Although we have not shown before breakdown region also exists in *n*-channel JFETs.

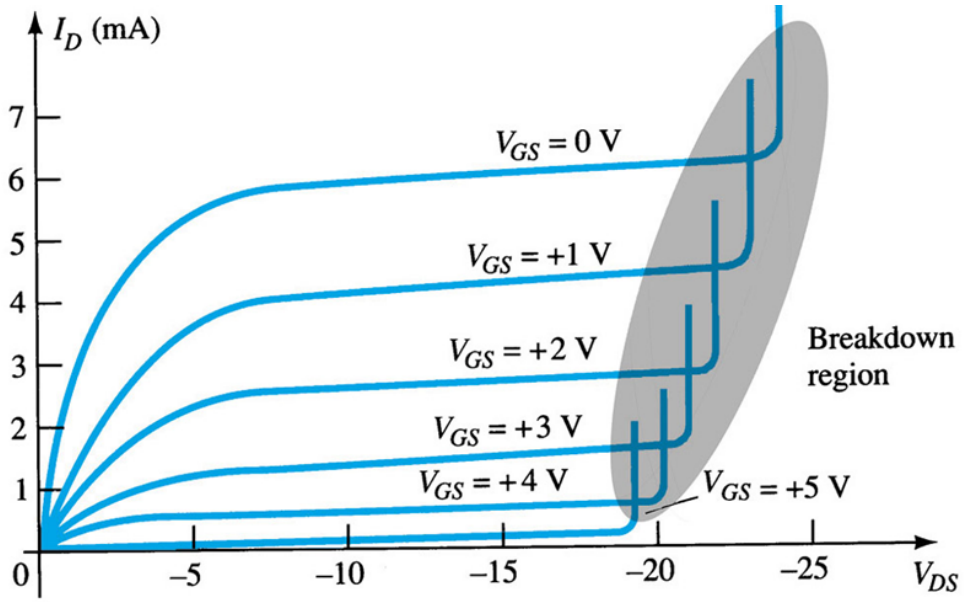



Figure 7.9: Output characteristics of an $p$-Channel JFET with $I_{DSS} = 6\,\text{mA}$ and $V_P = +6\,\text{V}$.

### 7.4.4 Circuit Symbol

The graphic symbols for the $n$-channel and $p$-channel JFETs are provided in Figure 7.10 below.

Note that the **arrow** at the **gate** terminal is pointing **in** for the $n$-channel device in Figure 7.10(a) to represent the direction in which $I_G$ would flow if the $pn$ junction was forward-biased.

For the $p$-channel device in Figure 7.10(b) the **arrow** at the **gate** terminal is pointing **out**.


Figure 7.10: JFET circuit symbols: (a) $n$-channel, (b) $p$-channel.

### 7.4.5 Transfer Characteristics

The saturation current is determined by the control voltage $V_{GS}$ as follows

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2} \tag{7.4.3}$$

This equation is called the **transfer characteristics** (transfer from input to output, i.e., from $V_{GS}$ to $I_D$) and can be plotted on a graph as shown in Figure 7.11 below

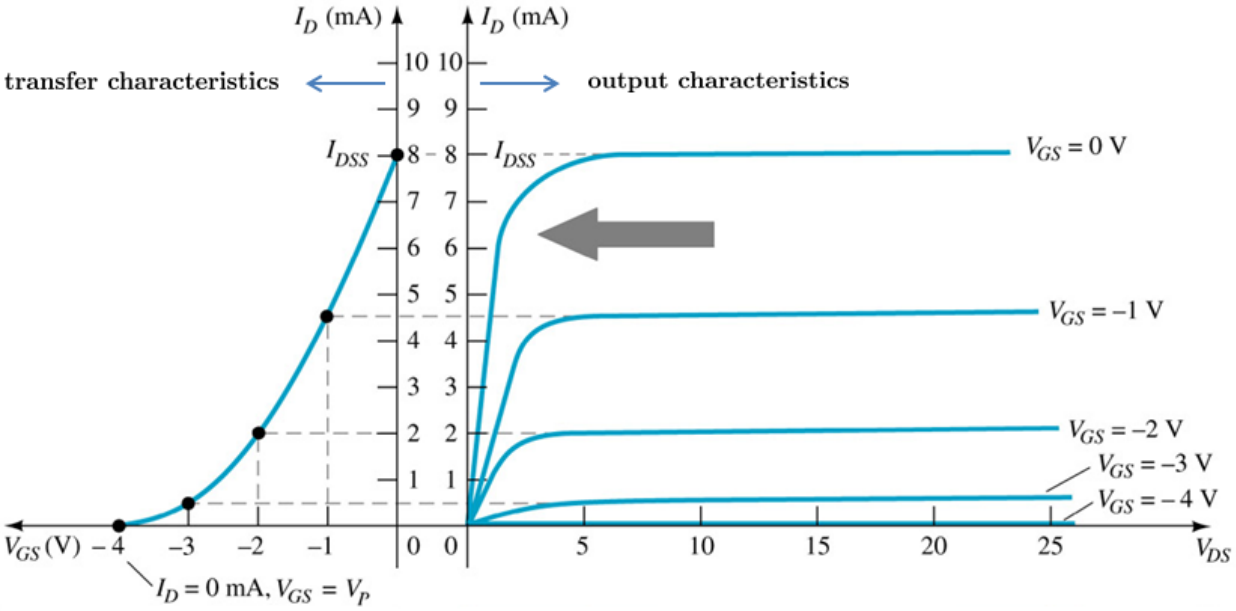



Figure 7.11: Transfer and output characteristics curves together for an $n$-channel JFET.

We can also plot this transfer characteristics as the ratios of $a_D = \frac{I_D}{I_{DSS}}$ and $a_G = \frac{V_{GS}}{V_P}$ without needing the actual values of $I_{DSS}$ and $V_P$ as shown in Figure 7.12 below. The scaled transfer characteristics is obtained as

$$a_D = (1 - a_G)^2 \tag{7.4.4}$$

where $0 \leq a_G \leq 1$ (note that also $0 \leq a_D \leq 1$). For $a_D = 0.5$, we obtain $a_G \cong 0.3$. So, $(0.3, 0.5)$-point can be also used in plot generation. With the values of $I_{DSS}$ and $V_P$, we know that

$$V_{GS} = a_G V_P \tag{7.4.5}$$

$$I_D = a_D I_{DSS} \tag{7.4.6}$$

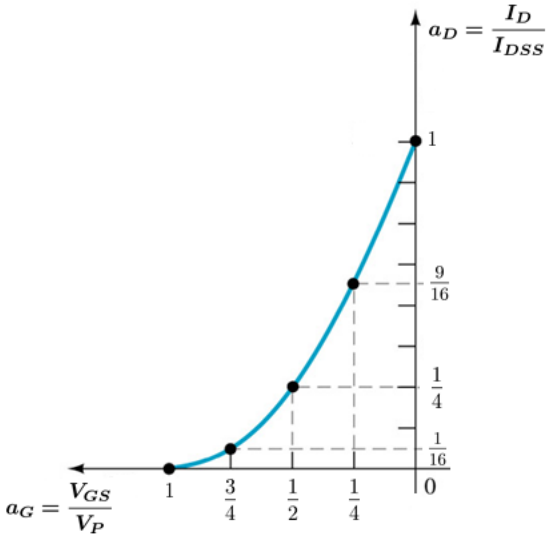



Figure 7.12: Scaled transfer characteristics curve.

## 7.5 Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)

MOSFETs have characteristics similar to JFETs and additional characteristics that make them very useful.

There are two types of MOSFETs:

- Depletion-type MOSFET (DMOSFET)
- Enhancement-type MOSFET (EMOSFET)

The terms *depletion* and *enhancement* define their basic mode of operation.

### 7.5.1 Depletion-Type MOSFET (DMOSFET)

#### 7.5.1.1 Construction

There are two types of DMOSFETs: $n$-channel and $p$-channel. The $n$-channel whose construction is shown in Figure 7.13 below is more widely used.

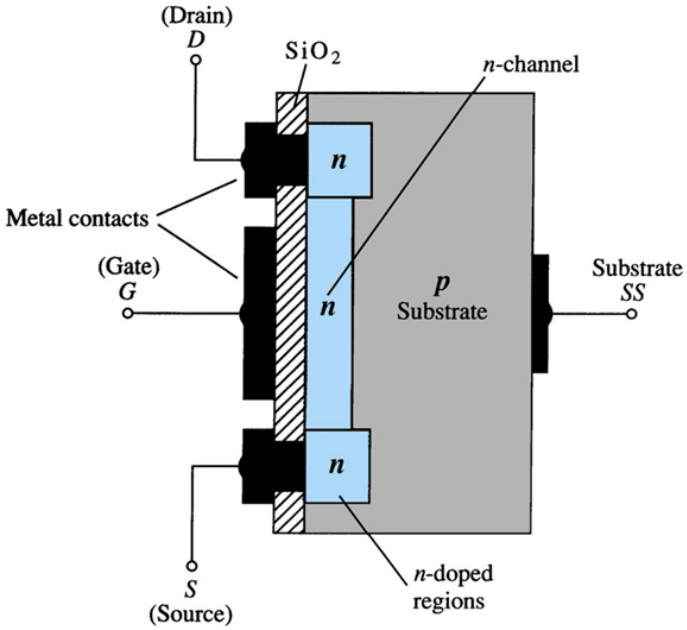



Figure 7.13: $n$-channel depletion-type MOSFET construction.

- A slab of $p$-type material is formed from a silicon base and is referred to as the **substrate**.
- For correct operation, substrate-channel $pn$ junction must be **reverse-biased**.

  In this course, we will only consider the cases where the **substrate** ($SS$) terminal is **connected** (shorted) to the **source** ($S$) terminal.
- Drain ($D$) and Source ($S$) are connected to $n$-channel via metal contacts.
- **Gate** ($G$) is connected to a metal contact surface but remains **insulated** from the $n$-channel by a very thin silicon dioxide ($SiO_2$) layer.

#### 7.5.1.2 Operating Characteristics

In a DMOSFET, the **channel** is **already present** under no-bias conditions or $V_{GS} = 0\,\text{V}$.

Here, $V_{GS}$ controls the **initial channel width** (and value of the saturation current).

When $V_{GS}$ is fixed, for a positive value of $V_{DS}$ the width of the channel gets narrower towards the top of the channel as the voltage across the channel increases towards the top as shown in Figure 7.14 below.

Eventually, when we increase the value of $V_{DS}$, the channel will be pinched-off at some value of $V_{DS}$ and the device will go into the saturation mode.

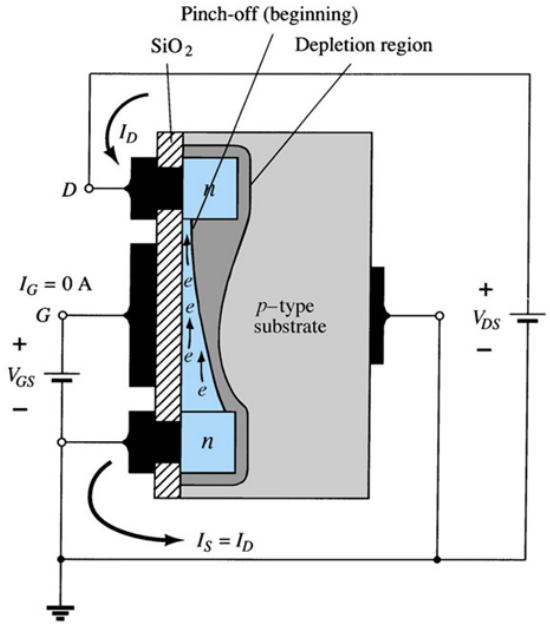



Figure 7.14: Change in channel width (and depletion region) for a fixed value of $V_{GS}$ ($V_{GS}$ determines the initial channel width) with $V_{DS} > 0$.

- $V_{GS}$ controls the **initial channel width** by attracting or repelling electrons.

  A **negative** value of $V_{GS}$ repels electrons (and attracts holes), so the channel gets narrower. This mode is exactly like a JFET, and it is called the **depletion mode**.

  A **positive** value of $V_{GS}$ attracts electrons (and repels holes), so the channel gets wider as shown in Figure 7.15 below. Thus unlike JFETs, the channel width can be increased in DMOSFETs. This mode is called the **enhancement mode**.

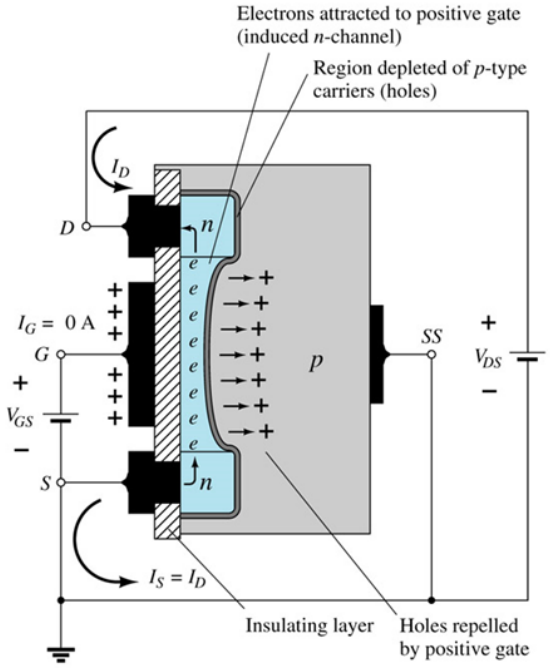



Figure 7.15: Increase (or enhancement) in initial channel width when $V_{GS} > 0$.

#### 7.5.1.3 Transfer Characteristics

Similar to JFET, DMOSFET transfer characteristics equation is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{7.5.7}$$

where $V_{GS}$ is allowed to be opposite polarity of $V_P$ (i.e., $V_{GS} > 0$ allowed for $n$-channel DMOSFETs) as shown in Figure 7.16

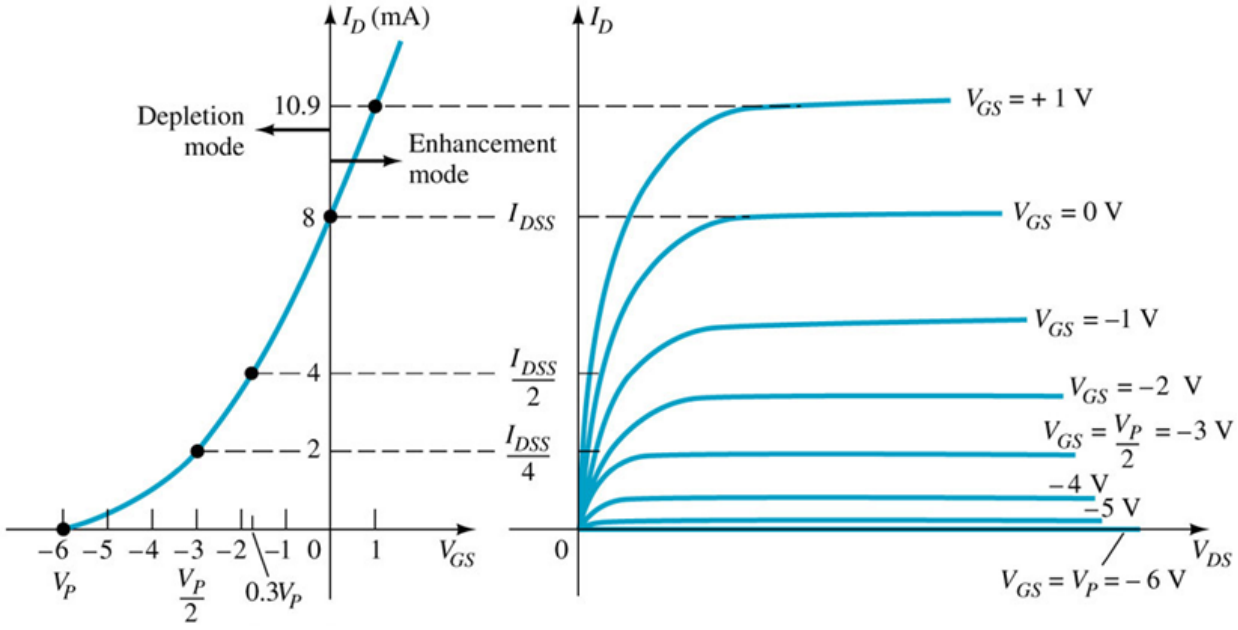



Figure 7.16: Transfer and output characteristics curves together for an $n$-channel DMOSFET.

#### 7.5.1.4 *p*-channel DMOSFET

The *p*-channel DMOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed. Its construction (a), transfer characteristics (b) and output characteristics (c) are shown in Figure 7.17 below.

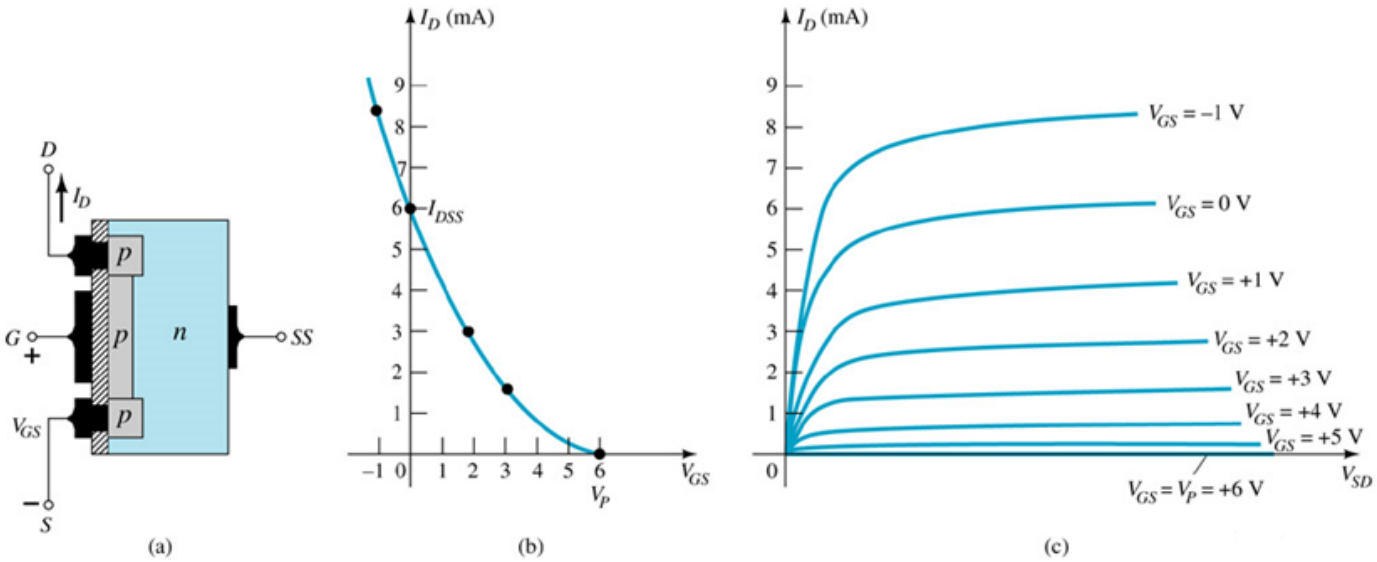


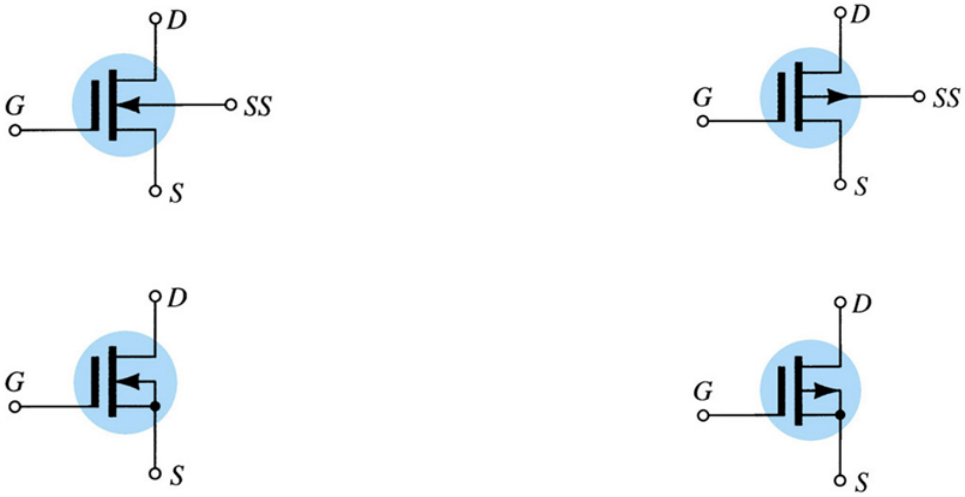

Figure 7.17: *p*-channel DMOSFET with $I_{DSS} = 6\,\text{mA}$ and $V_P = +6\,\text{V}$: (a) construction, (b) transfer characteristics, (c) output characteristics.

### 7.5.2 Circuit Symbol

The graphic symbols for the *n*-channel and *p*-channel DMOSFETs are provided in Figure 7.18 below. Notice that there is a gap between the gate and the channel representing the insulation ($SiO_2$) layer between the gate and the channel.

Note that the **arrow** at the **substrate** ($SS$) terminal is pointing **in** for the *n*-channel device in Figure 7.18(a) to represent the direction of substrate-channel *pn* junction.

For the *p*-channel device in Figure 7.18(b) the **arrow** at the **substrate** terminal is pointing **out**.




(a) (b)

Figure 7.18: DMOSFET circuit symbols: (a) $n$-channel, (b) $p$-channel.

### 7.5.3 Enhancement-Type MOSFET (EMOSFET)

#### 7.5.3.1 Construction

There are two types of EMOSFETs: $n$-channel and $p$-channel. The $n$-channel whose construction is shown in Figure 7.19 below is more widely used.

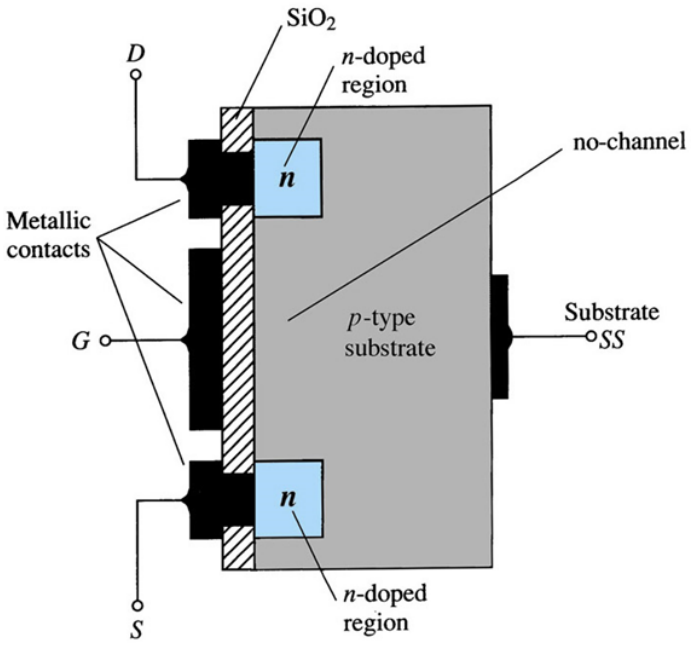



Figure 7.19: $n$-channel enhancement-type MOSFET construction.

- In an EMOSFET, **no channel** is present under no-bias conditions. We need to provide a positive gate-to-source voltage **greater** than a **threshold voltage** to initially form a channel between drain and source terminals, i.e., $V_{GS} \geq V_{GS(Th)}$.
- Thus, EMOSFET always works in the **enhancement** mode.

- Once $V_{GS}$ is fixed and a channel is formed, it operates like a normal FET.

#### 7.5.3.2 Transfer Characteristics

EMOSFET transfer characteristics equation plotted in shown in Figure 7.20 below is given by

$$I_D = k\left(V_{GS} - V_{GS(Th)}\right)^2 \tag{7.5.8}$$

where $k$ and $V_{GS(Th)}$ are device constants given in the specifications sheets.

If $k$ is not given, it can also be determined from a particular point $(V_{GS_0}, I_{D_0})$ on the transfer characteristics curve of the device as follows

$$k = \frac{I_{D_0}}{\left(V_{GS_0} - V_{GS(Th)}\right)^2} \tag{7.5.9}$$

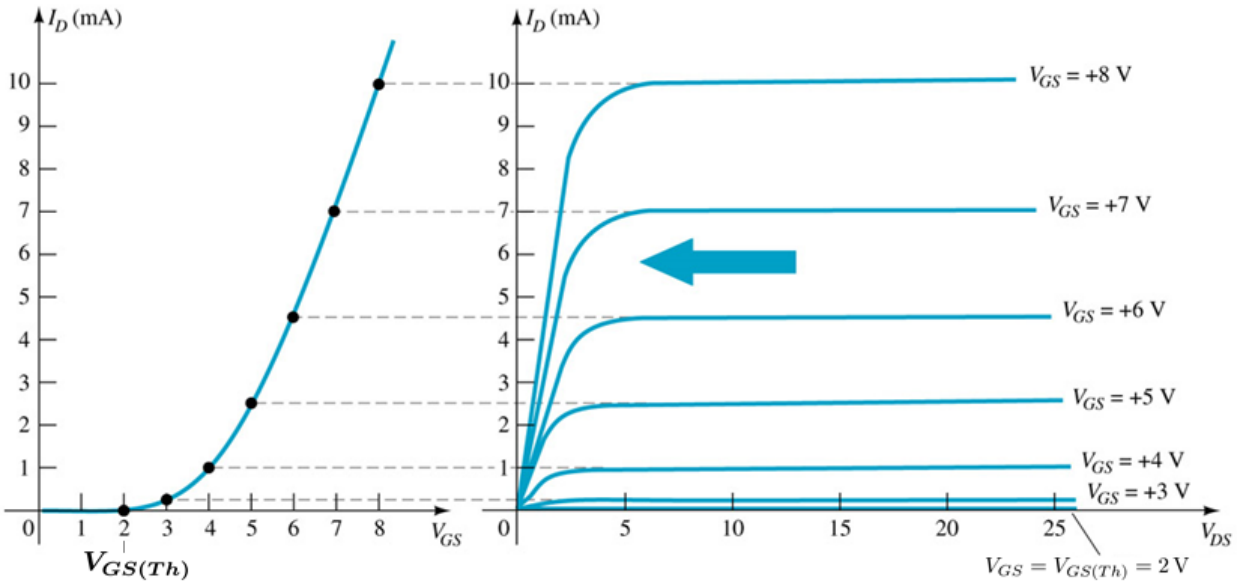



Figure 7.20: Transfer and output characteristics curves together for an $n$-channel EMOSFET.

Drain-to-source pinch-off (saturation) voltage $V_{DS(\text{sat})}$ is also given by

$$V_{DS(\text{sat})} = V_{GS} - V_{GS(Th)} \tag{7.5.10}$$

- EMOSFET transfer characteristics equation below can also be **used** for **DMOSFETS**

$$I_D = k\left(V_{GS} - V_{GS(Th)}\right)^2$$

where

$$V_{GS(Th)} = V_P \tag{7.5.11}$$

$$k = \frac{I_{DSS}}{V_P^2} \tag{7.5.12}$$

**Homework 7.1:** Show that results (7.5.11) and (7.5.12) above are correct.

#### 7.5.3.3 *p*-channel EMOSFET

The *p*-channel DMOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed. Its construction (a), transfer characteristics (b) and output characteristics (c) are shown in Figure 7.21 below.

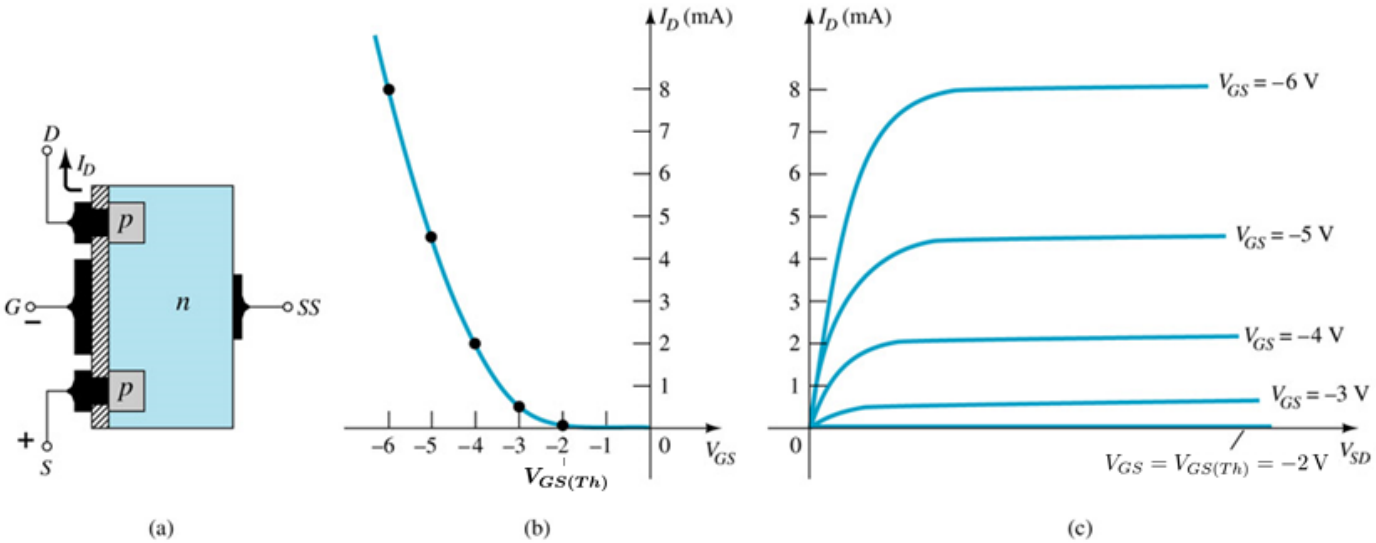


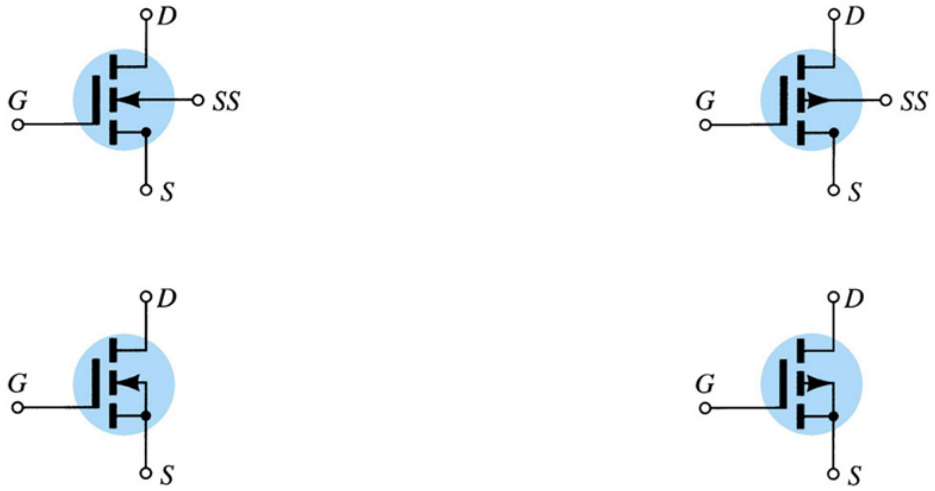

Figure 7.21: *p*-channel EMOSFET with $V_{GS(Th)} = 2\,\text{V}$ and $k = 0.5\,\text{mA/V}^2$: (a) construction, (b) transfer characteristics, (c) output characteristics.

### 7.5.4 Circuit Symbol

The graphic symbols for the *n*-channel and *p*-channel EMOSFETs are provided in Figure 7.22 below. Notice that channel is represented as **dashed line** to reflect the fact that a channel does not exist under no-bias conditions.

Note that the **arrow** at the **substrate** ($SS$) terminal is pointing **in** for the *n*-channel device in Figure 7.22(a) to represent the direction of substrate-channel *pn* junction.

For the *p*-channel device in Figure 7.22(b) the **arrow** at the **substrate** terminal is pointing **out**.




(a) (b)

Figure 7.22: EMOSFET circuit symbols: (a) $n$-channel, (b) $p$-channel.

### 7.5.5 MOSFET Handling

MOSFETs are very static sensitive. Because of the very thin $SiO_2$ layer between the external terminals and the layers of the device, any small electrical discharge can establish an unwanted conduction.

**Protection:**

- Always transport in a static sensitive bag
- Always wear a static strap when handling MOSFETs
- Apply voltage limiting devices between the Gate and Source, such as back-to-back Zeners to limit any transient voltage.

## 7.6 Summary

The transfer curves and some important characteristics of the $n$-channel FETs are displayed in Figure 7.23 below. A clear understanding of all the curves and parameters of the table will provide a sufficient background for the DC and AC analyses.

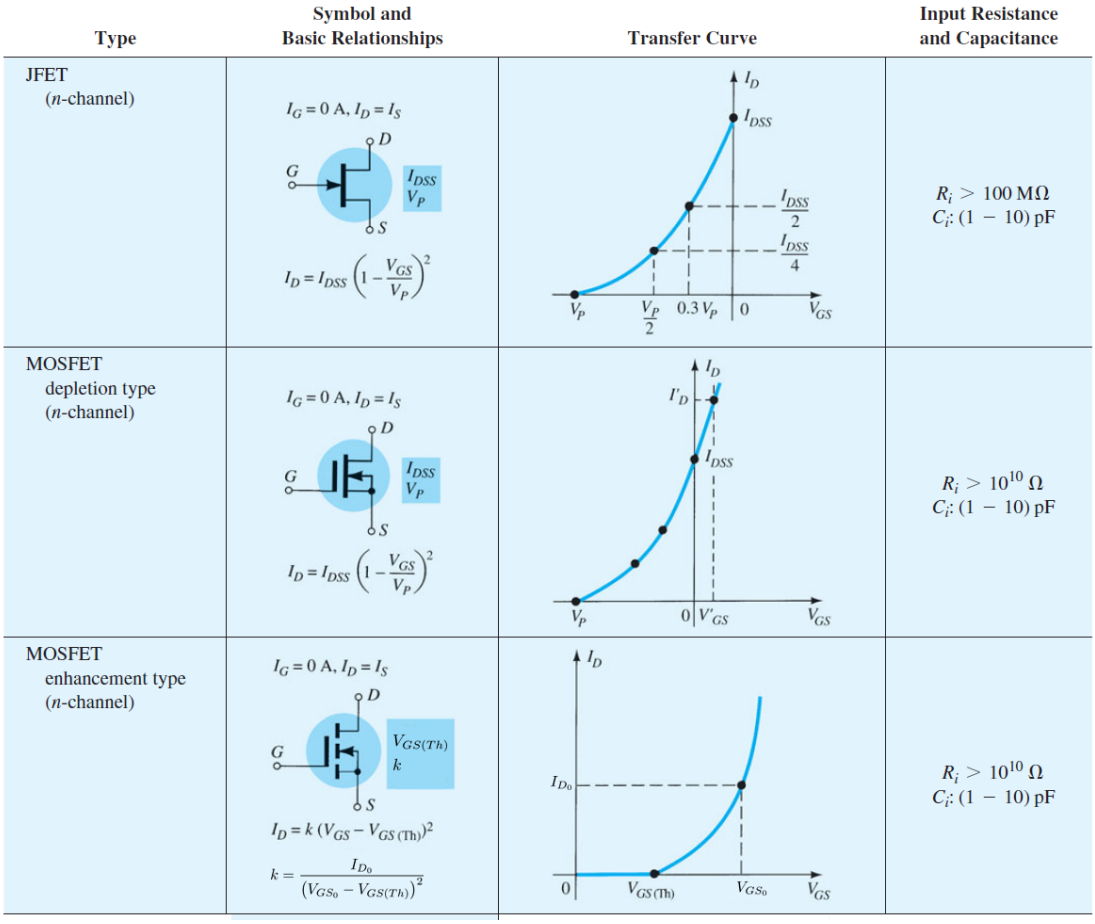



Figure 7.23: $n$-channel FET summary.

We can summarize the $n$-channel FET model with its state and circuit behaviour with the table below.

| $n$-channel FET Model | | |
|---|---|---|
| **State** | **Circuit Behaviour** | **Test Condition** |
| CUTOFF | $I_D = 0$,<br>$I_S = 0$, $I_G = 0$ | $V_{GS} < V_{GS(Th)}$ |
| SATURATION | $I_D = k\left(V_{GS} - V_{GS(Th)}\right)^2$,<br>$I_S = I_D$, $I_G = 0$ | $V_{GS} \geq V_{GS(Th)}$,<br>$V_{DS} \geq V_{DS(\text{sat})}$ |
| OHMIC<br>(LINEAR) | $I_D =$ not covered in this course,<br>$I_S = I_D$, $I_G = 0$ | $V_{GS} \geq V_{GS(Th)}$,<br>$V_{DS} < V_{DS(\text{sat})}$, $I_D < I_{D(\text{sat})}$ |

- **NOTE 1**: For JFET and DMOSFETs, take $V_{GS(Th)} = V_P$ and $k = \dfrac{I_{DSS}}{V_P^2}$
- **NOTE 2**: For JFETs, make sure $V_P \leq V_{GS} \leq 0$.

- **NOTE 3**: $V_{Th}$, $V_T$ and $V_{TN}$ (or $V_{TP}$) notations are also used in place of $V_{GS(Th)}$.

We can show the circuit behaviour for the CUTOFF and SATURATION modes of the $n$-channel FETs in Figure 7.24 below.

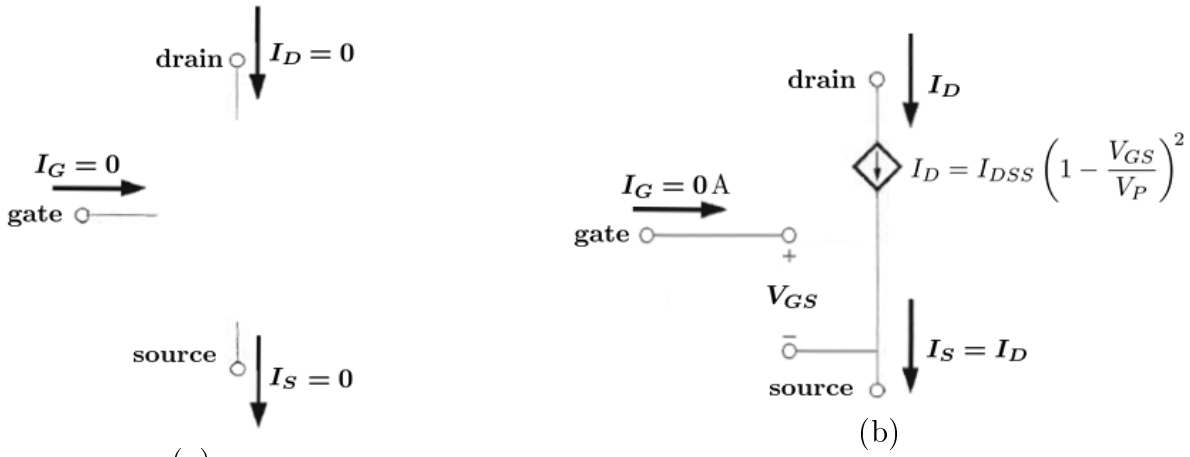



Figure 7.24: Circuit behaviour of the $n$-channel FET model: (a) Cutoff state, (b) Saturation state

- For a $p$-channel FET transistor, the **polarities** and **directions** are simply **reversed**.

  For example, the a $p$-channel FET will be ON (i.e., in SATURATION mode) when $V_{SG} \geq V_{SG(Th)}$ (i.e., when $V_{GS} \leq V_{GS(Th)}$).

# Chapter 8

# DC Biasing of FETs

## 8.1 DC Biasing

## 8.2 FET DC Analysis

1. Draw the DC equivalent circuit (signal frequency is zero, i.e., $f = 0$)
   a) Capacitors are open circuit, i.e., $X_C \to \infty$.
   b) Kill the AC power sources (short-circuit AC voltage sources and open-circuit AC current sources).
2. Write KVL for the $GS$-loop (i.e., $GS$-loop load line (or transfer load line) equation)
   a) Draw the transfer characteristics curve using the appropriate transfer characteristics equation.
   b) Draw the $GS$-loop load line over the transfer characteristics curve
   c) The intersection gives us $I_{DQ}$ and $V_{GSQ}$.

   NOTE: You can also solve two equations simultaneously and obtain the result analytically by solving the resultant quadratic equation. However, graphical way is less error-prone if the graph has a fine resolution.
3. Write KVL for the $DS$-loop (i.e., $DS$-loop load line (or output load line) load line equation)
   a) Calculate $V_{DSQ}$ using $I_{DQ}$ value from Step 2c.

## 8.3 DC Biasing Circuits

Most common four common-source biasing circuits are given below

**JFET Biasing Circuits**

- Fixed-Bias
- Self-Bias
- Voltage-Divider

**DMOSFET Biasing Circuits**

- Self-Bias
- Voltage-Divider

**EMOSFET Biasing Circuits**

- Voltage-Feedback
- Voltage-Divider

### 8.3.1 Fixed-Bias Configuration

A fixed-bias JFET circuit is given in Figure 8.1 below

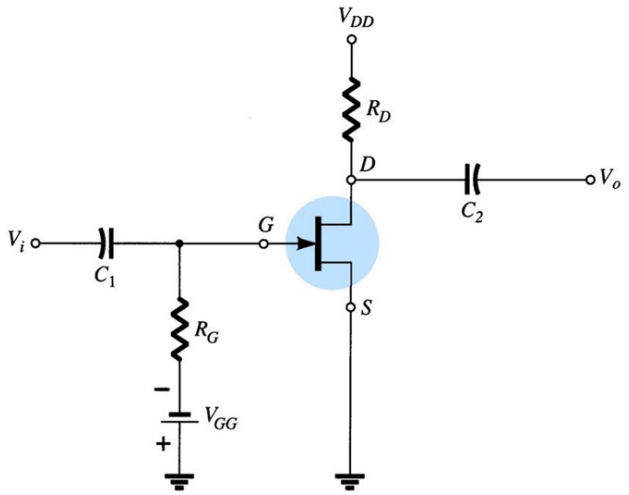



Figure 8.1: Fixed-bias JFET circuit.

Let us start DC analysis by drawing the DC equivalent circuit as shown in Figure 8.2 below

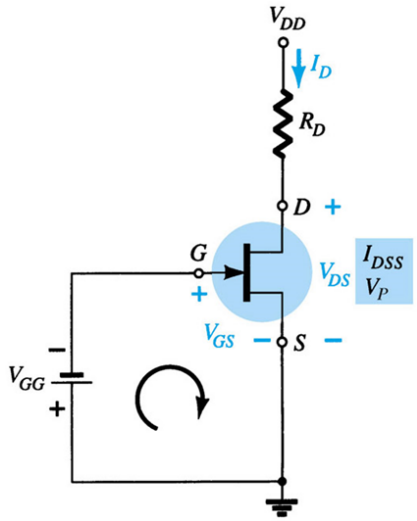



Figure 8.2: DC equivalent circuit (with $I_G = 0$) of the fixed-bias configuration in Figure 8.1.

Note that $R_G$ is ignored as $I_G = 0$.

#### 8.3.1.1 Gate-Source Loop

We can write KVL equation on the $GS$-loop

$$V_{GS} = -V_{GG}. \tag{8.3.1}$$

Then, we obtain $V_{GSQ}$ and $I_{DSQ}$ by solving the following two equations simultaneously

$$V_{GS} = -V_{GG} \qquad \ldots \text{transfer load-line} \tag{8.3.2}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \ldots \text{transfer characteristics} \tag{8.3.3}$$

The solution is trivial in this case and we obtain the result as

$$V_{GSQ} = -V_{GG} \tag{8.3.4}$$

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2 \tag{8.3.5}$$

We can also obtain the result graphically by plotting equations (8.3.2) and (8.3.3) on the same graph as shown in Figure 8.3 below.

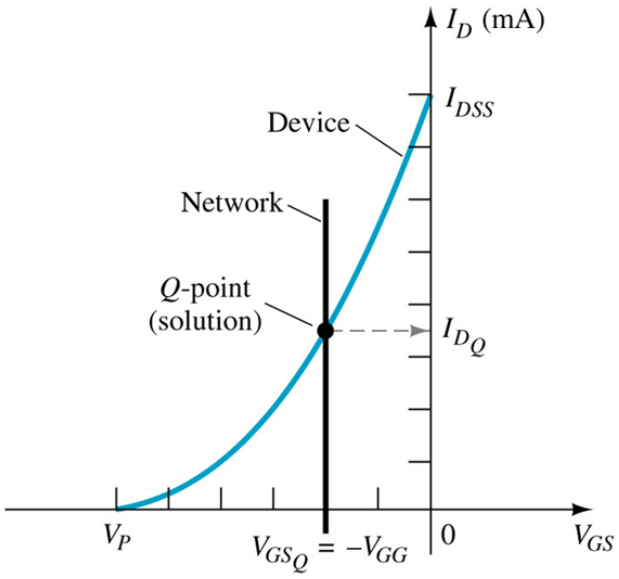



Figure 8.3: Graphical solution (for transfer load-line and transfer characteristics equations) for the fixed-bias configuration in Figure 8.1.

#### 8.3.1.2 Drain-Source Loop

Let us write down the KVL equation on the $DS$-loop

$$V_{DD} - I_D R_D - V_{DS} = 0 \tag{8.3.6}$$

$$V_{DS} = V_{DD} - I_D R_D \quad \ldots \text{DC load-line equation} \tag{8.3.7}$$

As we already obtained $I_{DQ}$ in Figure 8.3 we find $V_{DSQ}$ as

$$\boxed{V_{DSQ} = V_{DD} - I_{DQ} R_D} \tag{8.3.8}$$

Thus, we obtained the $Q$-point $(I_{DQ}, V_{DSQ})$, i.e., the operating point.

### 8.3.2 Self-Bias Configuration

A fixed-bias JFET circuit is given in Figure 8.4 below

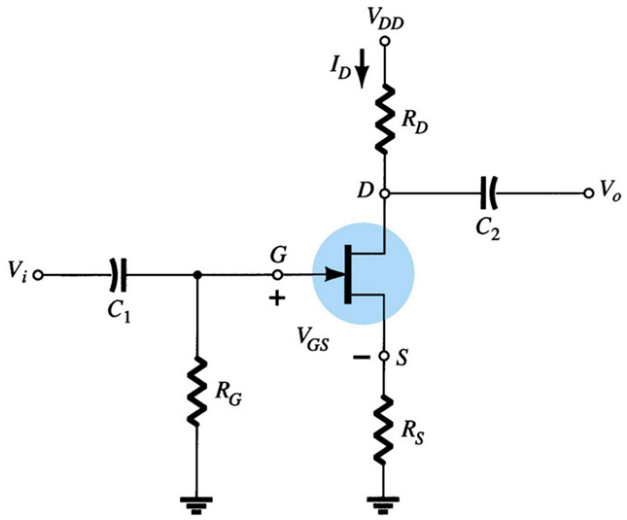



Figure 8.4: Self-bias JFET circuit.

Let us start DC analysis by drawing the DC equivalent circuit as shown in Figure 8.5 below

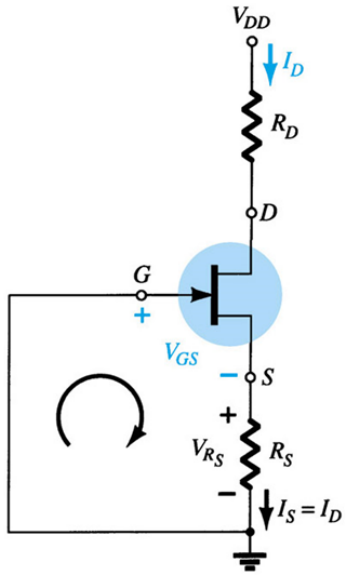



Figure 8.5: DC equivalent circuit (with $I_G = 0$) of the self-bias configuration in Figure 8.4.

Note that $R_G$ is ignored as $I_G = 0$.

#### 8.3.2.1 Gate-Source Loop

We can write KVL equation on the $GS$-loop

$$-V_{GS} - I_S R_S = 0 \tag{8.3.9}$$

$$V_{GS} = -I_D R_S \quad \ldots \text{as } I_S = I_D. \tag{8.3.10}$$

Then, we obtain $V_{GSQ}$ and $I_{DSQ}$ by solving the following two equations simultaneously

$$V_{GS} = -I_D R_S \qquad \ldots \text{transfer load-line} \qquad (8.3.11)$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \ldots \text{transfer characteristics} \qquad (8.3.12)$$

It is better to obtain the result graphically by plotting equations (8.3.11) and (8.3.12) on the same graph as shown in Figure 8.6 below.

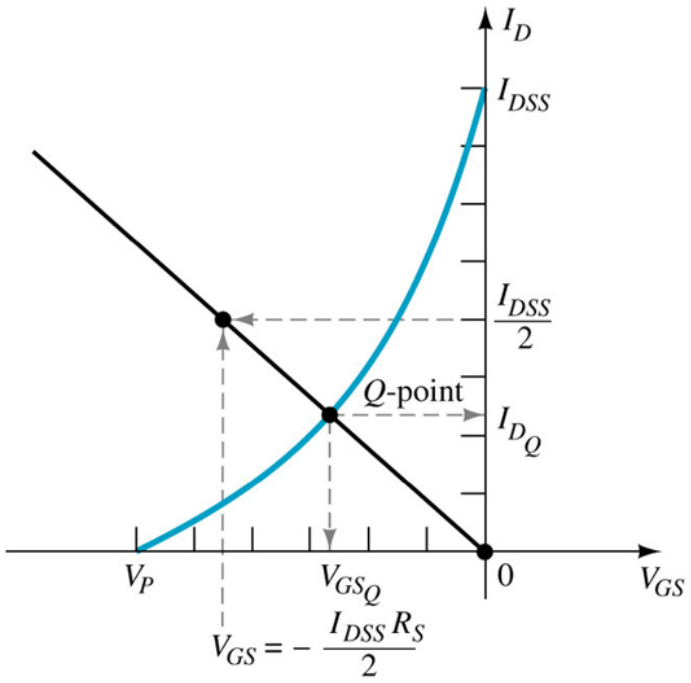



Figure 8.6: Graphical solution (for transfer load-line and transfer characteristics equations) for the self-bias configuration in Figure 8.4.

The graphically obtained current value $I_{DQ}$ may be refined using equations (8.3.11) and (8.3.12) in an iteration loop as follows

1. Insert graphically obtained $I_D$ into (8.3.11) and obtain a $V_{GS}$ value
2. Insert $V_{GS}$ obtained in Step 1 into (8.3.12) and obtain a new $I_D$ value to be used in Step 1.
3. Repeat Step 1 and Step 2 until $\Delta I_D$, the difference between the old $I_D$ used in Step 1 and new $I_D$ obtained in Step 2, is small enough.

#### 8.3.2.2 Drain-Source Loop

Let us write down the KVL equation on the $DS$-loop

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0 \qquad (8.3.13)$$

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0 \qquad \ldots \text{as } I_S = I_D \qquad (8.3.14)$$

$$V_{DD} - I_D (R_D + R_S) - V_{DS} = 0 \qquad \ldots \text{DC load-line equation} \qquad (8.3.15)$$

As we already obtained $I_{DQ}$ in Figure 8.6 we find $V_{DSQ}$ as

$$\boxed{V_{DSQ} = V_{DD} - I_{DQ}\,(R_D + R_S)} \tag{8.3.16}$$

Thus, we obtained the $Q$-point $(I_{DQ}, V_{DSQ})$, i.e., the operating point.

**Example 8.1:** For the figure below, calculate all DC currents and voltages.

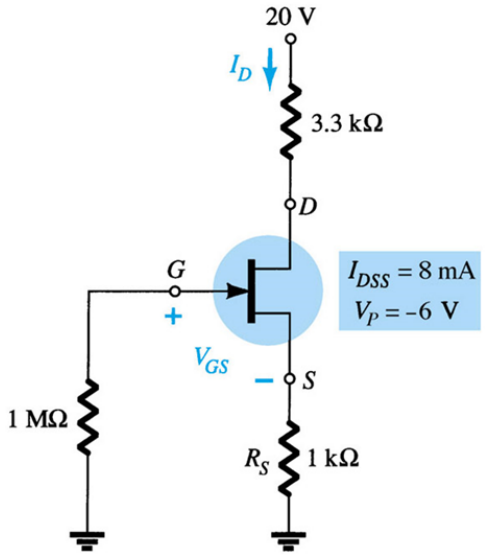



Figure 8.7: Self-bias JFET circuit for Example 8.1.

**Solution:** Let us express $V_{GS}$ using the KVL equation of $GS$-loop and $I_D$ from the transfer characteristics equation

$$V_{GS} = -I_D R_S = -1k\, I_D$$
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = (8m)\left(1 + \frac{V_{GS}}{6}\right)^2$$

where $-6 \leq V_{GS} \leq 0$.

We obtain $I_{DQ}$ and $V_{GSQ}$ by drawing these two equations on the same graph as shown in Figure 8.8 below

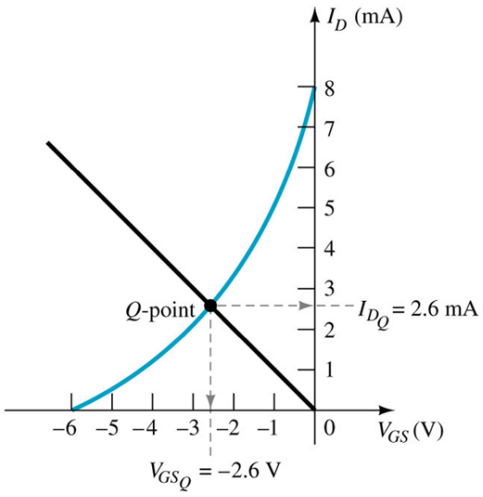



Figure 8.8: Obtaining $I_{DQ}$ graphically for the circuit in Figure 8.7.

Finally, we obtain $V_{DSQ}$ from the $DS$-loop as

$$V_{DSQ} = V_{DD} - I_{DQ}\,(R_D + R_S) = 20 - (2.6m)\,(3.3k + 1k) = 8.82\,\text{V}.$$

### 8.3.3 Voltage-Divider Bias Configuration

A voltage-divider bias JFET circuit is given in Figure 8.9 below

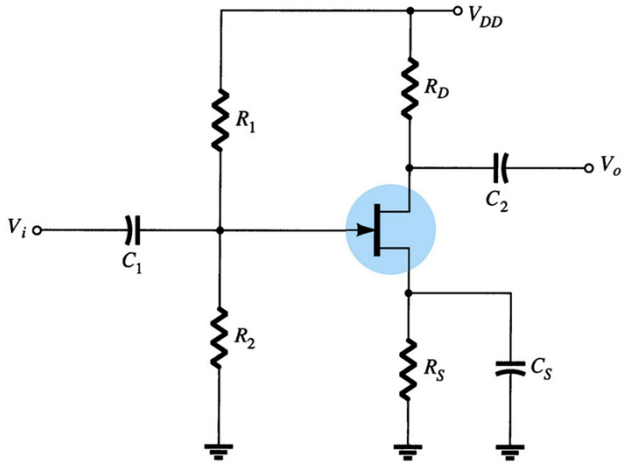



Figure 8.9: Voltage-divider bias JFET circuit.

Let us start DC analysis by drawing the DC equivalent circuit as shown in Figure 8.10 below

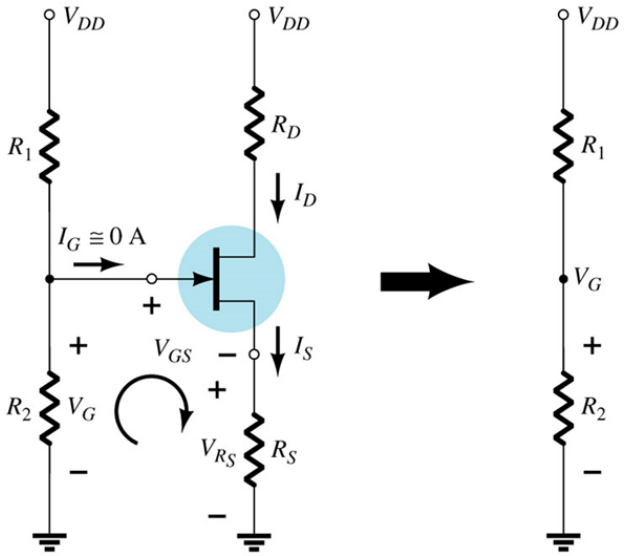



Figure 8.10: DC equivalent circuit of the voltage-divider configuration in Figure 8.9.

#### 8.3.3.1 Gate-Source Loop

We can write KVL equation on the $GS$-loop

$$V_G - V_{GS} - I_S R_S = 0 \qquad \ldots \text{where } V_G = \frac{R_2}{R_1 + R_2} V_{DD} \quad (8.3.17)$$

$$V_{GS} = V_G - I_D R_S \qquad \ldots \text{as } I_S = I_D. \quad (8.3.18)$$

Then, we obtain $V_{GSQ}$ and $I_{DSQ}$ by solving the following two equations simultaneously

$$V_{GS} = V_G - I_D R_S \qquad \ldots \text{transfer load-line} \quad (8.3.19)$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \ldots \text{transfer characteristics} \quad (8.3.20)$$

It is better to obtain the result graphically by plotting equations (8.3.19) and (8.3.20) on the same graph as shown in Figure 8.11 below.

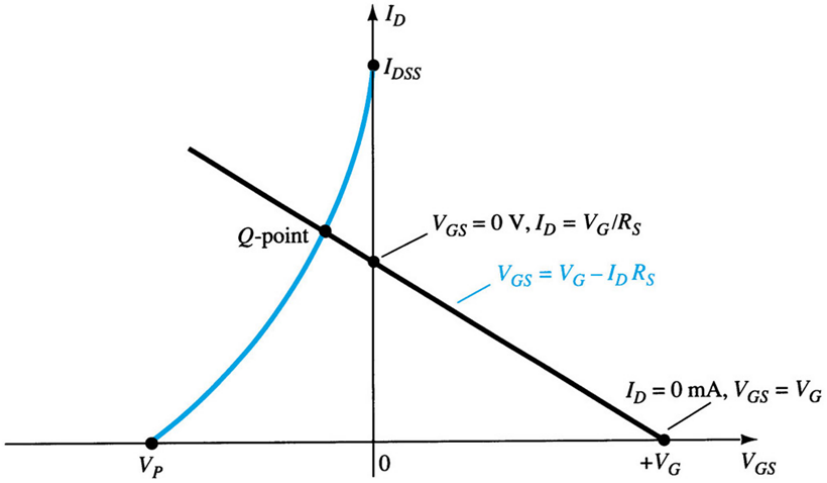



Figure 8.11: Graphical solution (for transfer load-line and transfer characteristics equations) for the voltage-divider configuration in Figure 8.9.

The graphically obtained current value $I_{DQ}$ may be refined using equations (8.3.19) and (8.3.20) in an iteration loop as follows

1. Insert graphically obtained $I_D$ into (8.3.19) and obtain a $V_{GS}$ value
2. Insert $V_{GS}$ obtained in Step 1 into (8.3.20) and obtain a new $I_D$ value to be used in Step 1.
3. Repeat Step 1 and Step 2 until $\Delta I_D$, the difference between the old $I_D$ used in Step 1 and new $I_D$ obtained in Step 2, is small enough.

#### 8.3.3.2 Drain-Source Loop

Let us write down the KVL equation on the $DS$-loop

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0 \tag{8.3.21}$$
$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0 \qquad \ldots \text{as } I_S = I_D \tag{8.3.22}$$
$$V_{DD} - I_D (R_D + R_S) - V_{DS} = 0 \qquad \ldots \text{DC load-line equation} \tag{8.3.23}$$

As we already obtained $I_{DQ}$ in Figure 8.11 we find $V_{DSQ}$ as

$$\boxed{V_{DSQ} = V_{DD} - I_{DQ} (R_D + R_S)} \tag{8.3.24}$$

Thus, we obtained the $Q$-point $(I_{DQ}, V_{DSQ})$, i.e., the operating point.

**Example 8.2:** For the figure below, calculate all DC currents and voltages.

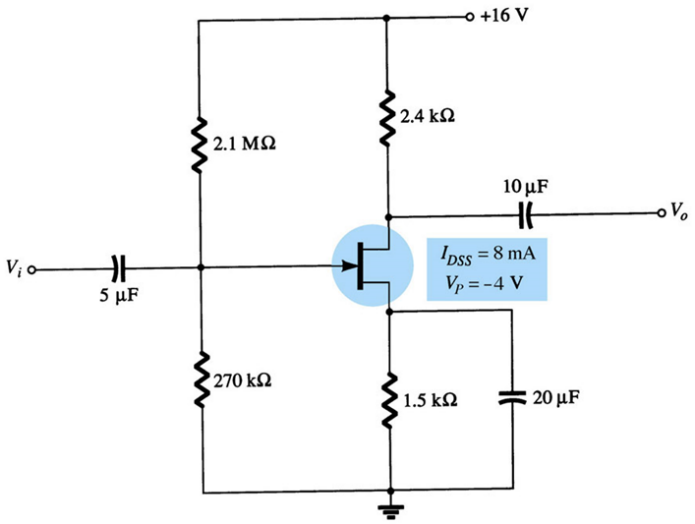



Figure 8.12: Voltage-divider bias JFET circuit for Example 8.2.

**Solution:** Let us find $V_G$, and express $V_{GS}$ using the KVL equation of $GS$-loop and $I_D$ from the transfer characteristics equation

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{0.27M}{2.1M + 0.27M} 16 = 1.82\,\text{V}.$$
$$V_{GS} = V_G - I_D R_S = 1.82 - 1.5k\, I_D$$
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 = (8m) \left(1 + \frac{V_{GS}}{4}\right)^2$$

where $-4 \leq V_{GS} \leq 0$.

We obtain $I_{DQ}$ and $V_{GSQ}$ by drawing these two equations on the same graph as shown in Figure 8.13 below

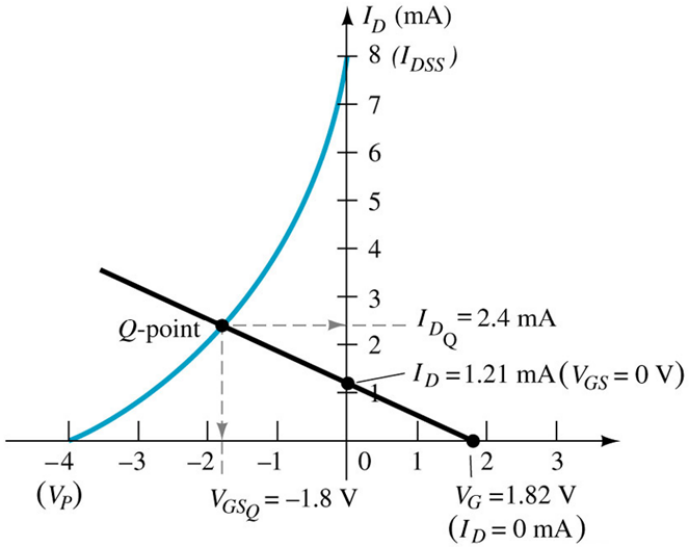



Figure 8.13: Obtaining $I_{DQ}$ graphically for the circuit in Figure 8.12.

Finally, we obtain $V_{DSQ}$ from the $DS$-loop as

$$V_{DSQ} = V_{DD} - I_{DQ}\,(R_D + R_S) = 16 - (2.4m)\,(2.4k + 1.5k) = 6.64\,\text{V}.$$

**Example 8.3:** For the figure below, calculate $Q$-point. Repeat for $R_S = 150\,\Omega$.

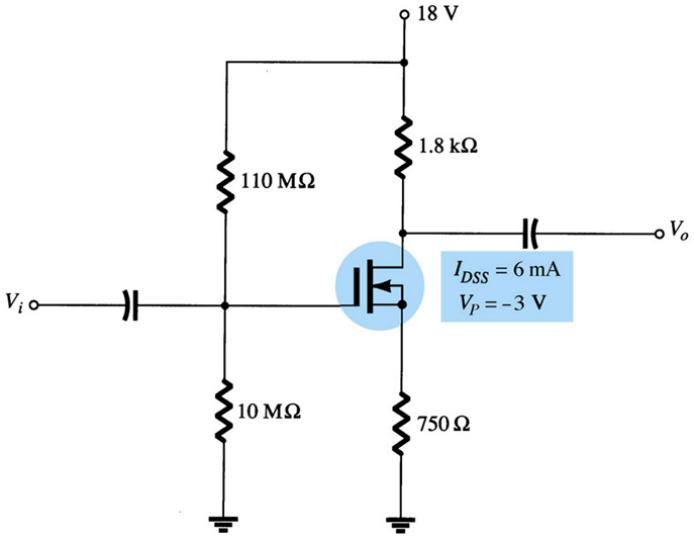



Figure 8.14: Voltage-divider bias DMOSFET circuit for Example 8.3.

**Solution:** Let us find $V_G$, and express $V_{GS}$ using the KVL equation of $GS$-loop and $I_D$ from

the transfer characteristics equation

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{10M}{110M + 10M} 18 = 1.5\,\text{V}.$$
$$V_{GS} = V_G - I_D R_S = 1.5 - 0.75k\, I_D$$
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 = (6m) \left(1 + \frac{V_{GS}}{3}\right)^2$$

where $V_{GS} \geq -3\,\text{V}$.

We obtain $I_{DQ}$ and $V_{GSQ}$ by drawing these two equations on the same graph as shown in Figure 8.15 below

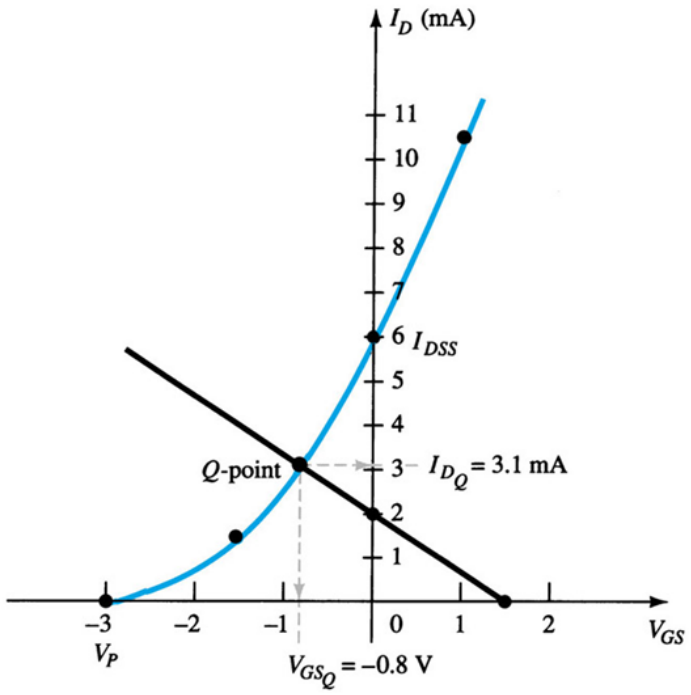



Figure 8.15: Obtaining $I_{DQ}$ graphically for the circuit in Figure 8.14 with $R_S = 750\,\Omega$.

Finally, we obtain $V_{DSQ}$ from the $DS$-loop as

$$V_{DSQ} = V_{DD} - I_{DQ}\,(R_D + R_S) = 18 - (3.1m)\,(1.8k + 0.75k) = 10.1\,\text{V}.$$

Let us repeat the calculations for $R_S = 150\,\Omega$. Transfer load-line equation ($GS$-loop equation) changes as below

$$V_{GS} = V_G - I_D R_S = 1.5 - 0.15k\, I_D$$

We reobtain $I_{DQ}$ and $V_{GSQ}$ by redrawing the transfer load-line and transfer characteristics equations on the same graph as shown in Figure 8.16 below

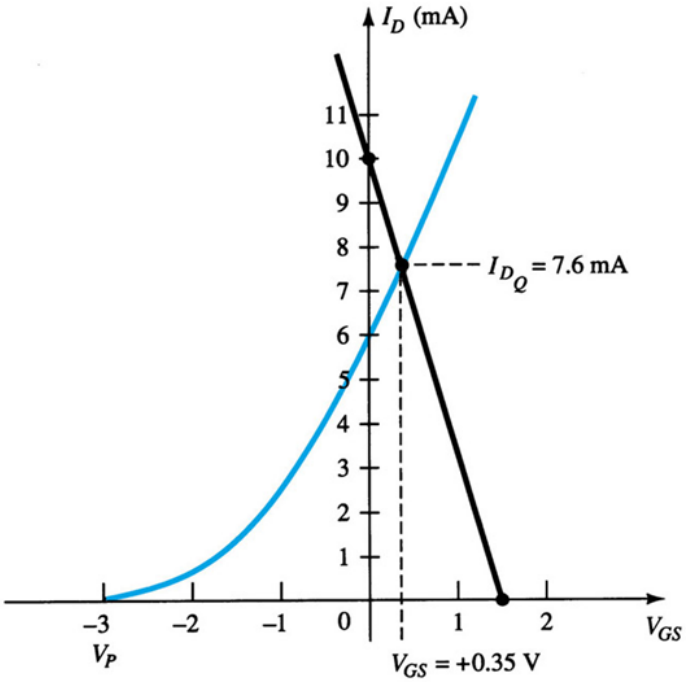



Figure 8.16: Obtaining $I_{DQ}$ graphically for the circuit in Figure 8.14 with $R_S = 150\,\Omega$.

Finally, $V_{DSQ}$ is recalculated from the $DS$-loop as

$$V_{DSQ} = V_{DD} - I_{DQ}\,(R_D + R_S) = 18 - (7.6m)\,(1.8k + 0.15k) = 3.18\,\text{V}.$$

**Example 8.4:** For the figure below, calculate all DC currents and voltages.

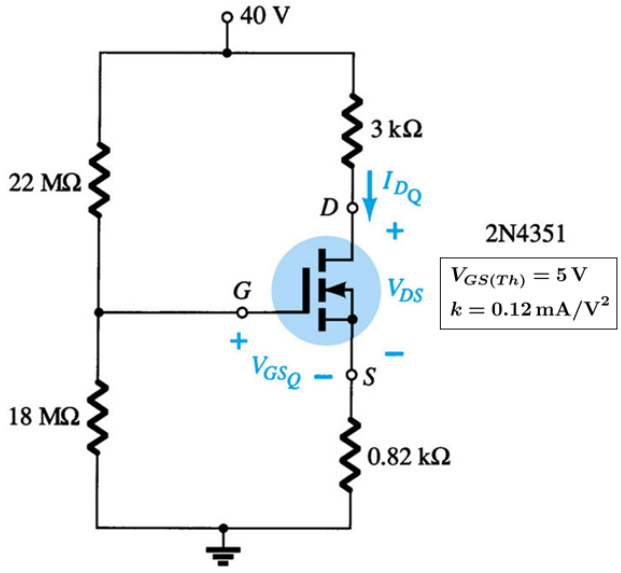



Figure 8.17: Voltage-divider bias EMOSFET circuit for Example 8.4.

**Solution:** Let us find $V_G$, and express $V_{GS}$ using the KVL equation of $GS$-loop and $I_D$ from

the transfer characteristics equation

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{18M}{22M + 18M} 40 = 18\,\text{V}.$$
$$V_{GS} = V_G - I_D R_S = 18 - 0.82k\, I_D$$
$$I_D = k\left(V_{GS} - V_{GS(Th)}\right)^2 = (0.12m)\left(V_{GS} - 5\right)^2$$

where $V_{GS} \geq 5\,\text{V}$ .

We obtain $I_{DQ}$ and $V_{GSQ}$ by drawing these two equations on the same graph as shown in Figure 8.18 below

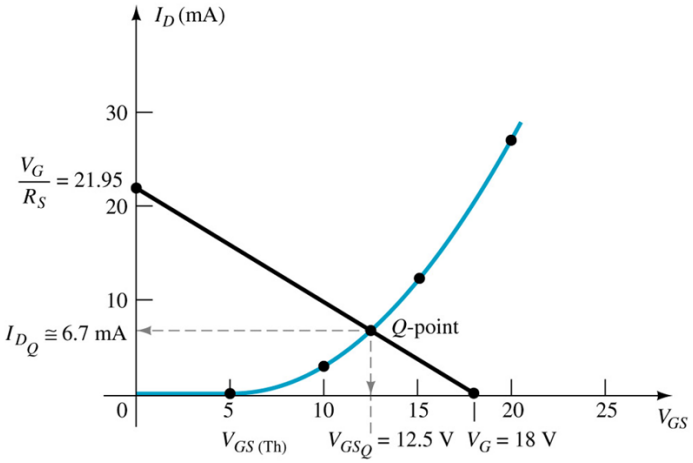



Figure 8.18: Obtaining $I_{DQ}$ graphically for the circuit in Figure 8.17.

Finally, we obtain $V_{DSQ}$ from the $DS$-loop as

$$V_{DSQ} = V_{DD} - I_{DQ}\left(R_D + R_S\right) = 40 - (6.7m)\left(3k + 0.82k\right) = 14.4\,\text{V}.$$

### 8.3.4 Voltage-Feedback Bias Configuration

A voltage-feedback bias EMOSFET circuit is given in Figure 8.19 below

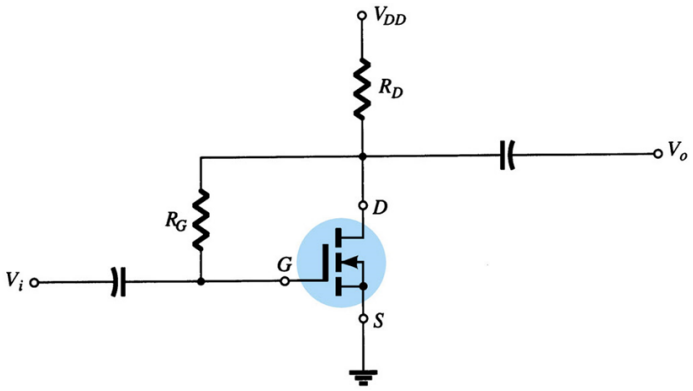



Figure 8.19: Voltage-feedback bias EMOSFET circuit.

Let us start DC analysis by drawing the DC equivalent circuit as shown in Figure 8.20 below

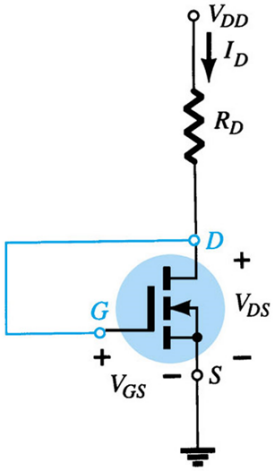



Figure 8.20: DC equivalent circuit (with $I_G = 0$) of the voltage-feedback configuration in Figure 8.19.

Note that $R_G$ is ignored as $I_G = 0$.

#### 8.3.4.1 Gate-Source Loop

We can write KVL equation on the $GS$-loop

$$V_{DD} - V_{GS} - I_D R_D = 0 \tag{8.3.25}$$

$$V_{GS} = V_G - I_D R_D \tag{8.3.26}$$

Then, we obtain $V_{GSQ}$ and $I_{DSQ}$ by solving the following two equations simultaneously

$$V_{GS} = V_{DD} - I_D R_D \quad \ldots \text{transfer load-line} \tag{8.3.27}$$

$$I_D = k\left(V_{GS} - V_{GS(Th)}\right)^2 \quad \ldots \text{transfer characteristics} \tag{8.3.28}$$

It is better to obtain the result graphically by plotting equations (8.3.27) and (8.3.28) on the same graph as shown in Figure 8.21 below.

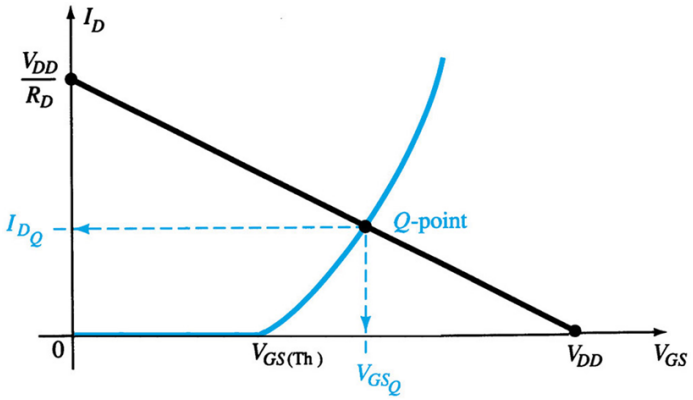



Figure 8.21: Graphical solution (for transfer load-line and transfer characteristics equations) for the voltage-feedback configuration in Figure 8.19.

The graphically obtained current value $I_{DQ}$ may be refined using equations (8.3.27) and (8.3.28) in an iteration loop as follows

1. Insert graphically obtained $I_D$ into (8.3.27) and obtain a $V_{GS}$ value
2. Insert $V_{GS}$ obtained in Step 1 into (8.3.28) and obtain a new $I_D$ value to be used in Step 1.
3. Repeat Step 1 and Step 2 until $\Delta I_D$, the difference between the old $I_D$ used in Step 1 and new $I_D$ obtained in Step 2, is small enough.

#### 8.3.4.2 Drain-Source Loop

Let us write down the KVL equation on the $DS$-loop

$$V_{DD} - I_D R_D - V_{DS} = 0 \qquad \ldots \text{DC load-line equation} \quad (8.3.29)$$

As we already obtained $I_{DQ}$ in Figure 8.21 we find $V_{DSQ}$ as

$$\boxed{V_{DSQ} = V_{DD} - I_{DQ} R_D} \qquad (8.3.30)$$

Note that, here $V_{DSQ} = V_{GSQ}$.

Thus, we obtained the $Q$-point $(I_{DQ}, V_{DSQ})$, i.e., the operating point.

**Example 8.5:** For the figure below, calculate all DC currents and voltages.

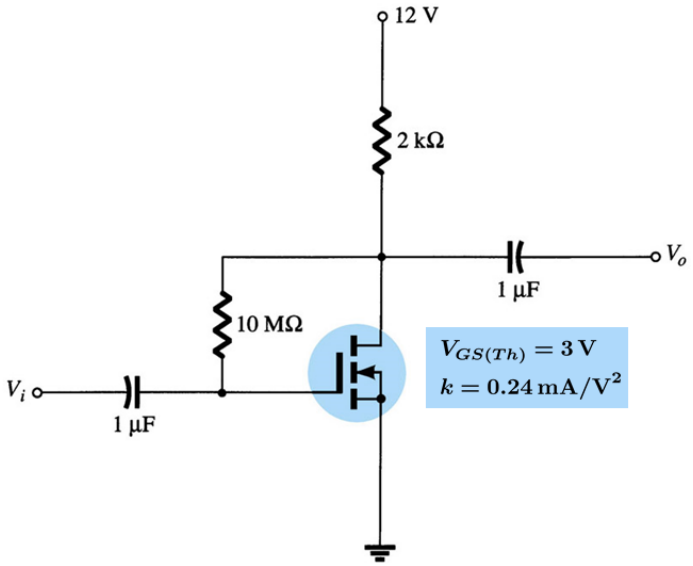



Figure 8.22: Voltage-feedback bias EMOSFET circuit for Example 8.5.

**Solution:** Let us find $V_G$, and express $V_{GS}$ using the KVL equation of $GS$-loop and $I_D$ from the transfer characteristics equation

$$V_{GS} = V_{DD} - I_D R_D = 12 - 2k\, I_D$$
$$I_D = k \left(V_{GS} - V_{GS(Th)}\right)^2 = (0.24m) \left(V_{GS} - 3\right)^2$$

where $V_{GS} \geq 3\,\text{V}$.

We obtain $I_{DQ}$ and $V_{GSQ}$ by drawing these two equations on the same graph as shown in Figure 8.23 below

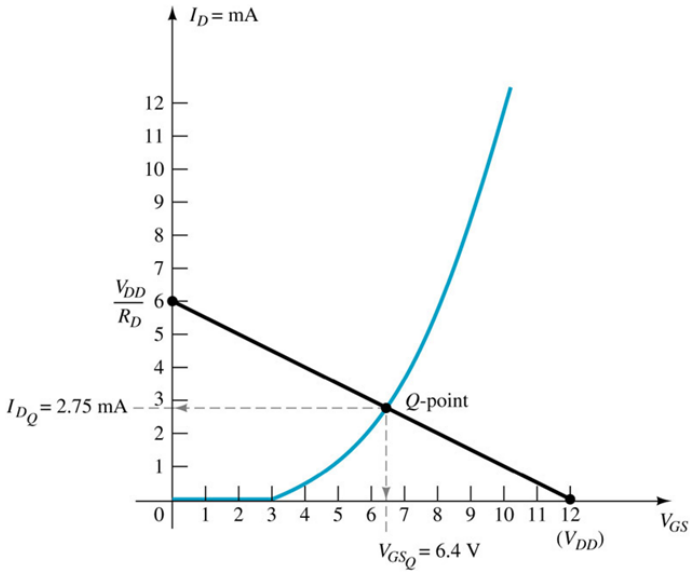



Figure 8.23: Obtaining $I_{DQ}$ graphically for the circuit in Figure 8.22.

Finally, we obtain $V_{DSQ}$ from the $DS$-loop as

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 12 - (2.75m)(2k) = 6.4\,\text{V}.$$

### 8.3.5 $p$-channel FETs

The analysis for $p$-channel FET circuits is the same as that for $n$-channel FET circuits.

The only differences are that

1. Currents are flowing in the opposite direction.
2. Voltages have opposite polarity, e.g., $V_{SG} \geq V_{SG(Th)}$ (i.e., $V_{GS} \leq V_{GS(Th)}$) is needed to turn on a $p$-channel FET.
3. If properly biased, then $V_S > V_D$, i.e., $V_{SD} > 0$.

**Example 8.6:** For the figure below, calculate all DC currents and voltages.

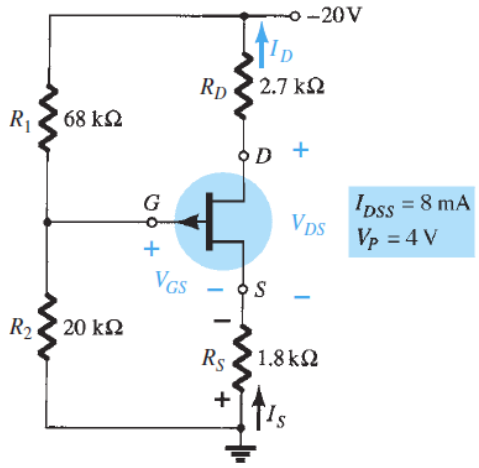



Figure 8.24: Voltage-divider bias JFET circuit for Example 8.6.

**Solution:** Let us find $V_G$, and express $V_{GS}$ using the KVL equation of $GS$-loop and $I_D$ from the transfer characteristics equation

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{20k}{68k + 20k}(-20) = -4.55\,\text{V}.$$
$$V_{GS} = V_G + I_D R_S = -4.55 + 1.8k\, I_D$$
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = (8m)\left(1 - \frac{V_{GS}}{4}\right)^2$$

where $-4 \leq V_{GS} \leq 0$.

We obtain $I_{DQ}$ and $V_{GSQ}$ by drawing these two equations on the same graph as shown in Figure 8.25 below

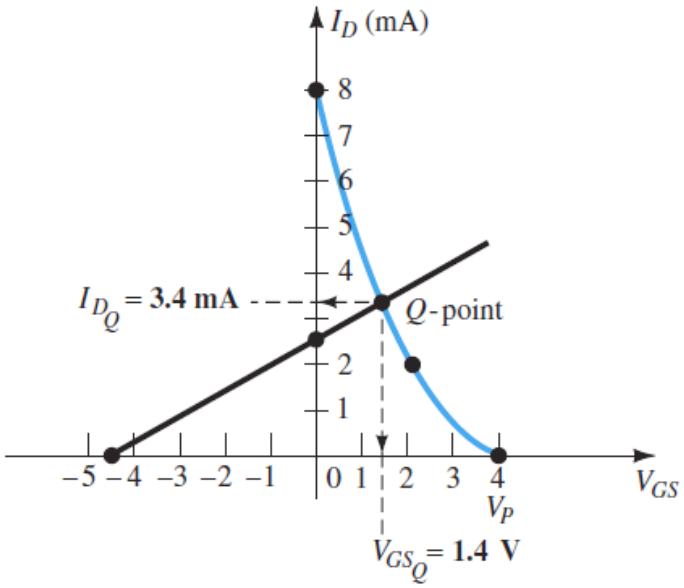



Figure 8.25: Obtaining $I_{DQ}$ graphically for the circuit in Figure 8.24.

Finally, we obtain $V_{DSQ}$ from the $DS$-loop as

$$V_{DSQ} = V_{DD} + I_{DQ}\,(R_D + R_S) = (-20) + (3.4m)\,(2.7k + 1.8k) = -4.7\,\text{V}.$$

Thus, $V_{SDQ} = 4.7\,\text{V}$.

## 8.4 Practical Applications

Some practical FET applications are listed below:

- Voltage-controlled resistor
- JFET voltmeter
- Timer network
- Fiber optic circuitry
- MOSFET relay driver

## 8.5 Summary

Summary of $n$-channel JFET and MOSFET bias circuits are given in Figure 8.26 and Figure 8.27, respectively.

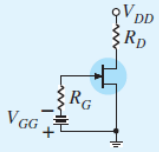
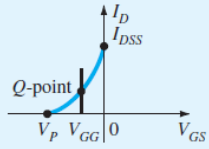
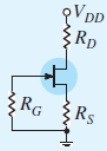
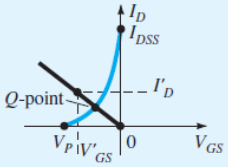
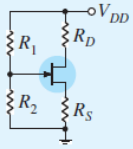
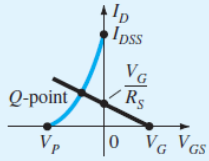
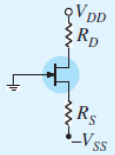
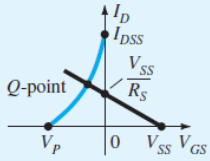
| Type | Configuration | Pertinent Equations | Graphical Solution |
|---|---|---|---|
| JFET<br>Fixed-bias |  | $V_{GS_Q} = -V_{GG}$<br>$V_{DS} = V_{DD} - I_D R_D$ |  |
| JFET<br>Self-bias |  | $V_{GS} = -I_D R_S$<br>$V_{DS} = V_{DD} - I_D(R_D + R_S)$ |  |
| JFET<br>Voltage-divider<br>bias |  | $V_G = \dfrac{R_2}{R_1 + R_2} V_{DD}$<br>$V_{GS} = V_G - I_D R_S$<br>$V_{DS} = V_{DD} - I_D(R_D + R_S)$ |  |
| JFET<br>Common-gate |  | $V_{GS} = V_{SS} - I_D R_S$<br>$V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$ |  |

Figure 8.26: $n$-channel JFET bias circuits.

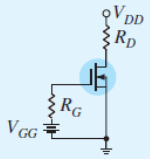
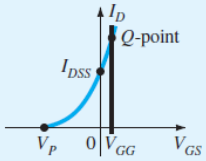
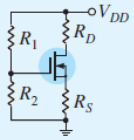
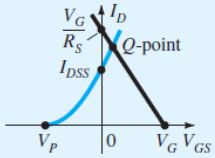
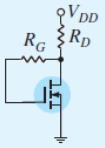
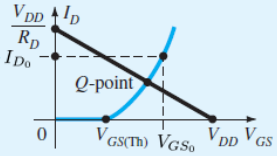
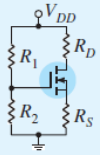
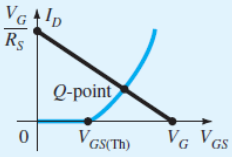
| Type | Configuration | Pertinent Equations | Graphical Solution |
|---|---|---|---|
| Depletion-type MOSFET Fixed-bias |  | $V_{GS_Q} = +V_{GG}$<br>$V_{DS} = V_{DD} - I_D R_D$ |  |
| Depletion-type MOSFET Voltage-divider bias |  | $V_G = \frac{R_2}{R_1 + R_2} V_{DD}$<br>$V_{GS} = V_G - I_S R_S$<br>$V_{DS} = V_{DD} - I_D(R_D + R_S)$ |  |
| Enhancement type MOSFET Feedback configuration |  | $V_{GS} = V_{DS}$<br>$V_{GS} = V_{DD} - I_D R_D$ |  |
| Enhancement type MOSFET Voltage-divider bias |  | $V_G = \frac{R_2}{R_1 + R_2} V_{DD}$<br>$V_{GS} = V_G - I_D R_S$ |  |

Figure 8.27: $n$-channel MOSFET bias circuits.

# Chapter 9

# AC-DC Load Lines of FET Circuits

## 9.1 FET AC Analysis

1. Draw the AC equivalent circuit (signal frequency is infinity, i.e., $f = \infty$)
   a) Capacitors are short circuit, i.e., $X_C \to 0$.
   b) Kill the DC power sources (short-circuit DC voltage sources and open-circuit DC current sources).
2. Write KVL for the loop which contains $DS$ terminals
   a) Develop AC load-line equation.
3. Draw AC-DC load lines
   a) Find available swings for a given input or find maximum undistorted swings.

### 9.1.1 AC and DC Load Lines

- AC and DC load line equations of FETs are similar to the AC and DC load line equations of BJTs where gate ($G$), drain ($D$) and source ($S$) replace base ($B$), collector ($C$) and emitter ($E$), respectively, in the subscripts of the equations.
- Thus, FET DC load line equation is given by

$$V_{DS} = V_{DD} - I_D R_{DC} \tag{9.1.1}$$

  where $R_{DC}$ is the equivalent output-loop ($DS$-loop) DC resistance. Hence, the rearranged **DC load line equation** (DC output equation) is given by

$$\boxed{I_D = \frac{-1}{R_{DC}} V_{DS} + \frac{V_{DD}}{R_{DC}}} \tag{9.1.2}$$

- Similarly, FET AC load line equation is given by

$$v_{DS} = -i_D R_{ac} + V_{DSQ} + I_{DQ} R_{ac} \tag{9.1.3}$$

where $R_{ac}$ is the equivalent output-loop ($DS$-loop) AC resistance, $v_{DS} = V_{DSQ} + v_{ds}$ and $i_D = I_{DQ} + i_d$. Hence, the rearranged **AC load line equation** (AC output equation) is given by

$$\boxed{i_D = \frac{-1}{R_{ac}} v_{DS} + I_{DQ} + \frac{V_{DSQ}}{R_{ac}}} \tag{9.1.4}$$

Let us draw DC and AC load lines together as shown in Figure 9.1 below.

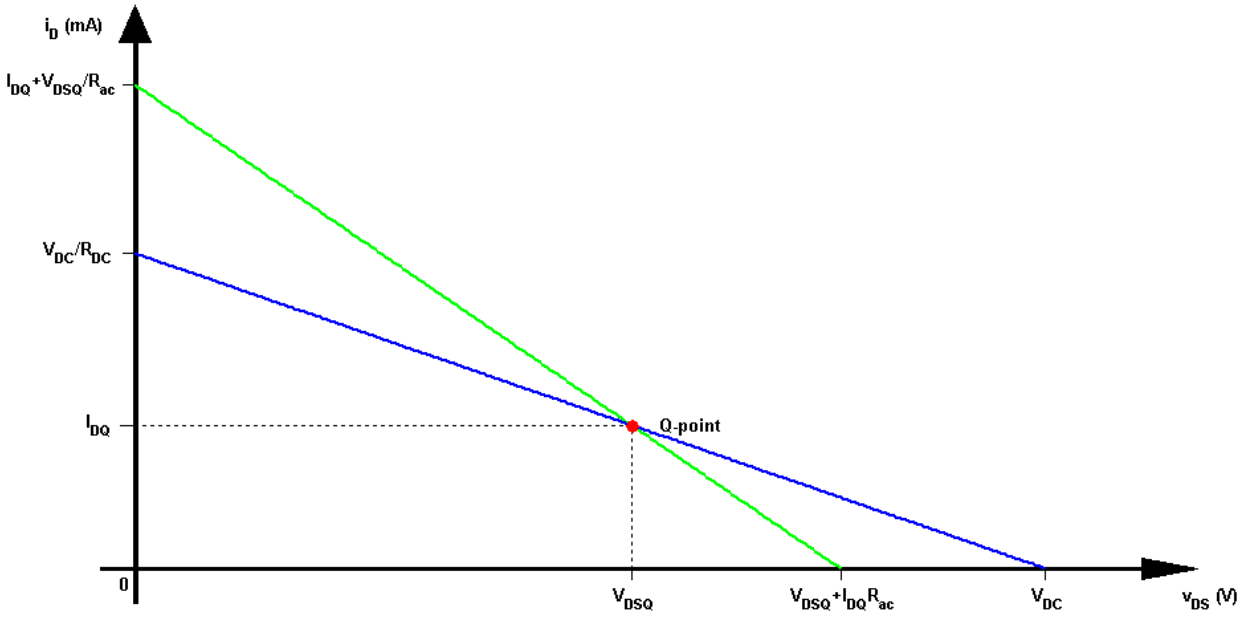



Figure 9.1: AC-DC load lines for FETs.

Once the $Q$-point is known, **peak** values of the **maximum undistorted** voltage and current **swings** $v_{ds(p)(\max)}$ and $i_{d(p)(\max)}$ are given by

$$\boxed{v_{ds(p)(\max)} = \min\left(V_{DSQ}, I_{DQ} R_{ac}\right)} \tag{9.1.5}$$

and

$$i_{d(p)(\max)} = \min\left(I_{DQ}, \frac{V_{DSQ}}{R_{ac}}\right) \tag{9.1.6}$$

respectively

### 9.1.2 Maximum Symmetric Undistorted Swing Design

Once we obtained the desired $Q$-point in the middle of the AC load line, i.e.,

$$\boxed{I_{DQ} = \frac{V_{DD}}{R_{DC} + R_{ac}}} \tag{9.1.7}$$

then the maximum available undistorted output swings will be obtained as shown in Figure 9.2 below.

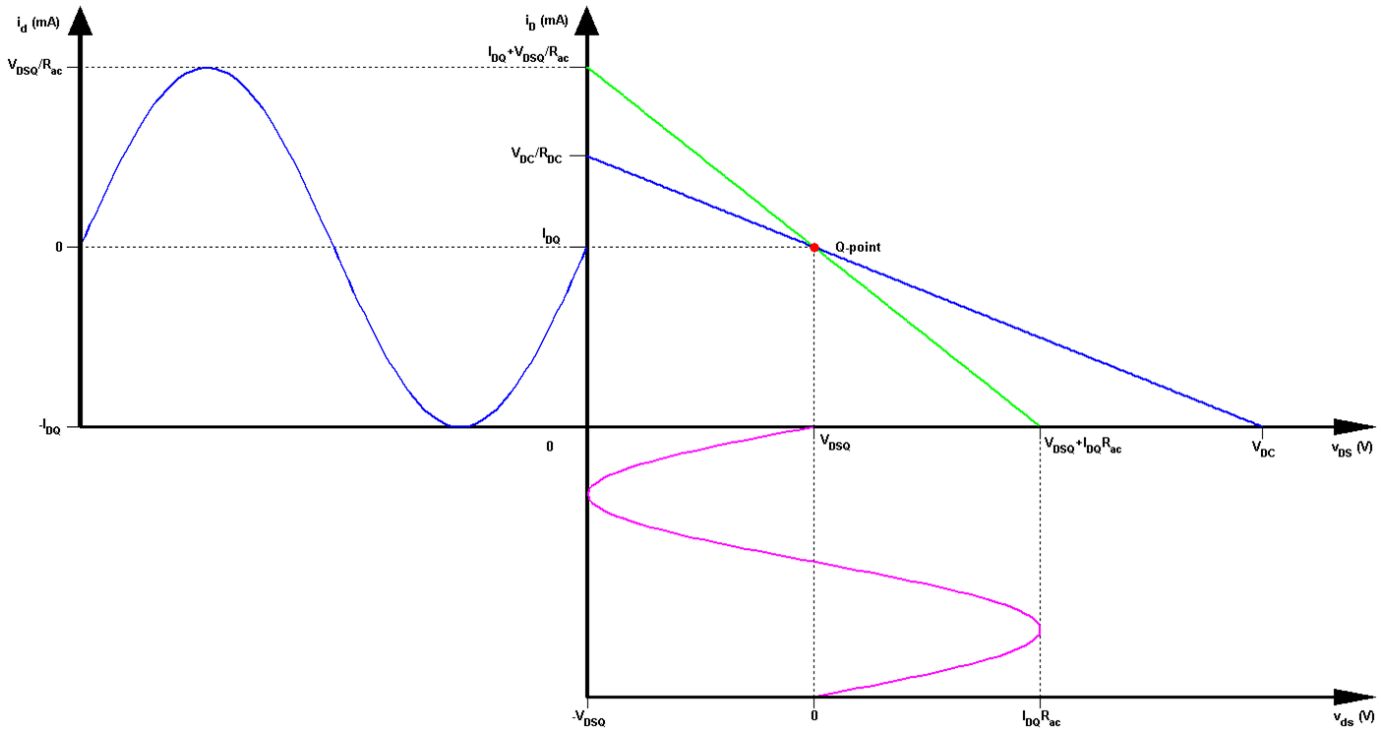



Figure 9.2: Maximum undistorted swing design for FETs with $Q$-point in the middle of the AC load line.

### 9.1.3 Other Amplifier Configurations

We developed and plotted AC-DC load lines for the common-source configuration. Now, let us look at other configurations.

- Common-gate (CG) configuration

  1. Obtain $R_{ac}$ from the $DG$ loop.
  2. Obtain $R_{DC}$ from the $DS$ loop.
  3. Draw the AC-DC load lines $i_D$ vs. $v_{DS}$ as before.

     NOTE: You can also draw the AC-DC load lines as $i_D$ vs. $v_{DG}$ by shifting the voltage axis by $V_{GSQ}$ volts to the left as $V_{DGQ} = V_{DSQ} - V_{GSQ}$. Thus, current axis will be drawn at $V_{DG}|_{I_D=0} = -V_{GSQ}$ volts not at 0 V.

- Common-drain (CD) configuration (also known as source-follower)

  1. Obtain $R_{ac}$ and $R_{DC}$ from the $DS$ loop as before.
  2. Draw the AC-DC load lines $i_S$ vs. $v_{DS}$ where $i_S = i_D$.

- For $p$-channel FETs, we express the currents in the reverse direction (i.e., having positive current values) and reverse the polarity of the terminal voltages (i.e., having positive voltage values), and then draw the AC-DC load lines, e.g., $i_D$ vs. $v_{SD}$.

# Chapter 10

# BJT Small-Signal Analysis

## 10.1 Purpose of SSAC Analysis

The purpose of small-signal AC (SSAC) analysis to determine the **three** parameters of an amplifier **input resistance**, **output resistance** and **gain**. In this course, we are mostly interested in the two-port voltage-gain amplifier model shown in Figure 10.1 below.

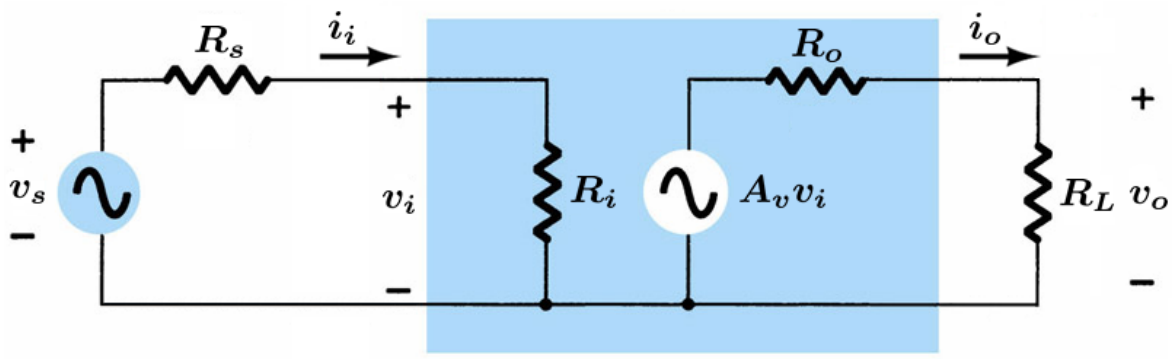



Figure 10.1: Two-port voltage-gain amplifier model.

- Input resistance $R_i$ is defined by the no-load input voltage of the amplifier divided by the no-load input current to the amplifier, i.e.,

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty}} \tag{10.1.1}$$

  NOTE: Input resistance **cannot** include the source resistance $R_s$.

- Output resistance $R_o$ is obtained by the test-voltage method, i.e., by dividing the test voltage value with the measured test current value. In the test-voltage method, load is replaced with a test voltage $v_{\text{test}}$ and the independent power sources ($v_s$ or $i_s$) are killed, i.e., $v_s = 0$ or $i_s = 0$. Thus, output resistance $R_o$ is given by

$$\boxed{R_o = \left.\frac{v_{\text{test}}}{i_{\text{test}}}\right|_{v_s=0, R_L=v_{\text{test}}}} \tag{10.1.2}$$

NOTE: Output resistance **cannot** include the load resistance $R_L$.

- No-load voltage gain $A_v$ (or $A_{V_{\text{NL}}}$) is defined by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty}} \tag{10.1.3}$$

- When load is connected, the voltage gain will decrease due to the voltage-divider consisting of $R_L$ and $R_o$. So, voltage gain with load, $A_V$, is given by

$$A_V = \frac{v_o}{v_i} = \left(\frac{v_o}{A_v v_i}\right)\left(\frac{A_v v_i}{v_i}\right) = \frac{R_L}{R_o + R_L} A_v \tag{10.1.4}$$

- Current gain $A_i$ is defined by the output current versus the input current, i.e.,

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_L}{v_i/R_i} = \frac{R_i}{R_L} A_V = \frac{R_i}{R_o + R_L} A_v \tag{10.1.5}$$

- Finally, overall voltage gain $A_{Vs}$ is given by

$$\boxed{A_{Vs} = \frac{v_o}{v_s} = \frac{R_L}{R_o + R_L} A_v \frac{R_i}{R_s + R_i}} \tag{10.1.6}$$

### 10.1.1 BJT SSAC Analysis Steps

1. Draw the SSAC equivalent circuit
   a) Draw the AC equivalent circuit (signal frequency is infinity, i.e., $f = \infty$)
      i. Capacitors are short circuit, i.e., $X_C \to 0$.
      ii. Kill the DC power sources (i.e., AC value of DC sources is zero).
   b) Replace BJT with its small-signal equivalent model (e.g., hybrid equivalent model or $r_e$ model).
2. Calculate the three amplifier parameters: $R_i$, $R_o$ and $A_v$
   a) Calculate no-load input resistance, $R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty}$.
   b) Calculate output resistance, $R_o$.
   c) Calculate no-load voltage gain, $A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$.

## 10.2 BJT Small-Signal Models

A small-signal model is an equivalent circuit that represents the SSAC characteristics of the transistor. It uses circuit elements that approximate the behavior of the transistor.

Two commonly used models used in SSAC analysis of BJTs are given below:

- hybrid equivalent model
- $r_e$ model

Mostly, we are going to use the **hybrid equivalent model**. But, we are going to introduce and provide results for the $r_e$ model as well.

**NOTE:** Small-signal equivalent model and its analysis are the same for both *npn* and *pnp* transistors.

### 10.2.1 Hybrid Equivalent Model

Parameters of the hybrid equivalent circuit provide the entire set on the specification sheet of a BJT and cover all operating conditions. Generalized hybrid equivalent circuit for any transistor configuration is provided in Figure 10.2 below.

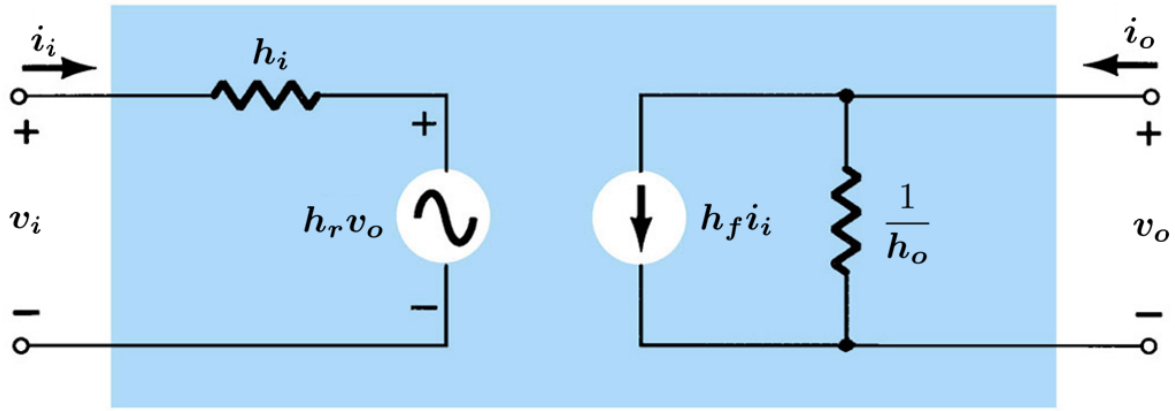



Figure 10.2: Complete hybrid equivalent circuit.

Here,

- $h_i$: input resistance
- $h_r$: reverse transfer voltage ratio ($v_i/v_o$)
- $h_f$: forward transfer current ratio ($i_o/i_i$)
- $h_o$: output conductance

For a specific configuration, the model parameters modified with the label of the common-mode terminal in their subscript. So, common-emitter and common-base configurations and their hybrid equivalent models are shown in Figure 10.3 and Figure 10.4 below, respectively.

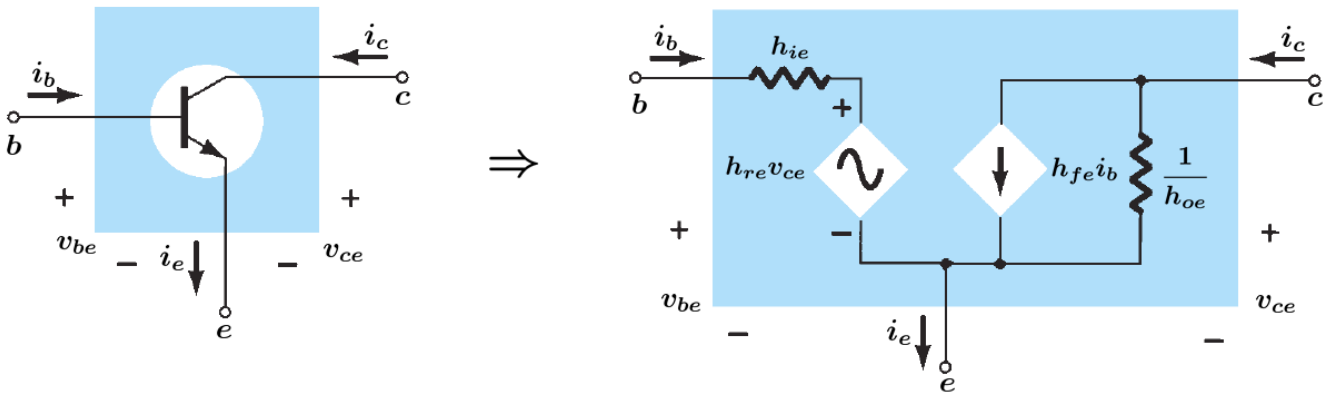



Figure 10.3: Common-emitter configuration and its complete hybrid equivalent circuit.

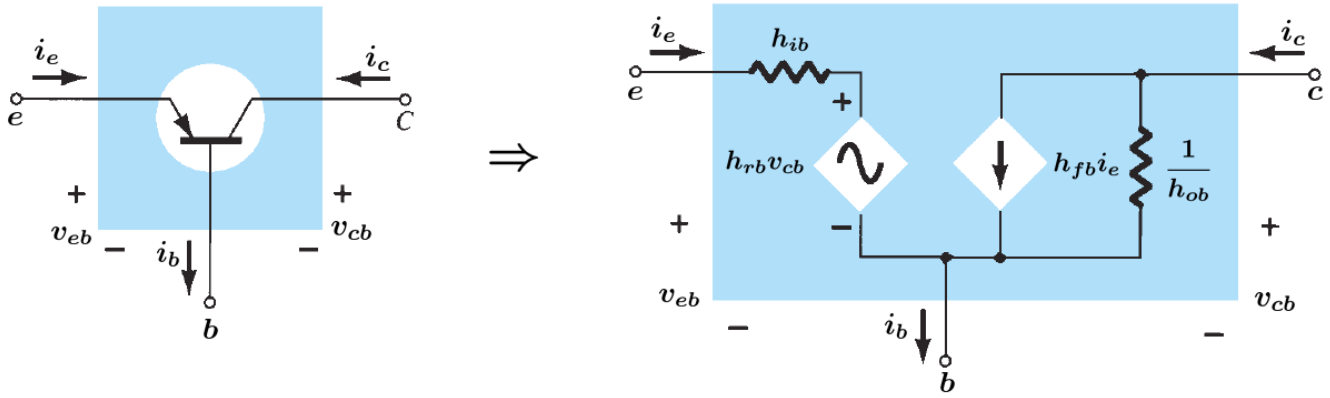



Figure 10.4: Common-base configuration and its complete hybrid equivalent circuit.

- For the common-collector configuration, we always use the common-emitter hybrid equivalent model.

#### 10.2.1.1 Simplified Hybrid Equivalent Model

Because $h_r$ is normally a relatively small quantity, its removal is approximated by $h_r \approx 0$ and $h_r v_o = 0$, resulting in the simplified hybrid equivalent circuit shown in Figure 10.5 below. In this course, we are going to use the **simplified hybrid equivalent model**.

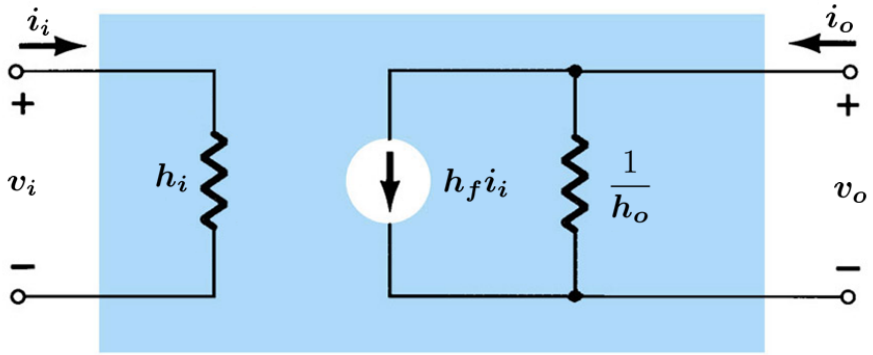



Figure 10.5: Simplified hybrid equivalent circuit.

This circuit, can be further simplified if a value for the parameter $h_o$ or $1/h_o$ is not provided. In that case, we can safely assume that $h_o = 0$ or $1/h_o = \infty$ resulting in the approximate hybrid equivalent circuit shown in Figure 10.6 below.

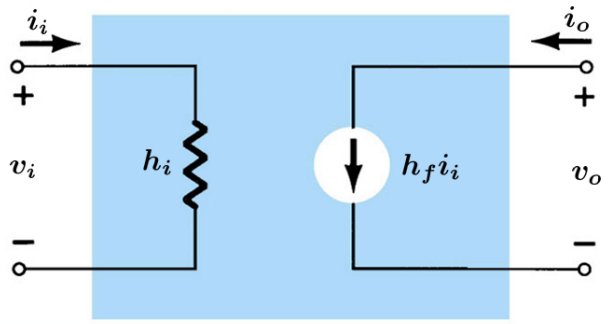



Figure 10.6: Approximate hybrid equivalent circuit.

#### 10.2.1.2 Common-Emitter Hybrid Equivalent Model

Common-emitter simplified hybrid equivalent circuit is shown in Figure 10.7 below.

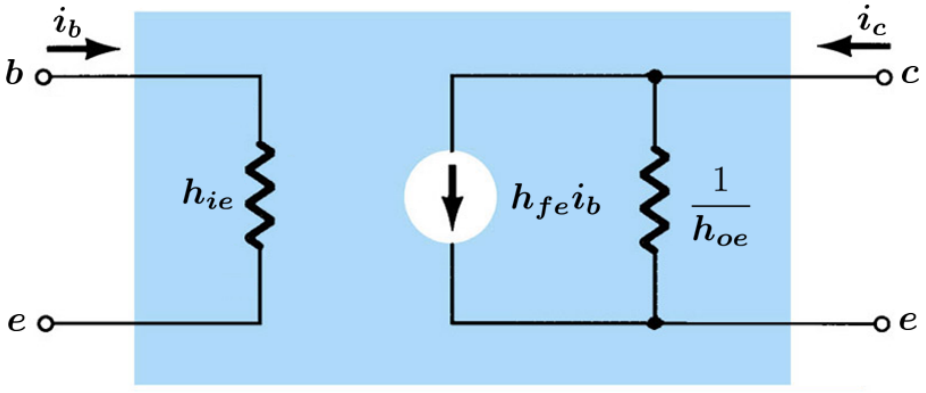



Figure 10.7: Common-emitter simplified hybrid equivalent circuit.

Here, the $h$-parameters are defined as below

$$h_{ie} = \left.\frac{\partial V_{BE}}{\partial I_B}\right|_{Q\text{-point}} = \frac{\gamma}{I_{BQ}} \quad \ldots \text{see diode dynamic resistance in Section 1.3.11} \tag{10.2.7}$$

$$h_{fe} = \left.\frac{\partial I_C}{\partial I_B}\right|_{Q\text{-point}} = \beta_{ac} \tag{10.2.8}$$

$$1/h_{oe} = \left.\frac{\partial V_{CE}}{\partial I_C}\right|_{Q\text{-point}} = \frac{V_A + V_{CEQ}}{I_{CQ}} \quad \ldots V_A \text{ is the early voltage and } V_A \gg V_{CEQ} \tag{10.2.9}$$

Typical values of $h_{fe}$ run from 50 to 200, $h_{ie}$ run from 500 Ω to 7 kΩ, and $1/h_{oe}$ run from 40 kΩ to 100 kΩ.

Note that, as $I_{CQ} = \beta I_{BQ}$ and $I_{EQ} = (\beta + 1)\, I_{BQ}$, we can also express $h_{ie}$ in terms of $I_{CQ}$ or $I_{EQ}$ as follows

$$h_{ie} = \frac{\gamma}{I_{BQ}} \tag{10.2.10}$$

$$= h_{fe}\frac{\gamma}{I_{CQ}} \tag{10.2.11}$$

$$= (h_{fe} + 1)\,\frac{\gamma}{I_{EQ}} \tag{10.2.12}$$

where $\gamma = kT/q$ is the thermal voltage and have fixed values for a given temperature, e.g., $\gamma = 26\,\text{mV}$ at room temperature $T = 300\,\text{K}$.

#### 10.2.1.3 Common-Emitter $r_e$ Model

Common-emitter $r_e$ model is shown in Figure 10.8 below.

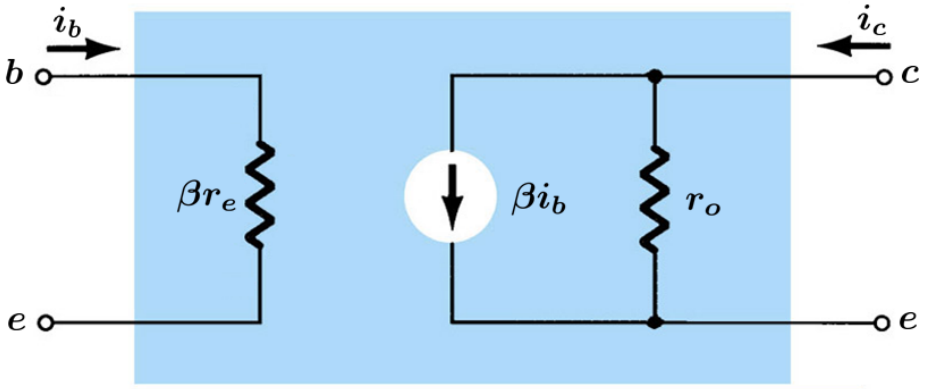



Figure 10.8: Common-emitter $r_e$ model.

One-to-one correspondence with the $h$-parameters are given below,

$$h_{fe} = \beta \tag{10.2.13}$$

$$h_{ie} = (\beta + 1)\, r_e \cong \beta r_e \tag{10.2.14}$$

$$1/h_{oe} = r_o. \tag{10.2.15}$$

Thus, $\beta = h_{fe}$, $\beta r_e = h_{ie}$ and $r_o = 1/h_{oe}$.

#### 10.2.1.4 Common-Base Hybrid Equivalent Model

Common-base simplified hybrid equivalent circuit is shown in Figure 10.9 below.

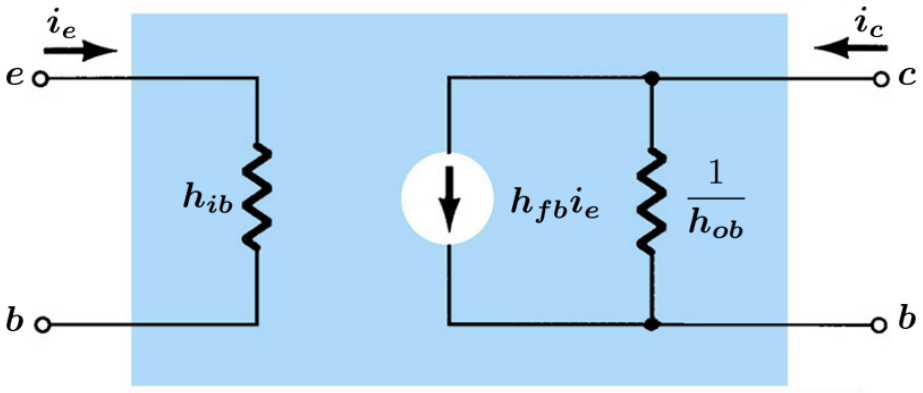



Figure 10.9: Common-base simplified hybrid equivalent circuit.

Here, the $h$-parameters are defined as below,

$$h_{ib} = \left.\frac{\partial V_{BE}}{\partial I_E}\right|_{Q\text{-point}} = \frac{\gamma}{I_{EQ}} \quad \ldots \text{see diode dynamic resistance in Section 1.3.11} \tag{10.2.16}$$

$$h_{fb} = -\left.\frac{\partial I_C}{\partial I_E}\right|_{Q\text{-point}} = -\alpha_{ac} \cong -1 \tag{10.2.17}$$

$$1/h_{ob} = \left.\frac{\partial V_{CB}}{\partial I_C}\right|_{Q\text{-point}} \approx \infty \tag{10.2.18}$$

Typically, $h_{fb} = -1$, and $h_{ib}$ run from $5\,\Omega$ to $50\,\Omega$, and $1/h_{ob}$ is in the megohm range. Thus, $1/h_{ob} \gg 1/h_{oe}$.

Note that, the relationship between $h_{ib}$ and $h_{ie}$ is given below

$$h_{ie} = (h_{fe} + 1)\, h_{ib} \tag{10.2.19}$$

or $h_{ib} = \dfrac{h_{ie}}{h_{fe} + 1}$.

#### 10.2.1.5 Common-Base $r_e$ Model

Common-base $r_e$ model is shown in Figure 10.10 below.

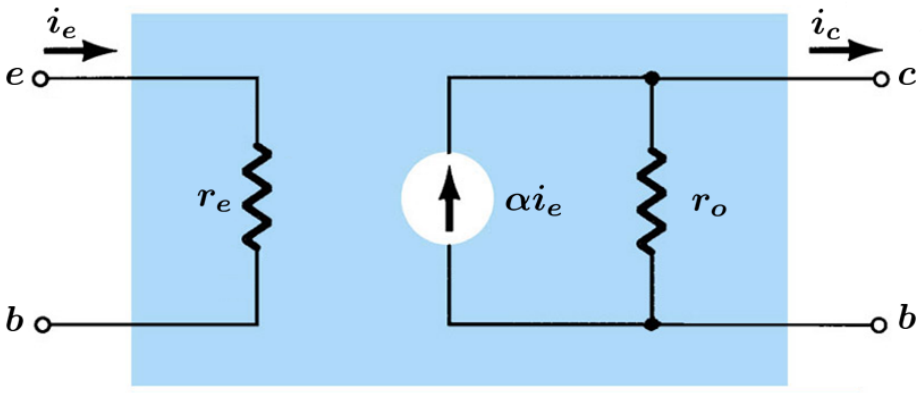



Figure 10.10: Common-base $r_e$ model.

One-to-one correspondence with the $h$-parameters are given below

$$h_{fb} = -\alpha \tag{10.2.20}$$
$$h_{ib} = r_e \tag{10.2.21}$$
$$1/h_{ob} = r_o. \tag{10.2.22}$$

Thus, $\alpha = -h_{fb} \cong 1$, $r_e = h_{ib}$ and $r_o = 1/h_{ob} \cong \infty$. Note that, minus sign is due to the direction of the current source.

#### 10.2.1.6 Phase Relationship

The phase relationship between input and output depends on the amplifier configuration circuit as listed below.

- Common-Emitter: 180 degrees
- Common-Base: 0 degrees
- Common-Collector: 0 degrees (Emitter-Follower)

## 10.3 Common-Emitter Fixed-Bias Configuration

Common-emitter fixed-bias configuration is given in Figure 10.11 below

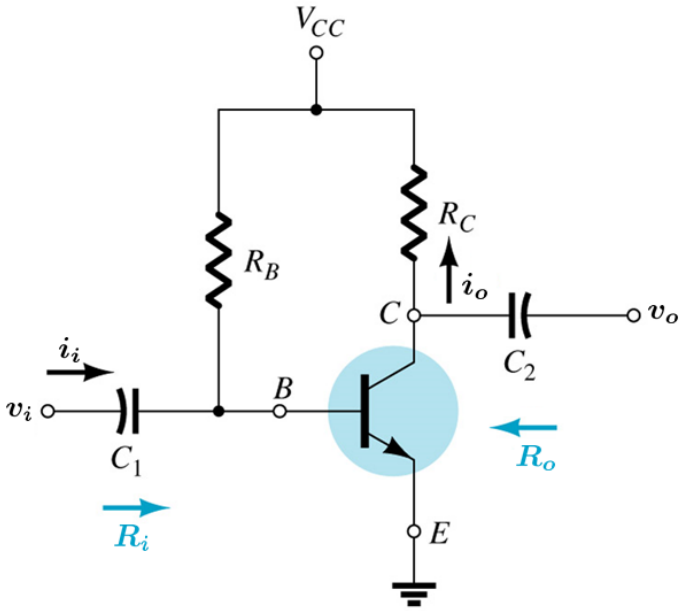



Figure 10.11: Common-emitter fixed-bias configuration.

Let us start SSAC analysis by drawing the AC equivalent circuit as shown in Figure 10.12 below

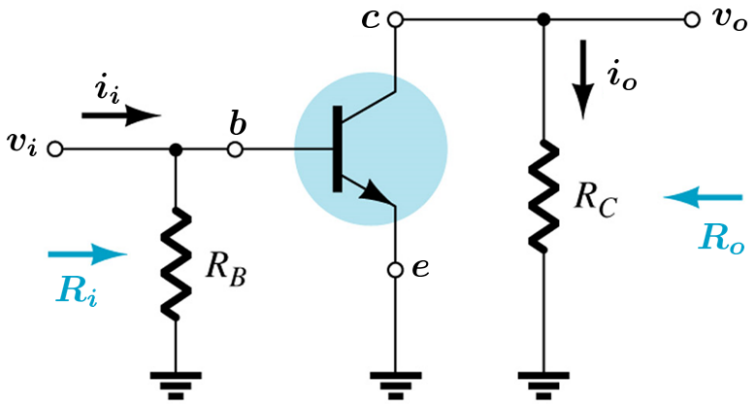



Figure 10.12: AC equivalent circuit of the fixed-bias circuit in Figure 10.11.

Then, we are going to replace BJT with its common-emitter hybrid equivalent model as shown in Figure 10.13 below

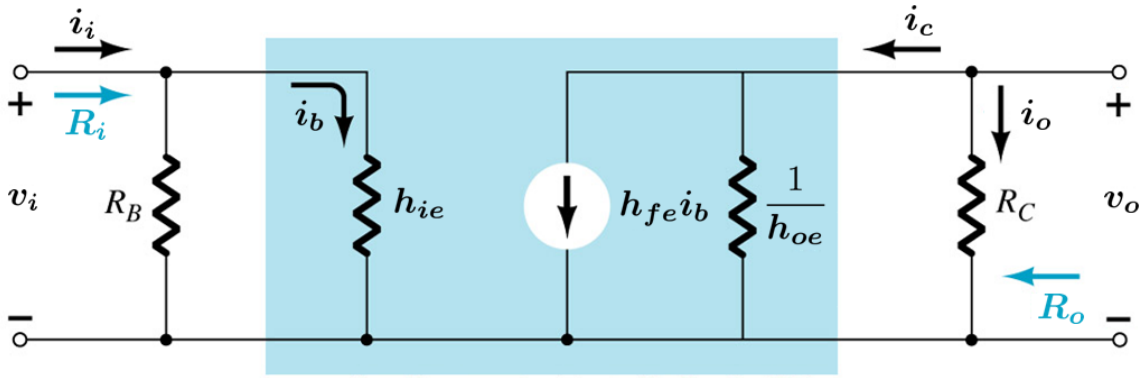



Figure 10.13: Small-signal equivalent circuit of the fixed-bias circuit in Figure 10.11.

- Obtain $h_{fe}$ and $1/h_{oe}$ from the specification sheet of the transistor or by testing the transistor using a curve tracer. Calculate $h_{ie}$ using the DC analysis values as $h_{ie} = \dfrac{26\,\text{mV}}{I_{BQ}} = h_{fe}\dfrac{26\,\text{mV}}{I_{CQ}}$.

### 10.3.1 Input Resistance

Input resistance $R_i$ is given as

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_B||h_{ie}} \tag{10.3.23}$$

- If $R_B \geq 10h_{ie}$, then $R_i$ simplifies to $R_i = h_{ie}$.
- Input resistance $R_i$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_i = R_B||\beta r_e \tag{10.3.24}$$

### 10.3.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$\begin{aligned} A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} &= \left(\frac{v_o}{h_{fe}i_b}\right)\left(\frac{h_{fe}i_b}{i_b}\right)\left(\frac{i_b}{v_i}\right) \\ &= \left(-R_C||1/h_{oe}\right)\left(h_{fe}\right)\left(\frac{1}{h_{ie}}\right) \\ &= -\frac{h_{fe}\left(R_C||1/h_{oe}\right)}{h_{ie}} \end{aligned}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = -\frac{h_{fe}\left(R_C||1/h_{oe}\right)}{h_{ie}}} \tag{10.3.25}$$

- No-load voltage gain $A_v$ according to the $\boldsymbol{r_e}$ **model** is given by

$$A_v = -\frac{R_C||r_o}{r_e} \tag{10.3.26}$$

- If $1/h_{oe} \geq 10R_C$, no-load voltage gain $A_v$ reduces to

$$A_v = -\frac{h_{fe}R_C}{h_{ie}} \qquad \ldots r_e \text{ model: } A_v = -\frac{R_C}{r_e} \tag{10.3.27}$$

- For the circuit in Figure 10.13, we can obtain the current gain $A_i$ as follows

$$\begin{aligned} A_i = \frac{i_o}{i_i} = \frac{v_o/R_C}{v_i/R_i} &= \frac{R_i}{R_C}\frac{v_o}{v_i} \\ &= \frac{R_i}{R_C}A_v \end{aligned} \tag{10.3.28}$$

- If $1/h_{oe} \geq 10R_C$ and $R_B \geq 10h_{ie}$, current gain $A_i$ reduces to

$$A_i = -h_{fe} \qquad \ldots r_e \text{ model: } A_i = -\beta \tag{10.3.29}$$

### 10.3.3 Output Resistance

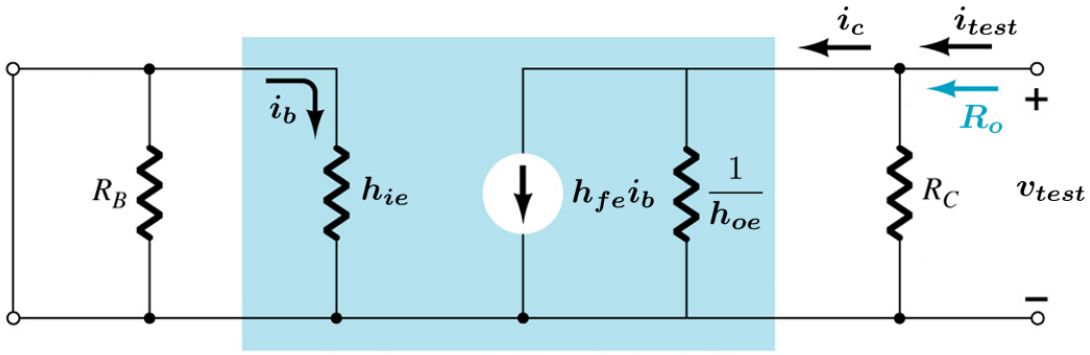



Figure 10.14: Test voltage circuit of Figure 10.13 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 10.14 above. Note that in the circuit $i_b = 0$, so $h_{fe}i_b = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_C||1/h_{oe}} \tag{10.3.30}$$

- If $1/h_{oe} \geq 10R_C$, then $R_o$ simplifies to $R_o = R_C$.
- Output resistance $R_o$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_o = R_C||r_o \tag{10.3.31}$$

### 10.3.4 Phase Relationship

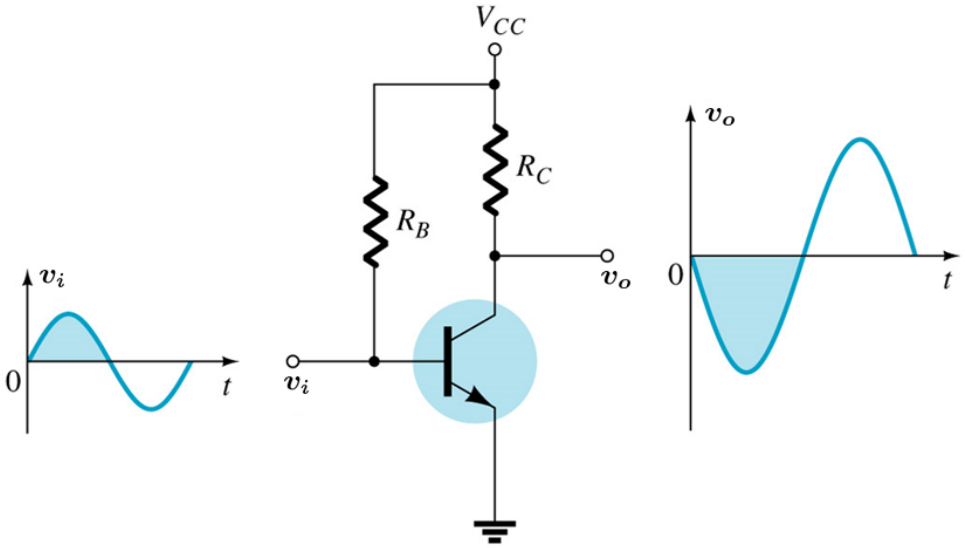



Figure 10.15: Demonstrating the 180° phase shift between input and output waveforms.

- The phase relationship between input and output is 180 degrees as shown in Figure 10.15 above.
- The negative sign used in the voltage gain formulas indicates the inversion.

## 10.4 Common-Emitter Voltage-Divider Bias Configuration

Common-emitter voltage-divider bias configuration is given in Figure 10.16 below

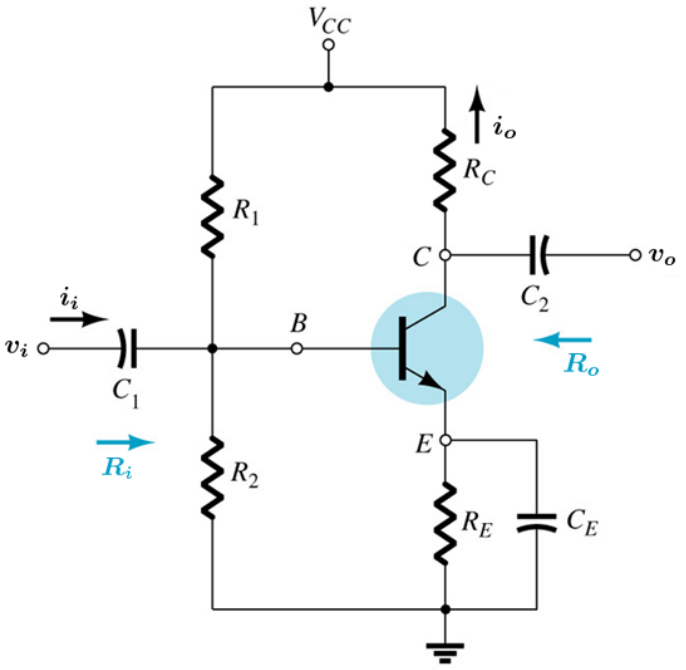



Figure 10.16: Common-emitter voltage-divider bias configuration.

Corresponding SSAC equivalent circuit is shown in Figure 10.17 below

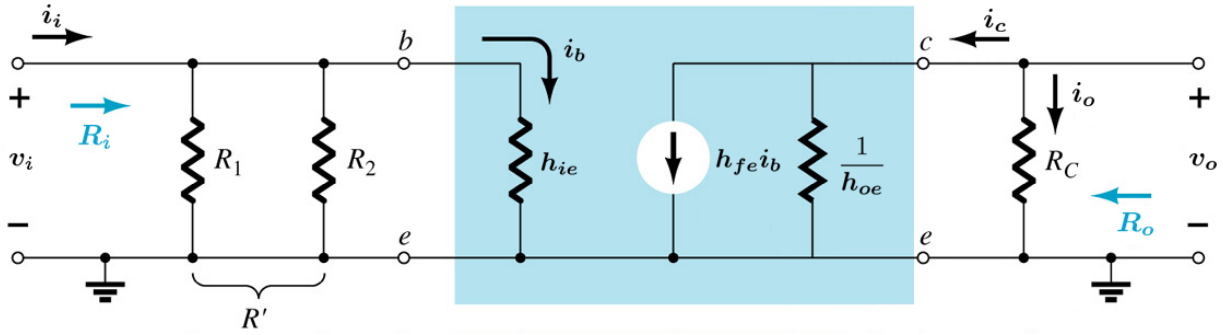



Figure 10.17: Small-signal equivalent circuit of the voltage-divider bias circuit in Figure 10.16.

### 10.4.1 Input Resistance

Input resistance $R_i$ is given as

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_1||R_2||h_{ie}} \tag{10.4.32}$$

- Input resistance $R_i$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_i = R_1||R_2||\beta r_e \tag{10.4.33}$$

### 10.4.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$\begin{aligned} A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} &= \left(\frac{v_o}{h_{fe} i_b}\right)\left(\frac{h_{fe} i_b}{i_b}\right)\left(\frac{i_b}{v_i}\right) \\ &= \left(-R_C || 1/h_{oe}\right)\left(h_{fe}\right)\left(\frac{1}{h_{ie}}\right) \\ &= -\frac{h_{fe}\left(R_C || 1/h_{oe}\right)}{h_{ie}} \end{aligned}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = -\frac{h_{fe}\left(R_C || 1/h_{oe}\right)}{h_{ie}}} \tag{10.4.34}$$

- No-load voltage gain $A_v$ according to the $\boldsymbol{r_e}$ **model** is given by

$$A_v = -\frac{R_C || r_o}{r_e} \tag{10.4.35}$$

- If $1/h_{oe} \geq 10R_C$, no-load voltage gain $A_v$ reduces to

$$A_v = -\frac{h_{fe} R_C}{h_{ie}} \qquad \ldots r_e \text{ model: } A_v = -\frac{R_C}{r_e} \tag{10.4.36}$$

- For the circuit in Figure 10.17, we can obtain the current gain $A_i$ as follows

$$\begin{aligned} A_i = \frac{i_o}{i_i} = \frac{v_o/R_C}{v_i/R_i} &= \frac{R_i}{R_C}\frac{v_o}{v_i} \\ &= \frac{R_i}{R_C} A_v \end{aligned} \tag{10.4.37}$$

- If $1/h_{oe} \geq 10$, and given $R' = R_1 || R_2$, current gain $A_i$ reduces to

$$A_i = -h_{fe}\frac{R'}{R' + h_{ie}} \qquad \ldots r_e \text{ model: } A_i = -\frac{R'}{R'/\beta + r_e} \tag{10.4.38}$$

### 10.4.3 Output Resistance

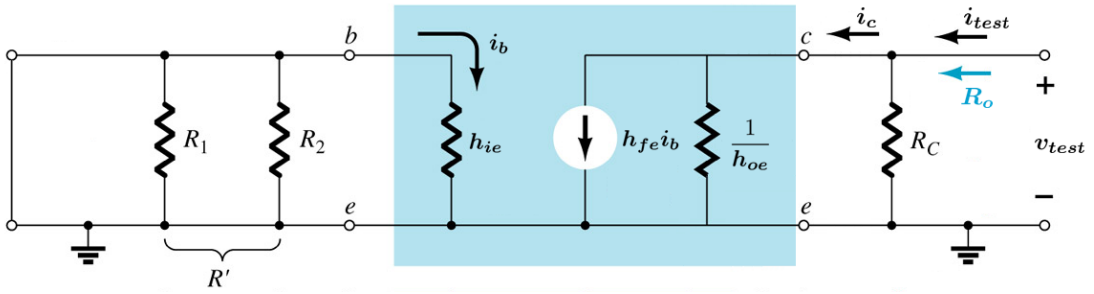



Figure 10.18: Test voltage circuit of Figure 10.17 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 10.18 above. Note that in the circuit $i_b = 0$, so $h_{fe} i_b = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_C || 1/h_{oe}} \tag{10.4.39}$$

- If $1/h_{oe} \geq 10R_C$, then $R_o$ simplifies to $R_o = R_C$.
- Output resistance $R_o$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_o = R_C || r_o \tag{10.4.40}$$

### 10.4.4 Phase Relationship

- Phase relationship between input and output of a common-emitter amplifier configuration if always 180 degrees. This is independent of the type of the bias-configuration.

## 10.5 Common-Emitter Unbypassed-Emitter Bias Configuration

Common-emitter unbypassed-emitter bias configuration is given in Figure 10.19 below

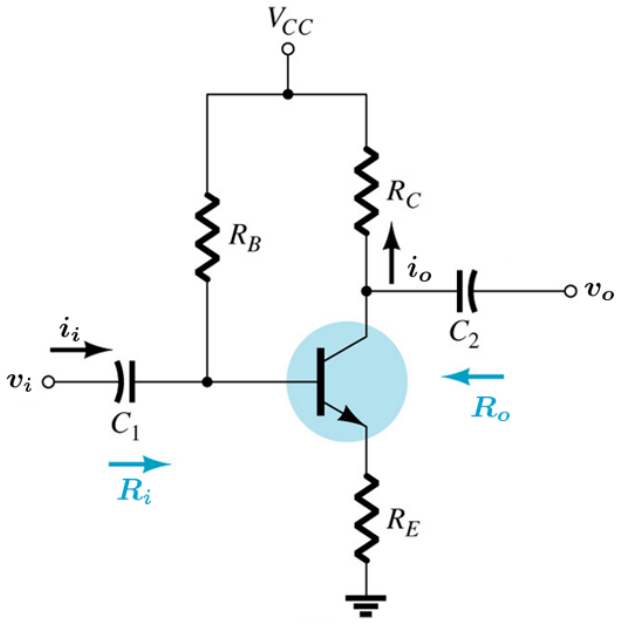



Figure 10.19: Common-emitter unbypassed-emitter bias configuration.

Corresponding SSAC equivalent circuit is shown in Figure 10.20 below

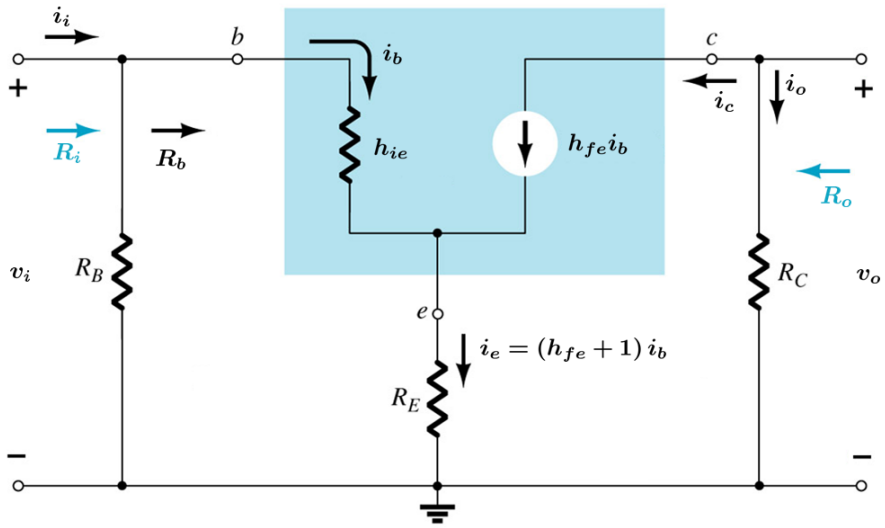



Figure 10.20: Small-signal equivalent circuit of the unbypassed-emitter bias circuit in Figure 10.19.

- When $R_E$ is not bypassed, we normally assume $1/h_{oe} = \infty$ in order to reduce the calculation complexity. Because of the feedback, even $1/h_{oe} \neq \infty$ the results do not really change at all.

### 10.5.1 Input Resistance

Input resistance $R_i$ is given as

$$R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_B || R_b \qquad \ldots R_b = h_{ie} + (h_{fe}+1)\,R_E$$
$$= R_B || \left[h_{ie} + (h_{fe}+1)\,R_E\right]$$

As a result, $R_i$ is given by

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_B || \left[h_{ie} + (h_{fe}+1)\,R_E\right]} \tag{10.5.41}$$

- Input resistance $R_i$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_i = R_B || \left(\beta+1\right)\left(r_e + R_E\right) \cong R_B || \beta\left(r_e + R_E\right) \tag{10.5.42}$$

### 10.5.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \left(\frac{v_o}{h_{fe}i_b}\right)\left(\frac{h_{fe}i_b}{i_b}\right)\left(\frac{i_b}{v_i}\right)$$
$$= \left(-R_C\right)\left(h_{fe}\right)\left(\frac{1}{R_b}\right)$$
$$= -\frac{h_{fe}R_C}{h_{ie} + (h_{fe}+1)\,R_E}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = -\frac{h_{fe}R_C}{h_{ie} + (h_{fe}+1)\,R_E}} \tag{10.5.43}$$

- No-load voltage gain $A_v$ according to the $\boldsymbol{r_e}$ **model** is given by

$$A_v = -\frac{R_C}{r_e + R_E} \tag{10.5.44}$$

- If $(h_{fe}+1)\,R_E \geq 10h_{ie}$, no-load voltage gain $A_v$ reduces to

$$A_v = -\frac{R_C}{R_E} \qquad \ldots r_e \text{ model: } A_v = -\frac{R_C}{R_E} \tag{10.5.45}$$

- For the circuit in Figure 10.20, we can obtain the current gain $A_i$ as follows

$$\begin{aligned} A_i = \frac{i_o}{i_i} &= \frac{v_o/R_C}{v_i/R_i} = \frac{R_i}{R_C}\frac{v_o}{v_i} \\ &= \frac{R_i}{R_C}A_v \end{aligned} \tag{10.5.46}$$

- Resultant current gain $A_i$ is given by

$$A_i = -h_{fe}\frac{R_B}{R_B + R_b} \qquad \ldots r_e \text{ model: } A_i = -\frac{R_B}{R_B/\beta + r_e + R_E} \tag{10.5.47}$$

### 10.5.3 Output Resistance

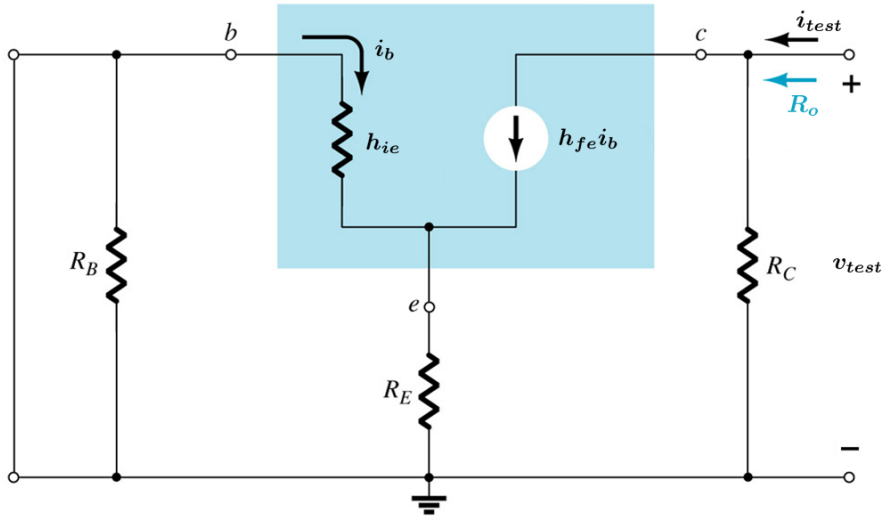



Figure 10.21: Test voltage circuit of Figure 10.20 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 10.21 above. Note that in the circuit $i_b = 0$, so $h_{fe}i_b = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_C} \tag{10.5.48}$$

- Output resistance $R_o$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_o = R_C \tag{10.5.49}$$

### 10.5.4 Phase Relationship

- Phase relationship between input and output of a common-emitter amplifier configuration if always 180 degrees. This is independent of the type of the bias-configuration.

## 10.6 Emitter-Follower Configuration

Emitter-follower (common-collector) configuration is given in Figure 10.22 below

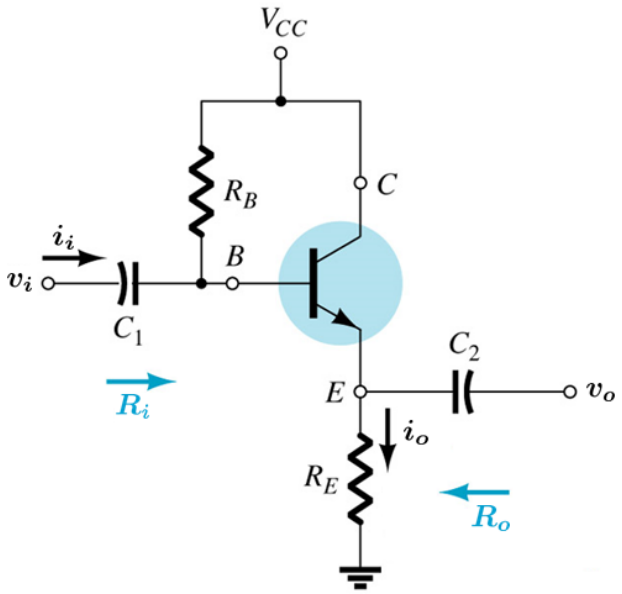



Figure 10.22: Emitter-follower configuration.

Corresponding SSAC equivalent circuit is shown in Figure 10.23 below

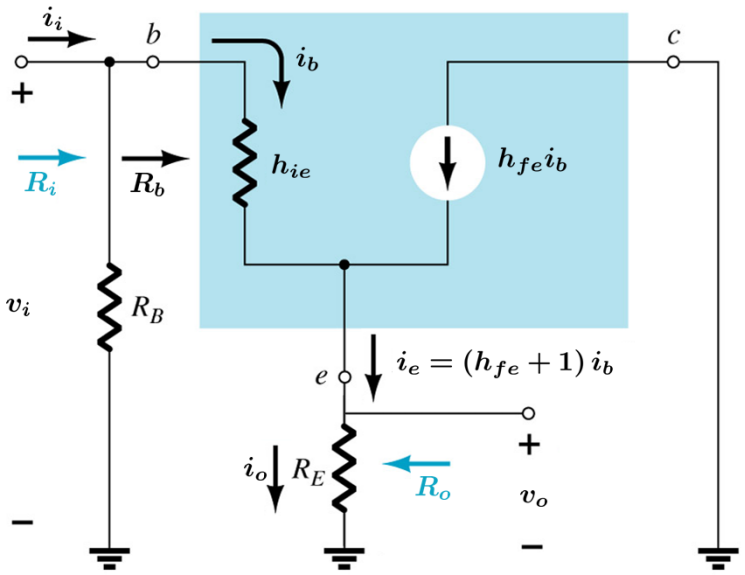



Figure 10.23: Small-signal equivalent circuit of the emitter-follower circuit in Figure 10.22.

- When $R_E$ is not bypassed, we normally assume $1/h_{oe} = \infty$ in order to reduce the calculation complexity.

### 10.6.1 Input Resistance

Input resistance $R_i$ is given as

$$R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_B||R_b \qquad \ldots R_b = h_{ie} + (h_{fe}+1)\,R_E$$
$$= R_B||\left[h_{ie} + (h_{fe}+1)\,R_E\right]$$

As a result, $R_i$ is given by

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_B||\left[h_{ie} + (h_{fe}+1)\,R_E\right]} \tag{10.6.50}$$

- Input resistance $R_i$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_i = R_B||\left(\beta+1\right)(r_e + R_E) \cong R_B||\beta\,(r_e + R_E) \tag{10.6.51}$$

### 10.6.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \left(\frac{v_o}{i_b}\right)\left(\frac{i_b}{v_i}\right)$$
$$= \left[(h_{fe}+1)\,R_E\right]\left(\frac{1}{R_b}\right) \qquad \ldots R_b = h_{ie} + (h_{fe}+1)\,R_E$$
$$= \frac{(h_{fe}+1)\,R_E}{h_{ie} + (h_{fe}+1)\,R_E} \cong 1$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \frac{(h_{fe}+1)\,R_E}{h_{ie}+(h_{fe}+1)\,R_E} \cong 1} \tag{10.6.52}$$

- No-load voltage gain $A_v$ according to the $\boldsymbol{r_e}$ **model** is given by

$$A_v = \frac{R_E}{r_e + R_E} \cong 1 \tag{10.6.53}$$

- For the circuit in Figure 10.23, we can obtain the current gain $A_i$ as follows

$$\begin{aligned} A_i = \frac{i_o}{i_i} &= \frac{v_o/R_E}{v_i/R_i} = \frac{R_i}{R_E}\frac{v_o}{v_i} \\ &= \frac{R_i}{R_E}A_v \end{aligned} \tag{10.6.54}$$

- Resultant current gain $A_i$ is given by,

$$A_i = (h_{fe}+1)\,\frac{R_B}{R_B + R_b} \qquad \ldots r_e \text{ model: } A_i = \frac{R_B}{R_B/(\beta+1) + r_e + R_E} \tag{10.6.55}$$

### 10.6.3 Output Resistance

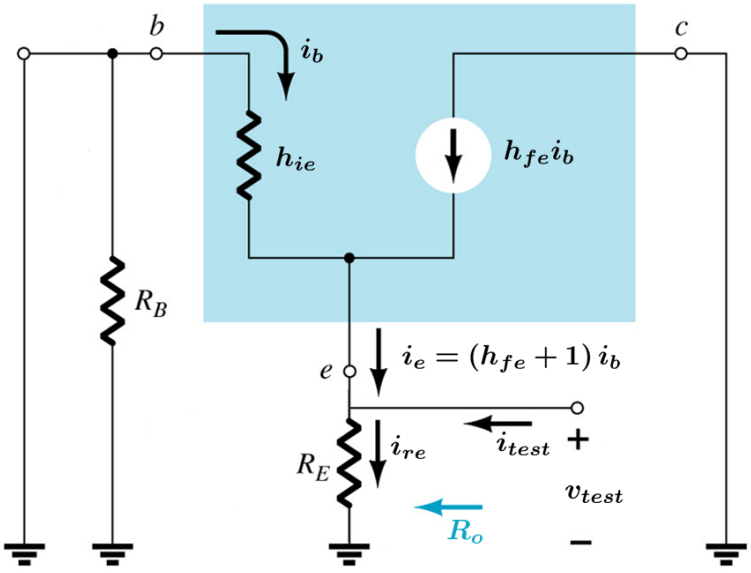



Figure 10.24: Test voltage circuit of Figure 10.23 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 10.24 above.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_E \| \frac{h_{ie}}{h_{fe}+1}} \tag{10.6.56}$$

- Output resistance $R_o$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_o = R_E||r_e \tag{10.6.57}$$

- If $1/h_{oe} \neq \infty$, then replace $R_E$ with $(R_E||1/h_{oe})$ in $R_i$, $A_v$ and $R_o$ calculations.
- If a voltage source with source resistance $R_s$ is connected to the input, replace $h_{ie}$ with $(h_{ie} + R_B||R_s)$ in $R_o$ calculations.

### 10.6.4 Phase Relationship

- Emitter-follower (common-collector) configuration has **no phase shift** between input and output.

## 10.7 Common-Emitter Collector Feedback Configuration

Common-emitter collector feedback bias configuration is given in Figure 10.25 below

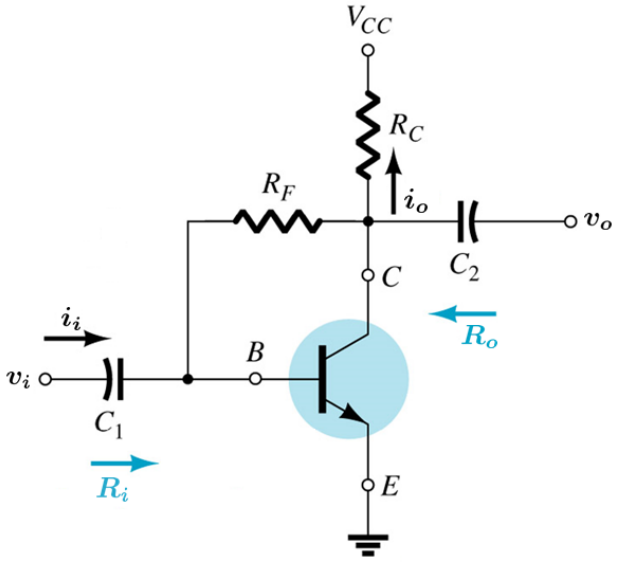



Figure 10.25: Common-emitter collector feedback bias configuration.

Corresponding SSAC equivalent circuit is shown in Figure 10.26 below

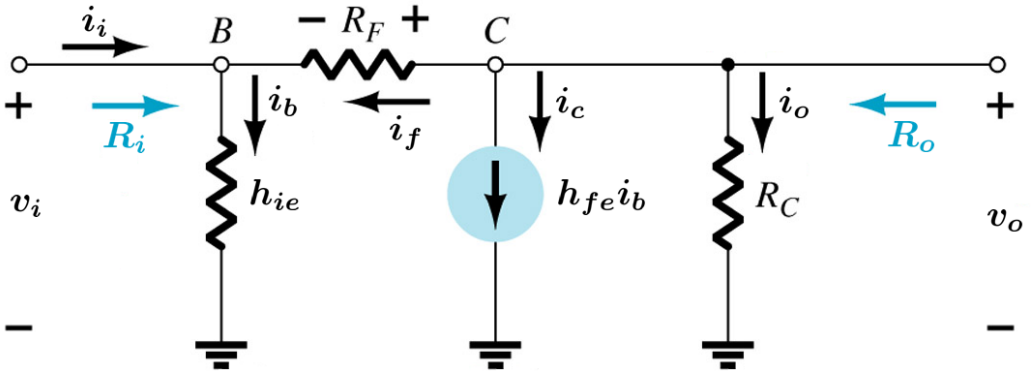



Figure 10.26: Small-signal equivalent circuit of the collector feedback bias circuit in Figure 10.25.

### 10.7.1 Input Resistance

Input resistance $R_i$ is given as

$$R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = \frac{h_{ie}}{1+\frac{h_{ie}+h_{fe}R_C}{R_F+R_C}} \qquad \ldots i_f = -\frac{h_{ie}+h_{fe}R_C}{R_F+R_C} i_b$$

$$\cong \frac{h_{ie}}{1+\frac{h_{fe}R_C}{R_F+R_C}} \qquad \ldots h_{fe}R_C \gg h_{ie}$$

As a result, $R_i$ is given by

$$\boxed{R_i = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} \cong \frac{h_{ie}}{1+\frac{h_{fe}R_C}{R_F+R_C}}} \tag{10.7.58}$$

- Input resistance $R_i$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_i \cong \frac{\beta r_e}{1+\frac{\beta R_C}{R_F+R_C}} \tag{10.7.59}$$

### 10.7.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \left(\frac{h_{fe}R_F - h_{ie}}{R_F+R_C}\right)\left(\frac{-R_C}{h_{ie}}\right) \qquad \ldots i_f = -\frac{h_{ie}+h_{fe}R_C}{R_F+R_C} i_b$$

$$\cong \left(\frac{h_{fe}R_F}{R_F+R_C}\right)\left(\frac{-R_C}{h_{ie}}\right) \qquad \ldots h_{fe}R_F \gg h_{ie}$$

$$\approx -\frac{h_{fe}R_C}{h_{ie}} \qquad \ldots R_F \gg R_C$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} \approx -\frac{h_{fe}R_C}{h_{ie}}} \tag{10.7.60}$$

- No-load voltage gain $A_v$ according to the $\boldsymbol{r_e}$ **model** is given by

$$A_v \approx -\frac{R_C}{r_e} \tag{10.7.61}$$

- For the circuit in Figure 10.26, we can obtain the current gain $A_i$ as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_C}{v_i/R_i} = \frac{R_i}{R_C}\frac{v_o}{v_i}$$

$$= \frac{R_i}{R_C}A_v \tag{10.7.62}$$

- Resultant current gain $A_i$ is given by,

$$A_i \cong -\frac{h_{fe}\left(R_F+R_C\right)}{R_F+\left(h_{fe}+1\right)R_C} \qquad \ldots r_e \text{ model: } A_i = -\frac{R_F+R_C}{R_F/\beta+R_C} \tag{10.7.63}$$

### 10.7.3 Output Resistance

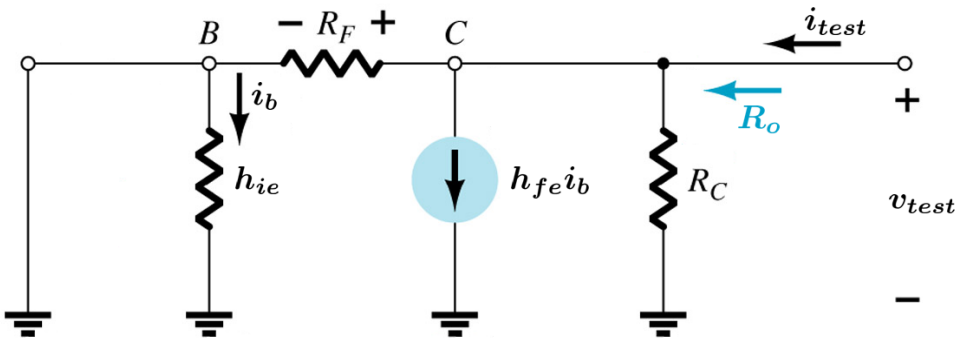



Figure 10.27: Test voltage circuit of Figure 10.26 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 10.27 above. Note that in the circuit $i_b = 0$, so $h_{fe}i_b = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_C||R_F} \tag{10.7.64}$$

- Output resistance $R_o$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_o = R_C||R_F \tag{10.7.65}$$

- If $1/h_{oe} \neq \infty$, then replace $R_C$ with $(R_C||1/h_{oe})$ in $R_i$, $A_v$ and $R_o$ calculations.
- If a voltage source with source resistance $R_s$ is connected to the input, replace $R_F$ with $[R_F\,(R_s + h_{ie})\,/\,(h_{fe}R_s + h_{ie})]$ in $R_o$ calculations.

### 10.7.4 Phase Relationship

- Phase relationship between input and output of a common-emitter amplifier configuration if always 180 degrees. This is independent of the type of the bias-configuration.

## 10.8 Common-Base Configuration

Common-base configuration is given in Figure 10.28 below

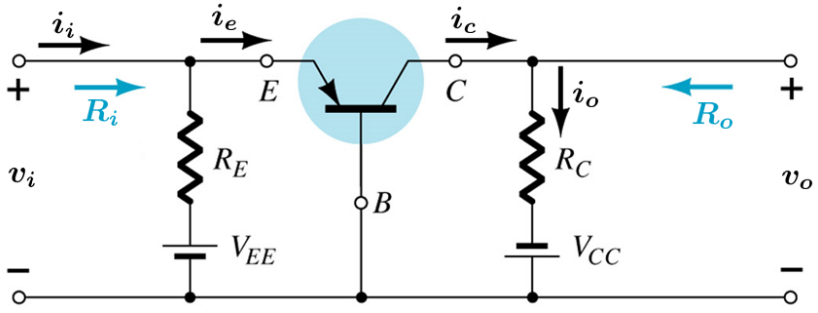



Figure 10.28: Common-base configuration.

Corresponding SSAC equivalent circuit is shown in Figure 10.29 below

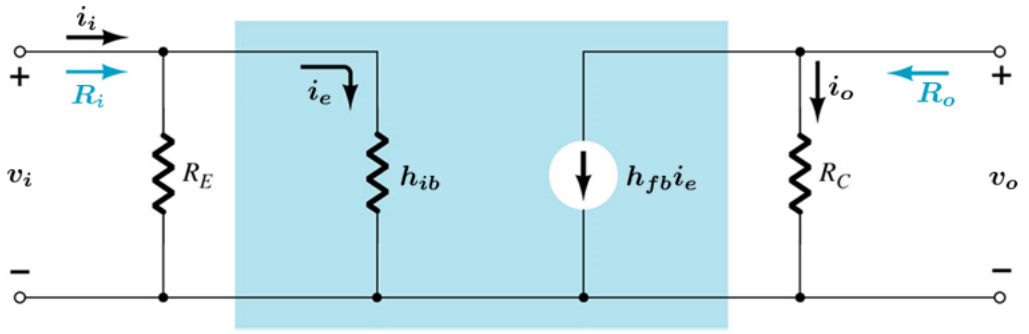



Figure 10.29: Small-signal equivalent circuit of the common-base circuit in Figure 10.28.

- Here, $h_{ib} = \dfrac{h_{ie}}{h_{fe}+1} = \dfrac{26\,\text{mV}}{I_{EQ}}$ and $h_{fb} = -\alpha_{ac} = -1$.

### 10.8.1 Input Resistance

Input resistance $R_i$ is given as

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_E||h_{ib}} \tag{10.8.66}$$

- If $R_E \geq 10h_{ib}$, then $R_i$ simplifies to $R_i = h_{ib}$.
- Input resistance $R_i$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_i = R_E||r_e \tag{10.8.67}$$

### 10.8.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$\begin{aligned} A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} &= \left(\frac{v_o}{h_{fb}i_e}\right)\left(\frac{h_{fb}i_e}{i_e}\right)\left(\frac{i_e}{v_i}\right) \\ &= (-R_C)\,(h_{fb})\left(\frac{1}{h_{ib}}\right) \\ &= \frac{R_C}{h_{ib}} \qquad \ldots h_{fb} = -1 \end{aligned}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \frac{R_C}{h_{ib}}} \tag{10.8.68}$$

- No-load voltage gain $A_v$ according to the $\boldsymbol{r_e}$ **model** is given by

$$A_v = \frac{R_C}{r_e} \tag{10.8.69}$$

- For the circuit in Figure 10.29, we can obtain the current gain $A_i$ as follows

$$A_i = \frac{i_o}{i_i} = \frac{v_o/R_C}{v_i/R_i} = \frac{R_i}{R_C}\frac{v_o}{v_i} = \frac{R_i}{R_C}A_v \tag{10.8.70}$$

- Resultant current gain $A_i$ is given by,

$$A_i = \frac{R_E||h_{ib}}{h_{ib}} \approx 1 \qquad \ldots r_e \text{ model: } A_i = \frac{R_E||r_e}{r_e} \approx 1 \tag{10.8.71}$$

### 10.8.3 Output Resistance

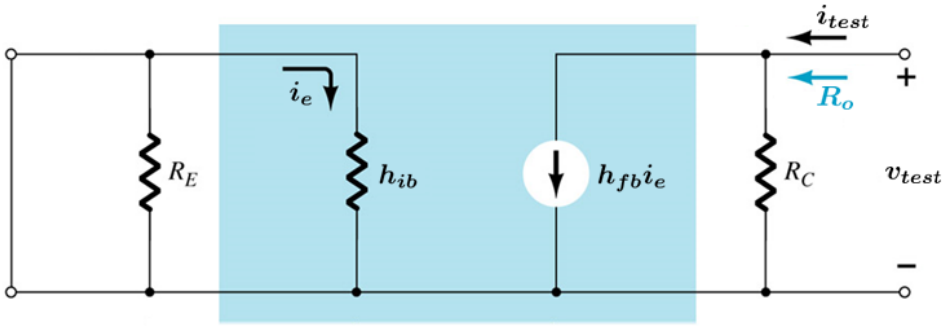



Figure 10.30: Test voltage circuit of Figure 10.29 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 10.30 above. Note that in the circuit $i_e = 0$, so $h_{fb}i_e = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_C} \tag{10.8.72}$$

- Output resistance $R_o$ according to the $\boldsymbol{r_e}$ **model** is given by

$$R_o = R_C \tag{10.8.73}$$

- If $1/h_{ob} \neq \infty$, then replace $R_C$ with $(R_C||1/h_{ob})$ in $R_i$, $A_v$ and $R_o$ calculations.

### 10.8.4 Phase Relationship

- A common-base amplifier configuration has **no phase shift** between input and output

**Example 10.1:** Consider the common-base BJT amplifier in the figure below.

a) Perform DC analysis and find the $Q$-point.

b) Evaluate the overall voltage gain $A_{Vs}$ and the current gain $A_i$.

c) Sketch $v_o$ on the AC+DC load line graph when

i. $v_s = 100\sin(\omega t)$ mV,

ii. $v_s = 900\sin(\omega t)$ mV.

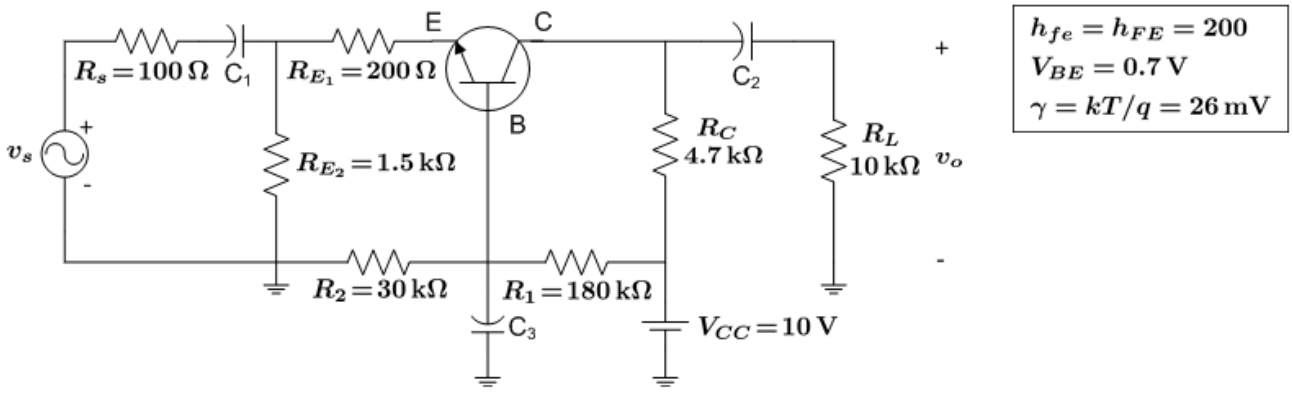



Figure 10.31: BJT amplifier circuit for Example 10.1.

**Solution:** a) Let us first draw the DC equivalent circuit first as shown in Figure 10.32 below,

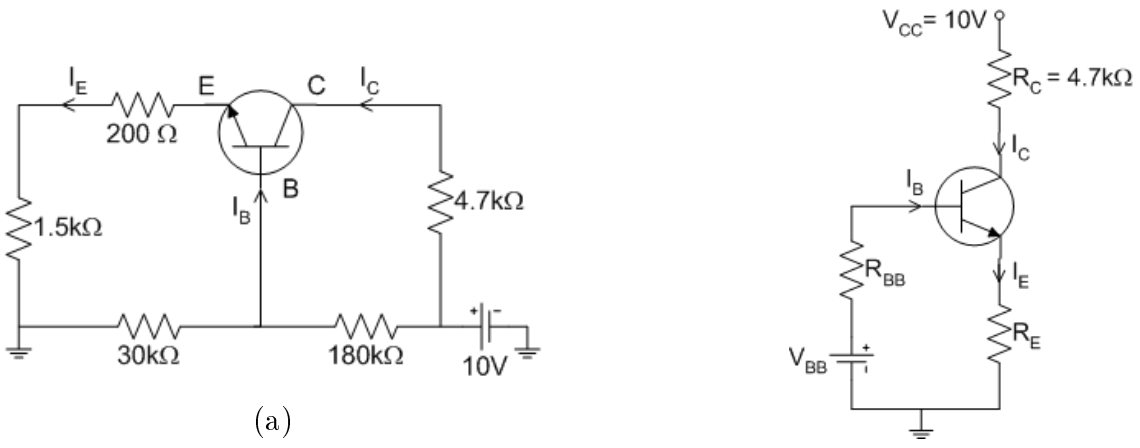



Figure 10.32: DC equivalent circuit of Figure 10.31: (a) as it is (b) Thévenin applied.

Here, $R_E = R_{E_1} + R_{E_2} = 0.2k + 1.5k = 1.7\,\text{k}\Omega$.

Now, let us calculate $V_{BB}$, $R_{BB}$, $I_{CQ}$, $V_{CEQ}$ and $V_{CBQ}$

$$\begin{aligned}
V_{BB} &= \left(\frac{30k}{30k+180k}\right)(10) = 1.43\,\text{V},\\
R_{BB} &= 30k||180k = 25.71\,\text{k}\Omega,\\
I_{CQ} \cong I_{EQ} &= \frac{1.43-0.7}{25.71k/201+1.7k} = 0.4\,\text{mA},\\
V_{CEQ} &= 10-(0.4m)(4.7k+1.7k) = 7.44\,\text{V},\\
V_{CBQ} &= 7.44-0.7 = 6.74\,\text{V}.
\end{aligned}$$

b) In order to calculate the voltage gain, we need to draw the common-base SSAC equivalent circuit. As it is not given $1/h_{ob} = \infty$. Let us now calculate $h_{ib}$ as

$$h_{ib} = \frac{26m}{0.4m} = 65\,\Omega.$$

So, the small-signal equivalent circuit is given in Figure 10.32 below

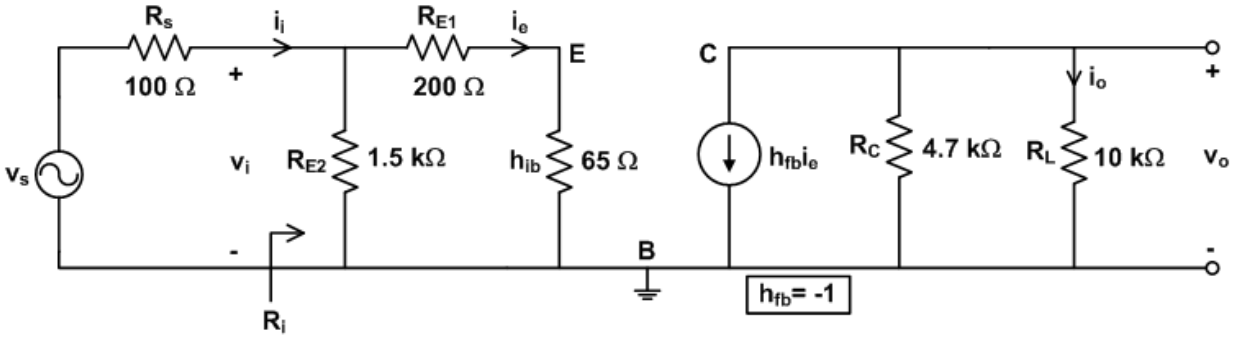



Figure 10.33: Small-signal equivalent circuit of Figure 10.31.

Now, let us calculate input resistance $R_i$ and voltage gain with load $A_V$ as follows

$$\begin{aligned}
R_i &= R_{E_2}||\left(R_{E1}+h_{ib}\right) = 1.5k||(200+65) \cong 225\,\Omega\\
A_V &= \frac{v_o}{v_i} = \left(\frac{v_o}{h_{fb}i_e}\right)\left(\frac{h_{fb}i_e}{i_e}\right)\left(\frac{i_e}{v_i}\right)\\
&= \left(-R_C||R_L\right)\left(h_{fb}\right)\left(\frac{1}{R_{E_1}+h_{ib}}\right) = \frac{R_C||R_L}{R_{E_1}+h_{ib}}\\
&= \frac{4.7k||10k}{200+65} = \frac{3.2k}{0.265k} = 12.08.
\end{aligned}$$

Thus, overall voltage gain $A_{Vs}$ and current gain $A_i$ are given by

$$\begin{aligned}
A_{Vs} = \frac{v_o}{v_s} &= \left(\frac{v_o}{v_i}\right)\left(\frac{v_i}{v_s}\right) = A_V\,\frac{R_i}{R_s+R_i} = (12.08)\left(\frac{225}{100+225}\right)\\
&= 8.36,\\
A_i = \frac{i_o}{i_i} &= \frac{v_o/R_L}{v_i/R_i} = A_V\,\frac{R_i}{R_L} = (12.08)\left(\frac{0.225k}{10k}\right)\\
&= 0.27.
\end{aligned}$$

c) Let us write down the AC load line equation for this common-base amplifier, noting that $v_o = v_{cb} = -i_c(R_C||R_L) = -i_c R_{ac}$ and $v_{cb} = v_{ce} - v_{be} = v_{ce} - \frac{h_{ib}}{R_{E_1}+h_{ib}} v_i \approx v_{ce}$)

$$\begin{aligned} v_{CB} &= -i_C R_{ac} + V_{CBQ} + I_{CQ} R_{ac} && \ldots V_{CBQ} = V_{CEQ} - V_{BEQ} \\ v_{CE} - V_{BEQ} &= -i_C R_{ac} + V_{CEQ} - V_{BEQ} + I_{CQ} R_{ac} && \ldots v_{CB} \approx v_{CE} - V_{BEQ} \\ v_{CE} &= -i_C R_{ac} + V_{CEQ} + I_{CQ} R_{ac} \end{aligned}$$

So, we calculate $R_{ac}$ from the C-B loop and $R_{DC}$ from the C-E loop as follows

$$\begin{aligned} R_{ac} &= R_C||R_L = 4.7k||10k = 3.2\,\text{k}\Omega, \\ R_{DC} &= R_C + R_E = 4.7k + 1.7k = 6.4\,\text{k}\Omega. \end{aligned}$$

Note that, maximum available undistorted swing amplitude is

$$\min\left(V_{CEQ}, I_{CQ} R_{ac}\right) = \min(7.44, (0.4m)(3.2k)) = \min(7.44, 1.28) = 1.28\,\text{V}.$$

Thus, as $A_{Vs} = 8.36$, maximum input source amplitude which gives an undistorted output is

$$\max(v_{s(p)}) = 1.28/8.36 = 153.1\,\text{mV}.$$

If the input source amplitude exceeds this value, we will observe distortion at the output.

i. For $v_s = 100\sin(\omega t)$ mV, we are going to observe an undistorted sinusoidal output with an amplitude of 0.836 V around $V_{CBQ} = 6.74$ V as shown in Figure 10.34 below.

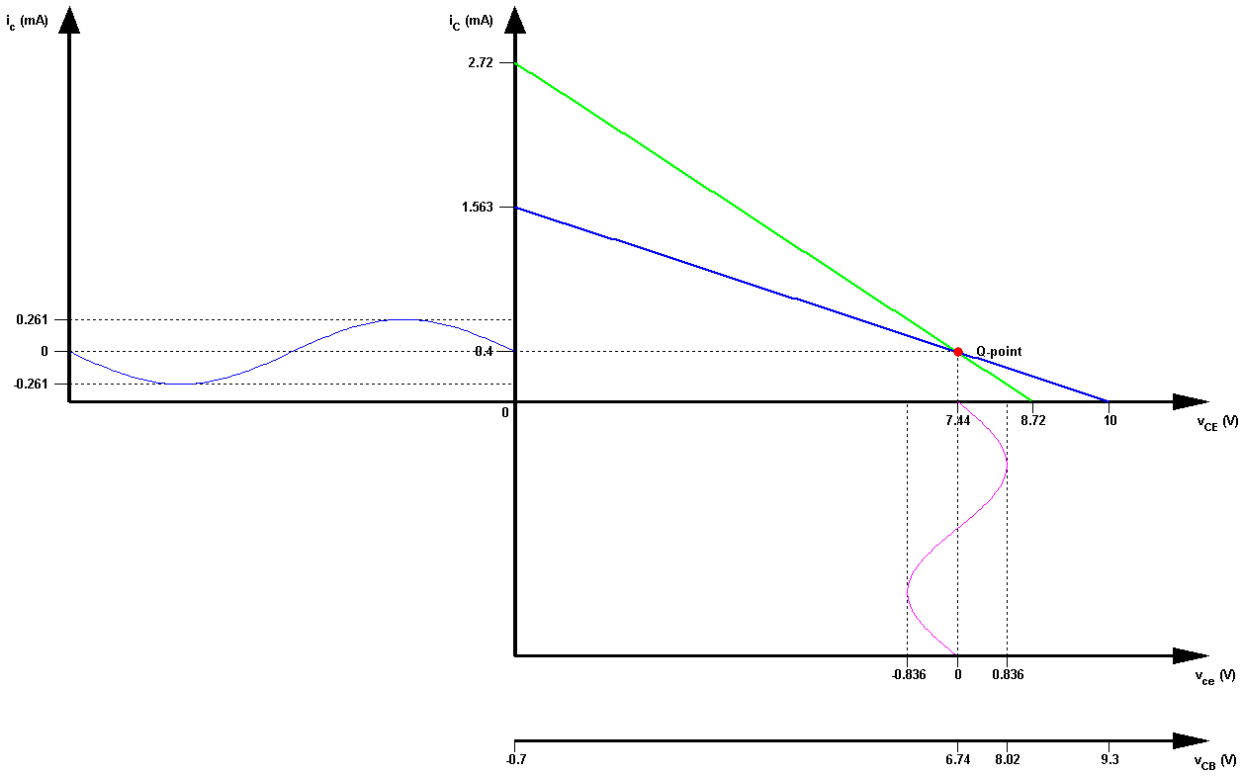



Figure 10.34: AC-DC load-lines for Example 10.1with input $v_s = 100\sin(\omega t)$ mV.

ii. For $v_s = 900\sin(\omega t)$ mV, we are going to observe a distorted output as shown in Figure 10.35 below.

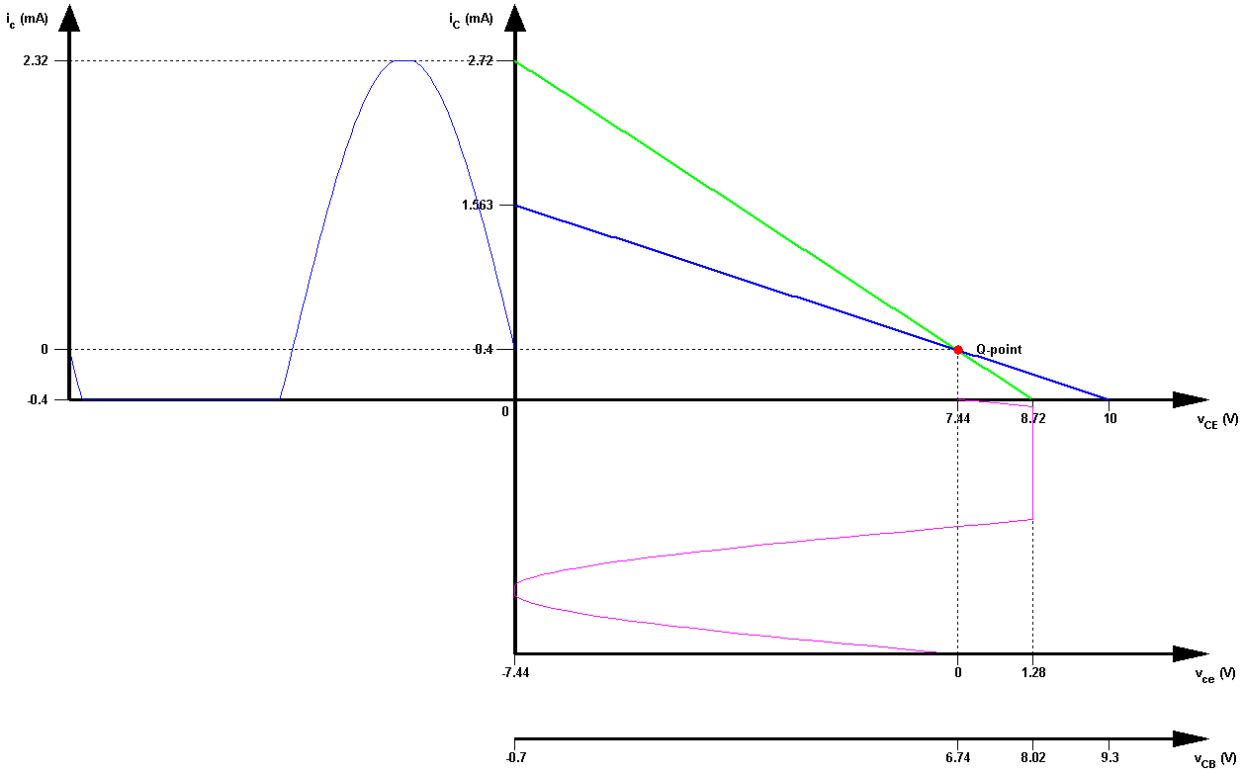



Figure 10.35: AC-DC load-lines for Example 10.1with input $v_s = 900\sin(\omega t)$ mV.

# Chapter 11

# FET Small-Signal Analysis

### 11.0.1 FET SSAC Analysis Steps

1. Draw the SSAC equivalent circuit
   a) Draw the AC equivalent circuit (signal frequency is infinity, i.e., $f = \infty$)
      i. Capacitors are short circuit, i.e., $X_C \to 0$.
      ii. Kill the DC power sources (i.e., AC value of DC sources is zero).
   b) Replace FET with its small-signal equivalent model.
2. Calculate the three amplifier parameters: $R_i$, $R_o$ and $A_v$
   a) Calculate no-load input resistance, $R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty}$.
   b) Calculate output resistance, $R_o$.
   c) Calculate no-load voltage gain, $A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$.

## 11.1 FET Small-Signal Model

Small-signal equivalent model for a FET transistor is provided in Figure 11.1 below. This model and its analysis is the same for all FET types, i.e., JFET, DMOSFET, EMOSFET, $n$-channel and $p$-channel.

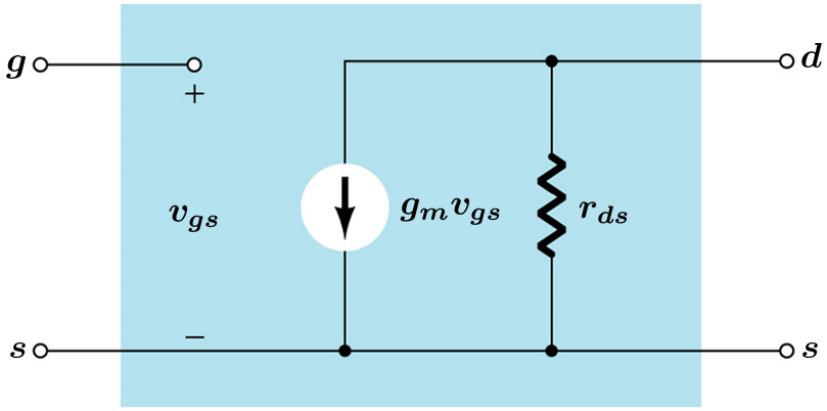



Figure 11.1: FET small-signal equivalent circuit.

Here,

- $g_m = g_{fs} = y_{fs} = \left.\dfrac{\partial I_D}{\partial V_{GS}}\right|_{Q\text{-point}}$ is the forward transfer conductance,
- $r_{ds} = \dfrac{1}{g_{os}} = \dfrac{1}{y_{os}} = \left.\dfrac{\partial V_{DS}}{\partial I_D}\right|_{Q\text{-point}}$ is the output resistance.

Forward transfer conductance $g_m$ is mostly called as the **transconductance** parameter.

When $r_{ds} \neq \infty$, we can also use the voltage-controlled voltage source model (via Norton-to-Thévenin transformation, a.k.a source transformation) as shown in Figure 11.2 below. We mostly use this model for the common-gate and unbypassed self-bias configurations.

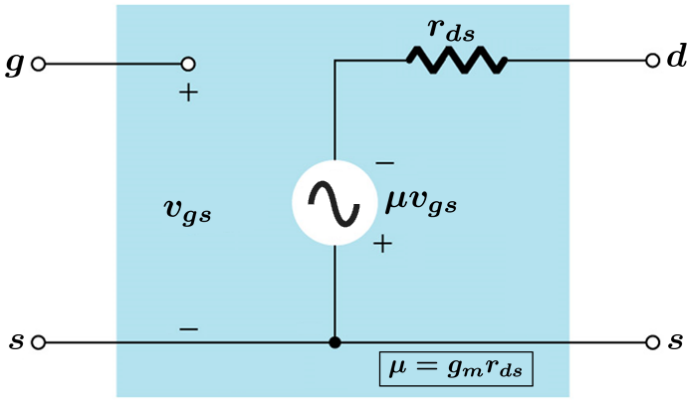



Figure 11.2: FET small-signal equivalent circuit with the voltage-controlled voltage source.

Here $\mu = g_m r_{ds}$ is the forward transfer-voltage gain.

- Typical values of $g_m$ run from 1 mS to 5 mS,
- Typical values of $r_{ds}$ run from 20 kΩ to 100 kΩ,
- Consequently, typical values of $\mu$ run from 20 to 500.

#### 11.1.0.1 Transconductance Parameter ($g_m$)

Transconductance parameter $g_m$ is given by

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{Q\text{-point}} \cong \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{Q\text{-point}} \tag{11.1.1}$$

In other words, $g_m$ is the slope of the characteristics at the point of operation as shown in Figure 11.3 below.

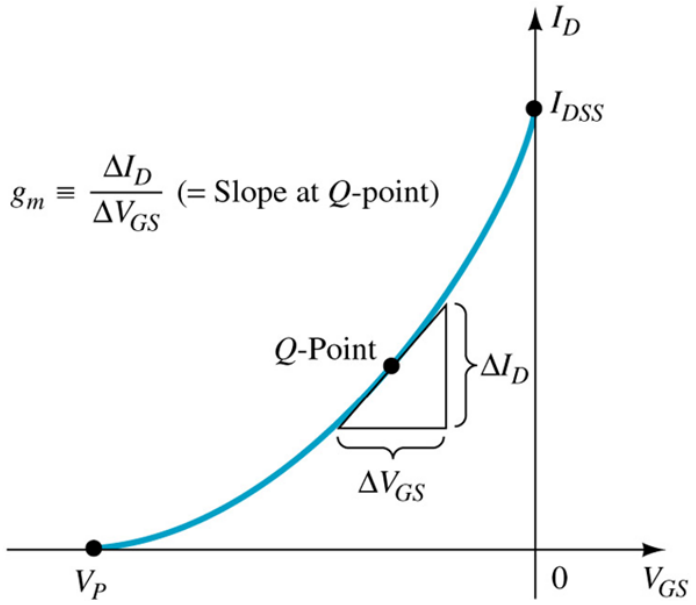



Figure 11.3: Graphical definition of the transconductance $g_m$.

- Let us derive $g_m$ for the JFET equation, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$$\begin{aligned} g_m &= \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{Q\text{-point}} = \left.\frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)\right|_{Q\text{-point}} \\ &= \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GSQ}}{V_P}\right) \qquad (11.1.2) \\ &= \frac{2I_{DSS}}{|V_P|}\sqrt{\frac{I_{DQ}}{I_{DSS}}} \qquad \ldots I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2 \\ &= g_{m0}\sqrt{\frac{I_{DQ}}{I_{DSS}}} \qquad \ldots g_{m0} = \frac{2I_{DSS}}{|V_P|} \qquad (11.1.3) \end{aligned}$$

- Let us derive $g_m$ for the MOSFET equation, $I_D = k\left(V_{GS} - V_{GS(Th)}\right)^2$

$$\begin{aligned} g_m &= \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{Q\text{-point}} = 2k\left(V_{GS} - V_{GS(Th)}\right)\big|_{Q\text{-point}} \\ &= 2k\left(V_{GSQ} - V_{GS(Th)}\right) \qquad (11.1.4) \\ &= 2\sqrt{k}\sqrt{I_{DQ}} \qquad \ldots I_{DQ} = k\left(V_{GS} - V_{GS(Th)}\right)^2 \qquad (11.1.5) \end{aligned}$$

#### 11.1.0.2 Phase Relationship

The phase relationship between input and output depends on the amplifier configuration circuit as listed below.

- Common-Source: 180 degrees
- Common-Gate: 0 degrees
- Common-Drain: 0 degrees (Source-Follower)

## 11.2 Common-Source Fixed-Bias Configuration

Common-source fixed-bias configuration is given in Figure 11.4 below

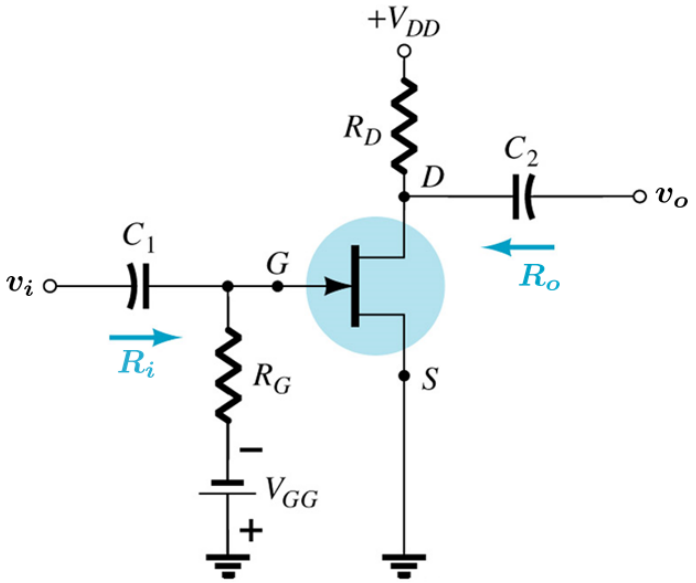



Figure 11.4: Common-source fixed-bias configuration.

Corresponding SSAC equivalent circuit is shown in Figure 11.5 below

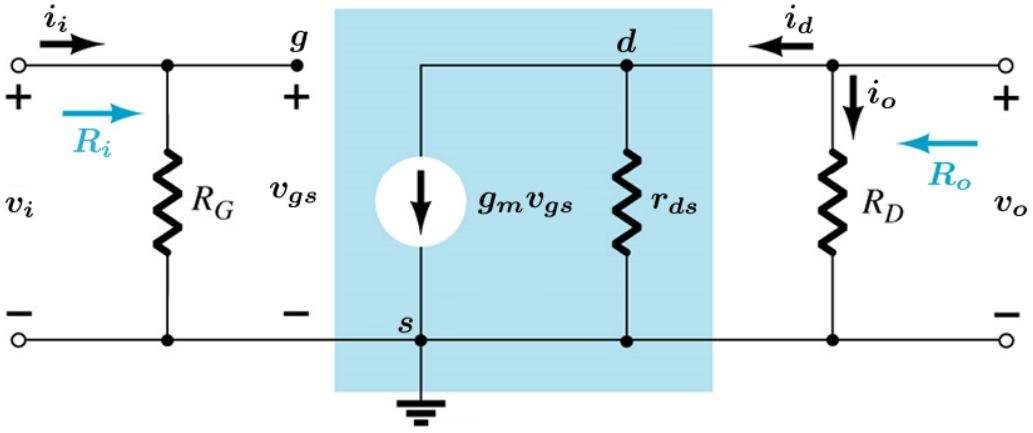



Figure 11.5: Small-signal equivalent circuit of the fixed-bias circuit in Figure 11.4.

### 11.2.1 Input Resistance

Input resistance $R_i$ is given as

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_G} \tag{11.2.6}$$

### 11.2.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$\begin{aligned} A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} &= \left(\frac{v_o}{g_m v_{gs}}\right)\left(\frac{g_m v_{gs}}{v_{gs}}\right)\left(\frac{v_{gs}}{v_i}\right) \\ &= \left(-R_D||r_{ds}\right)\left(g_m\right)\left(1\right) \\ &= -g_m\left(R_D||r_{ds}\right) \end{aligned}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = -g_m\left(R_D||r_{ds}\right)} \tag{11.2.7}$$

- If $r_{ds} \geq 10R_D$, voltage gain $A_v$ reduces to

$$A_v = -g_m R_D \tag{11.2.8}$$

- For the circuit in Figure 11.5, we can obtain the current gain $A_i$ as follows

$$\begin{aligned} A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} &= \frac{R_i}{R_D}\frac{v_o}{v_i} \\ &= \frac{R_i}{R_D}A_v \end{aligned} \tag{11.2.9}$$

- If $r_{ds} \geq 10R_D$, current gain $A_i$ reduces to

$$A_i = -g_m R_G \tag{11.2.10}$$

### 11.2.3 Output Resistance

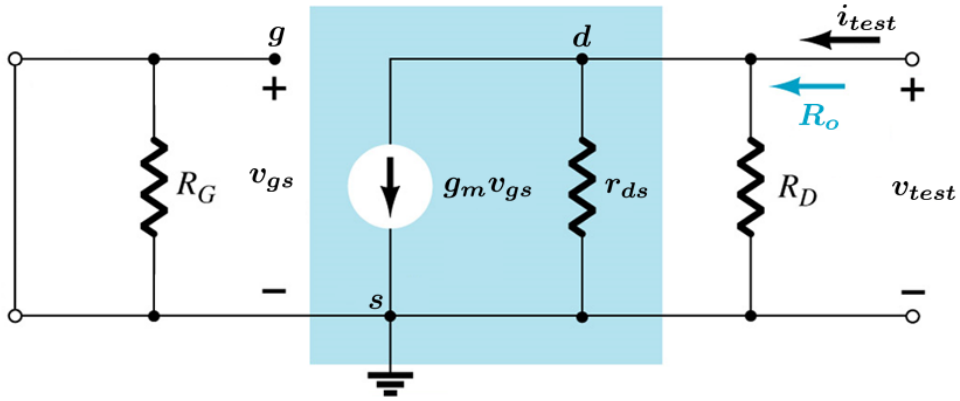



Figure 11.6: Test voltage circuit of Figure 11.5 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 11.6 above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_D || r_{ds}} \tag{11.2.11}$$

- If $r_{ds} \geq 10R_D$, then $R_o$ simplifies to $R_o = R_D$.

## 11.3 Common-Source Self-Bias Configuration

Common-source self-bias configuration is given in Figure 11.7 below

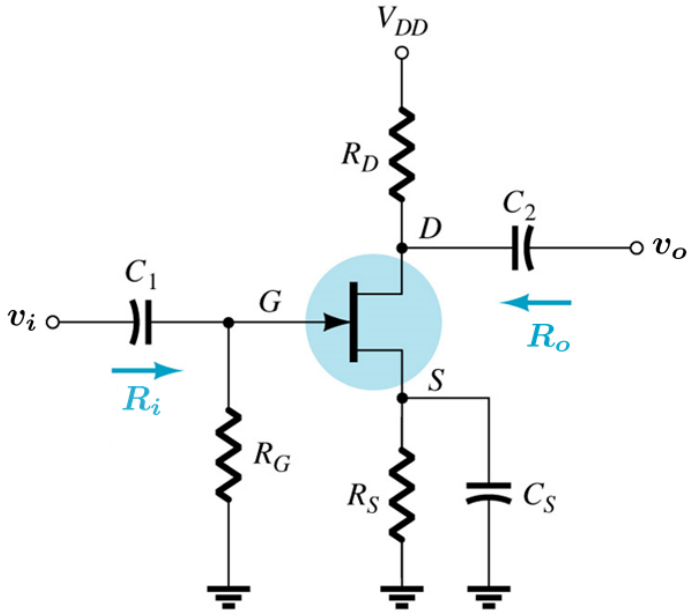



Figure 11.7: Common-source self-bias configuration.

Corresponding SSAC equivalent circuit is shown in Figure 11.8 below

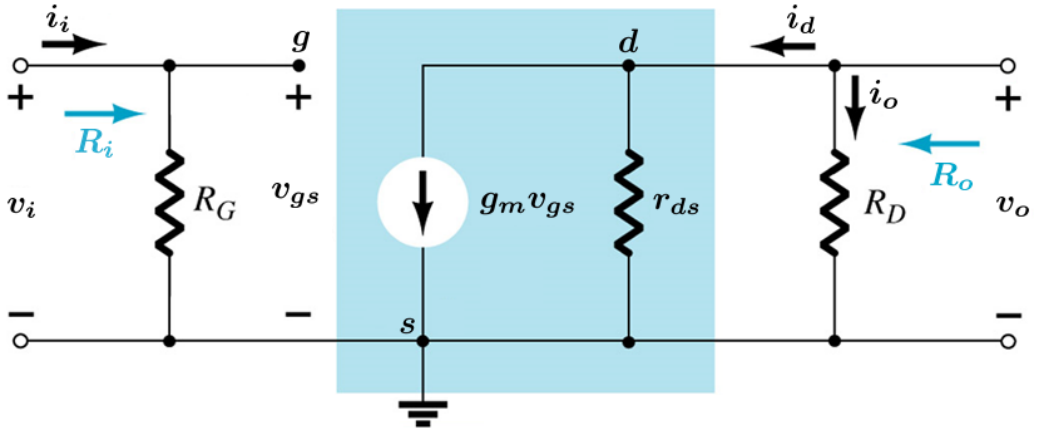



Figure 11.8: Small-signal equivalent circuit of the self-bias circuit in Figure 11.7.

### 11.3.1 Input Resistance

Input resistance $R_i$ is given as

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_G} \tag{11.3.12}$$

### 11.3.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$\begin{aligned} A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} &= \left(\frac{v_o}{g_m v_{gs}}\right)\left(\frac{g_m v_{gs}}{v_{gs}}\right)\left(\frac{v_{gs}}{v_i}\right) \\ &= \left(-R_D||r_{ds}\right)\left(g_m\right)\left(1\right) \\ &= -g_m\left(R_D||r_{ds}\right) \end{aligned}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = -g_m\left(R_D||r_{ds}\right)} \tag{11.3.13}$$

- If $r_{ds} \geq 10R_D$, no-load voltage gain $A_v$ reduces to

$$A_v = -g_m R_D \tag{11.3.14}$$

- For the circuit in Figure 11.8, we can obtain the current gain $A_i$ as follows

$$\begin{aligned} A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} &= \frac{R_i}{R_D}\frac{v_o}{v_i} \\ &= \frac{R_i}{R_D}A_v \end{aligned} \tag{11.3.15}$$

- If $r_{ds} \geq 10R_D$, current gain $A_i$ reduces to

$$A_i = -g_m R_G \tag{11.3.16}$$

### 11.3.3 Output Resistance

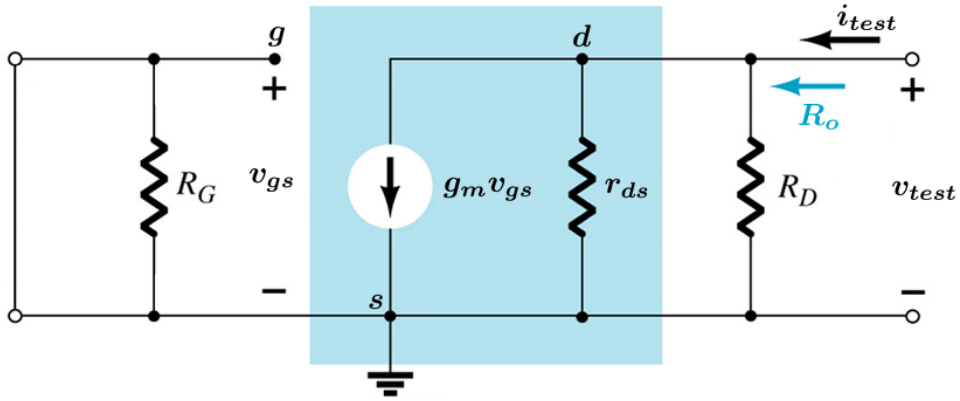



Figure 11.9: Test voltage circuit of Figure 11.8 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 11.9 above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_D || r_{ds}} \tag{11.3.17}$$

- If $r_{ds} \geq 10R_D$, then $R_o$ simplifies to $R_o = R_D$.

## 11.4 Common-Source Voltage-Divider Bias Configuration

Common-source voltage-divider bias configuration is given in Figure 11.10 below

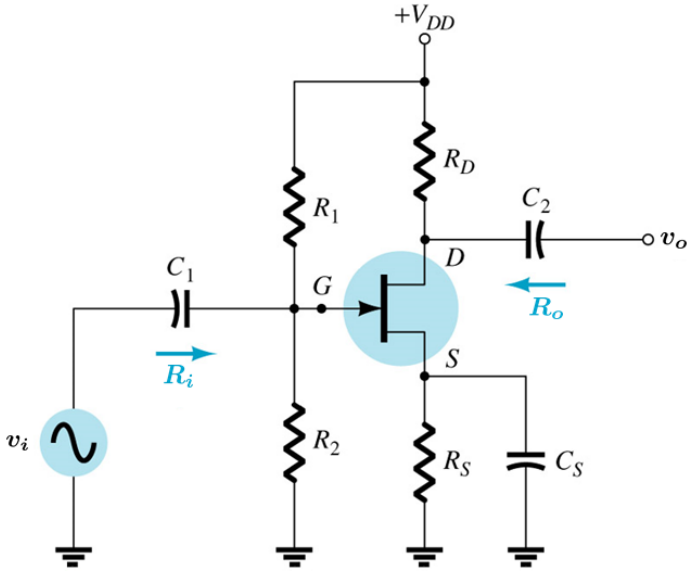



Figure 11.10: Common-source voltage-divider bias configuration.

Corresponding SSAC equivalent circuit is shown in Figure 11.11 below

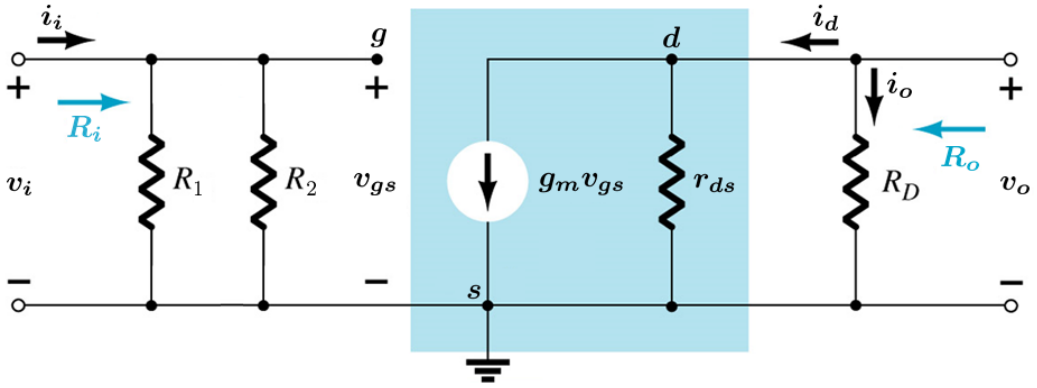



Figure 11.11: Small-signal equivalent circuit of the voltage-divider bias circuit in Figure 11.10.

### 11.4.1 Input Resistance

Input resistance $R_i$ is given as

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_1||R_2} \tag{11.4.18}$$

### 11.4.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$\begin{aligned} A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} &= \left(\frac{v_o}{g_m v_{gs}}\right)\left(\frac{g_m v_{gs}}{v_{gs}}\right)\left(\frac{v_{gs}}{v_i}\right) \\ &= \left(-R_D||r_{ds}\right)\left(g_m\right)\left(1\right) \\ &= -g_m\left(R_D||r_{ds}\right) \end{aligned}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = -g_m\left(R_D||r_{ds}\right)} \tag{11.4.19}$$

- If $r_{ds} \geq 10R_D$, no-load voltage gain $A_v$ reduces to

$$A_v = -g_m R_D \tag{11.4.20}$$

- For the circuit in Figure 11.11, we can obtain the current gain $A_i$ as follows

$$\begin{aligned} A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} &= \frac{R_i}{R_D}\frac{v_o}{v_i} \\ &= \frac{R_i}{R_D}A_v \end{aligned} \tag{11.4.21}$$

- If $r_{ds} \geq 10R_D$, current gain $A_i$ reduces to

$$A_i = -g_m\left(R_1||R_2\right) \tag{11.4.22}$$

### 11.4.3 Output Resistance

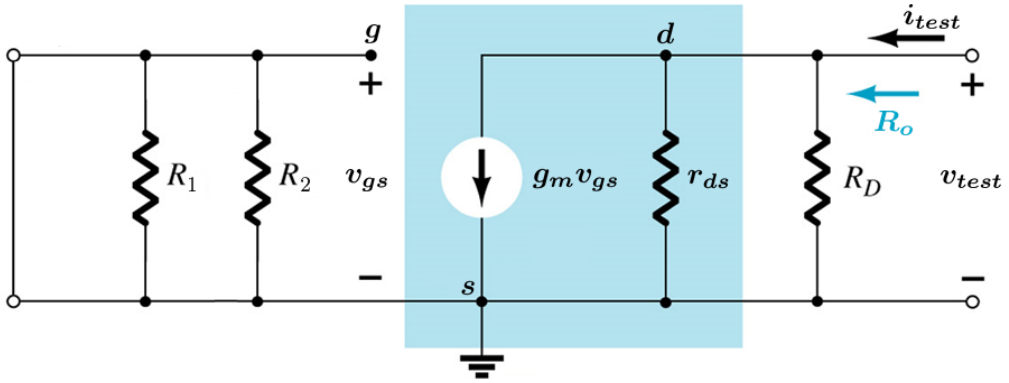



Figure 11.12: Test voltage circuit of Figure 11.11 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 11.12 above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_D || r_{ds}} \tag{11.4.23}$$

- If $r_{ds} \geq 10R_D$, then $R_o$ simplifies to $R_o = R_D$.

## 11.5 Common-Source Unbypassed Self-Bias Configuration

Common-source unbypassed self-bias (unbypassed $R_S$) configuration is given in Figure 11.13 below

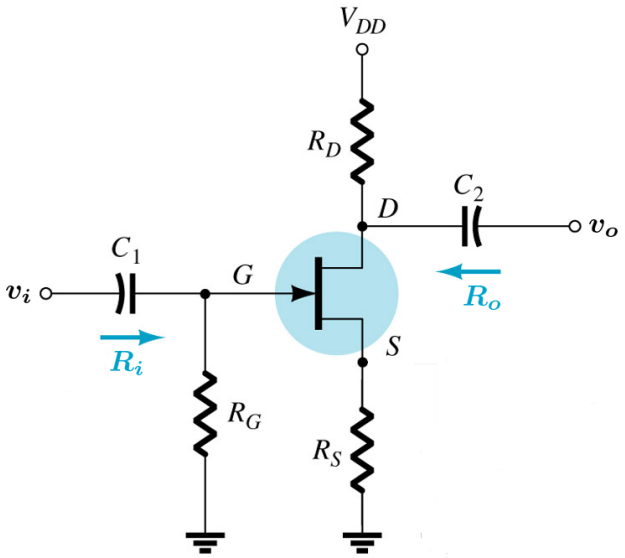



Figure 11.13: Common-source unbypassed self-bias configuration.

Corresponding SSAC equivalent circuit is shown in Figure 11.14 below

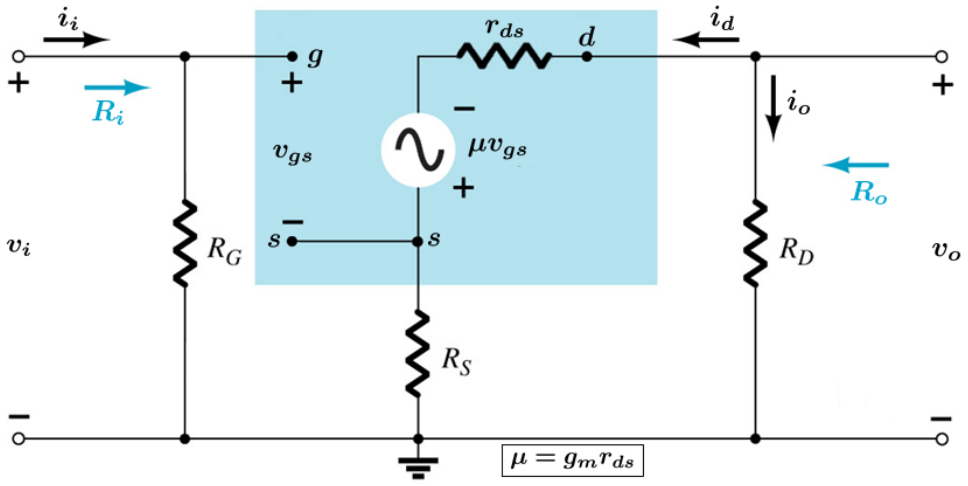



Figure 11.14: Small-signal equivalent circuit of the unbypassed self-bias circuit in Figure 11.13.

- When $R_S$ is not bypassed, we normally use the voltage-controlled voltage source model in the small-signal equivalent circuit as shown in Figure 11.14 above.

### 11.5.1 Input Resistance

Input resistance $R_i$ is given as

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_G} \tag{11.5.24}$$

### 11.5.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$\begin{aligned}
A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} &= \left(\frac{v_o}{i_d}\right)\left(\frac{i_d}{v_{gs}}\right)\left(\frac{v_{gs}}{v_i}\right) \\
&= (-R_D)\left(\frac{\mu}{R_S+R_D+r_{ds}}\right)\left(\frac{v_{gs}}{v_{gs}+i_d R_S}\right) && \ldots i_d = \frac{\mu v_{gs}}{R_S+R_D+r_{ds}} \\
&= (-R_D)\left(\frac{\mu}{R_S+R_D+r_{ds}}\right)\left(\frac{1}{1+\frac{\mu R_S}{R_S+R_D+r_{ds}}}\right) \\
&= -\frac{\mu R_D}{(\mu+1)R_S+R_D+r_{ds}} && \ldots \mu = g_m r_{ds} \\
&= -\frac{g_m R_D}{1+g_m R_S+\frac{R_S+R_D}{r_{ds}}}
\end{aligned}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = -\frac{g_m R_D}{1+g_m R_S+\dfrac{R_S+R_D}{r_{ds}}}} \tag{11.5.25}$$

- If $r_{ds} \geq 10\,(R_D+R_S)$, no-load voltage gain $A_v$ reduces to

$$A_v = -\frac{g_m R_D}{1+g_m R_S} \tag{11.5.26}$$

- If $r_{ds} \geq 10\,(R_D+R_S)$ and $g_m R_S \gg 1$, no-load voltage gain $A_v$ reduces to

$$A_v \approx -\frac{R_D}{R_S} \tag{11.5.27}$$

- For the circuit in Figure 11.14, we can obtain the current gain $A_i$ as follows

$$\begin{aligned}
A_i = \frac{i_o}{i_i} &= \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D}\frac{v_o}{v_i} \\
&= \frac{R_i}{R_D}A_v
\end{aligned} \tag{11.5.28}$$

### 11.5.3 Output Resistance

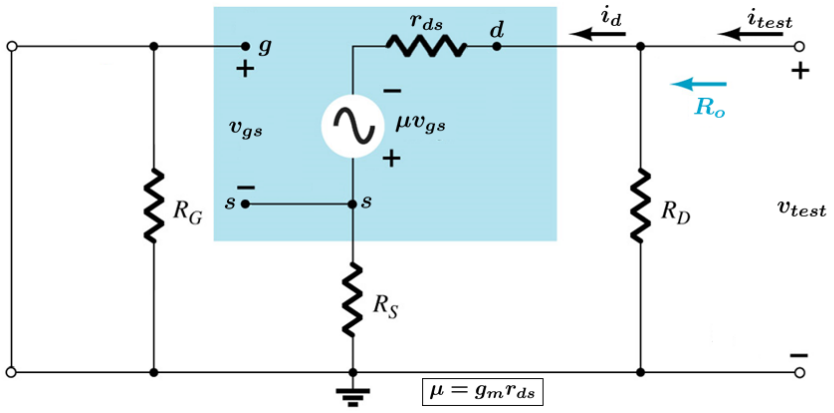



Figure 11.15: Test voltage circuit of Figure 11.14 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 11.15 above.

$$
\begin{aligned}
R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} &= \frac{v_{test}}{\frac{v_{test}}{R_D} + i_d} && \ldots i_{test} = i_{R_D} + i_d \\
&= \frac{v_{test}}{\frac{v_{test}}{R_D} - \frac{v_{gs}}{R_S}} && \ldots v_s = -v_{gs}, i_d = \frac{-v_{gs}}{R_S} \\
&= \frac{v_{test}}{\frac{v_{test}}{R_D} + \frac{v_{test}}{(\mu+1)R_S + r_{ds}}} && \ldots v_{gs} = -\frac{v_{test}}{(\mu+1) + r_{ds}/R_S} \\
&= R_D || \left[(\mu+1) R_S + r_{ds}\right] && \ldots \mu = g_m r_{ds} \\
&= R_D || \left[(g_m R_S + 1) r_{ds} + R_S\right] \\
&\cong R_D
\end{aligned}
$$

As a result, $R_o$ is given by

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} \cong R_D} \tag{11.5.29}$$

## 11.6 Source-Follower Configuration

Source-follower (common-drain) configuration is given in Figure 11.16 below

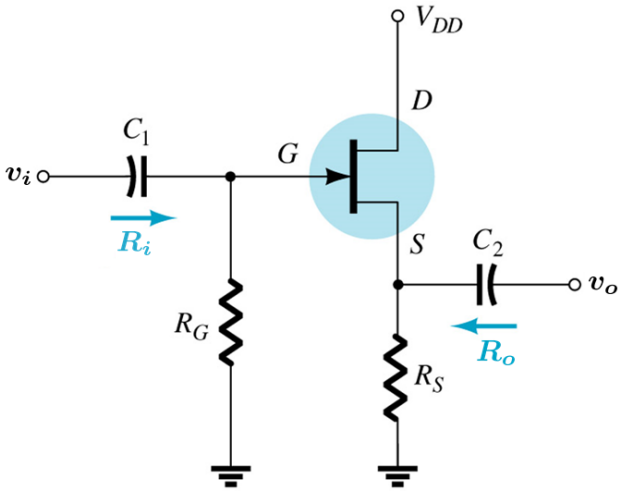



Figure 11.16: Source-follower configuration.

Corresponding SSAC equivalent circuit is shown in Figure 11.17 below

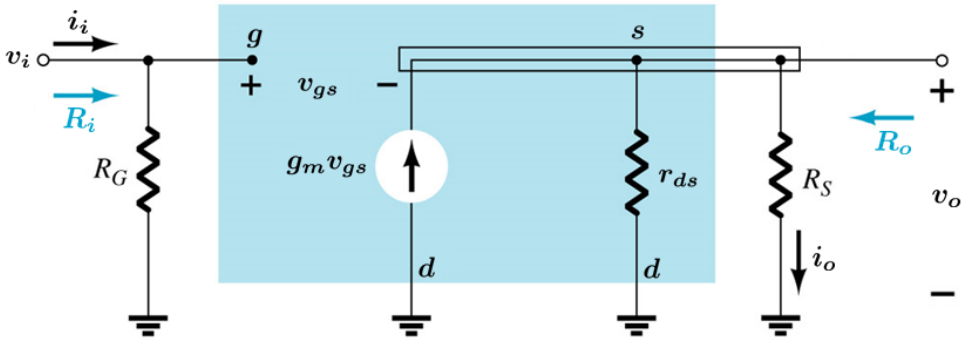



Figure 11.17: Small-signal equivalent circuit of the source-follower circuit in Figure 11.16.

### 11.6.1 Input Resistance

Input resistance $R_i$ is given as

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R_G} \tag{11.6.30}$$

### 11.6.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$\begin{aligned} A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} &= \left(\frac{v_o}{v_{gs}}\right)\left(\frac{v_{gs}}{v_i}\right) \\ &= \left[g_m\left(R_S||r_{ds}\right)\right]\left(\frac{1}{1+g_m\left(R_S||r_{ds}\right)}\right) \qquad \ldots v_i = v_{gs} + v_o \\ &= \frac{g_m\left(R_S||r_{ds}\right)}{1+g_m\left(R_S||r_{ds}\right)} \\ &\cong 1 \end{aligned}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = \frac{g_m\,(R_S||r_{ds})}{1+g_m\,(R_S||r_{ds})} \cong 1} \tag{11.6.31}$$

- For the circuit in Figure 11.17, we can obtain the current-gain $A_i$ as follows

$$\begin{aligned} A_i = \frac{i_o}{i_i} &= \frac{v_o/R_S}{v_i/R_i} = \frac{R_i}{R_S}\frac{v_o}{v_i} \\ &= \frac{R_i}{R_S}A_v \end{aligned} \tag{11.6.32}$$

### 11.6.3 Output Resistance

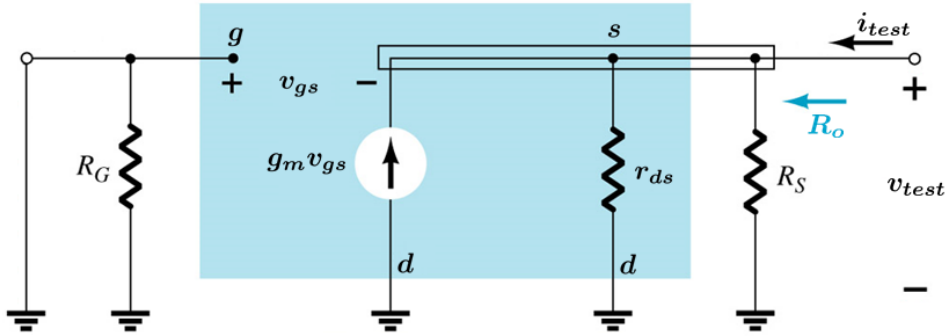



Figure 11.18: Test voltage circuit of Figure 11.17 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 11.18 above.

$$\begin{aligned} R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0,R_L=v_{test}} &= \frac{v_{test}}{\frac{v_{test}}{R_S||r_{ds}} - g_m v_{gs}} && \dots i_{test} = i_{R_S||r_{ds}} - g_m v_{gs} \\ &= \frac{v_{test}}{\frac{v_{test}}{R_S||r_{ds}} + g_m v_{test}} && \dots v_{test} = -v_{gs} \\ &= \frac{v_{test}}{\frac{v_{test}}{R_S||r_{ds}} + \frac{v_{test}}{1/g_m}} \\ &= R_S||r_{ds}||\frac{1}{g_m} \end{aligned}$$

As a result, $R_o$ is given by

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0,R_L=v_{test}} = R_S||r_{ds}||\frac{1}{g_m}} \tag{11.6.33}$$

- If $(R_S||r_{ds}) \geq 10/g_m$, output resistance $R_o$ reduces to

$$R_o \cong \frac{1}{g_m} \tag{11.6.34}$$

## 11.7 Common-Source Drain Feedback Configuration

Common-source drain feedback bias configuration is given in Figure 11.19 below

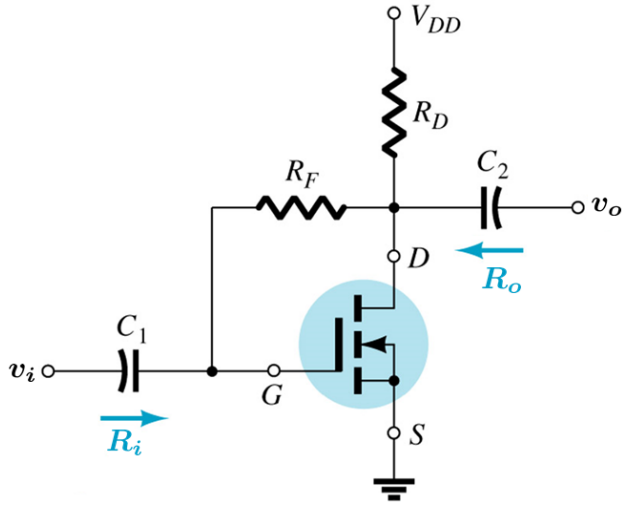



Figure 11.19: Common-source drain feedback bias configuration.

Corresponding SSAC equivalent circuit is shown in Figure 11.20 below

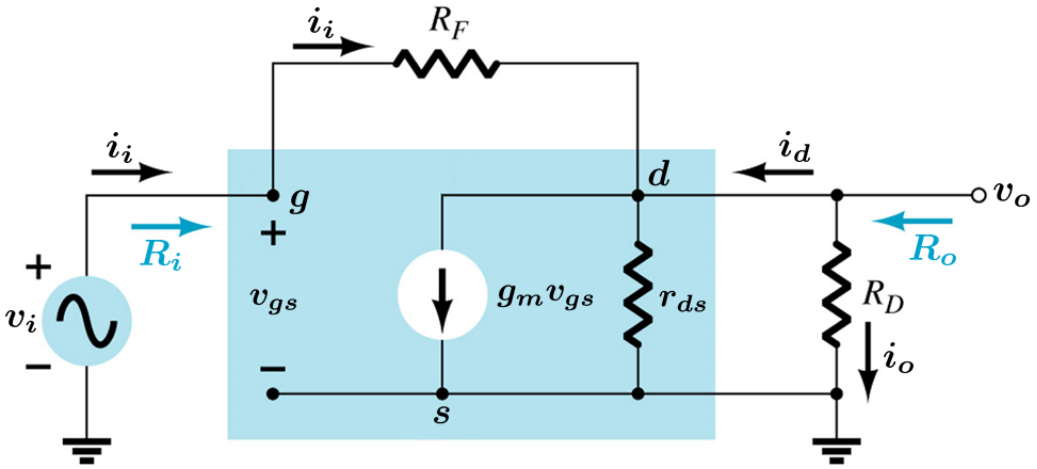



Figure 11.20: Small-signal equivalent circuit of the drain feedback bias circuit in Figure 11.19.

### 11.7.1 Input Resistance

Input resistance $R_i$ is given as

$$
\begin{aligned}
R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} &= \frac{v_{gs}}{g_m v_{gs} + v_o/\left(R_D||r_{ds}\right)} && \ldots v_i = v_{gs} \\
&= \frac{R_F + R_D||r_{ds}}{1 + g_m\left(R_D||r_{ds}\right)} && \ldots v_o = \frac{\left(1 - g_m R_F\right)\left(R_D||r_{ds}\right) v_{gs}}{R_F + R_D||r_{ds}} \\
&\cong \frac{R_F}{1 + g_m\left(R_D||r_{ds}\right)} && \ldots R_F \gg R_D||r_{ds}
\end{aligned}
$$

As a result, $R_i$ is given by

$$\boxed{R_i = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} \cong \frac{R_F}{1 + g_m\left(R_D||r_{ds}\right)}} \tag{11.7.35}$$

### 11.7.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$\begin{aligned} A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} &= \frac{\left(1 - g_m R_F\right)\left(R_D||r_{ds}\right)}{R_F + R_D||r_{ds}} && \ldots v_i = v_{gs} \\ &\cong -g_m\left(R_D||r_{ds}||R_F\right) && \ldots g_m R_F \gg 1 \end{aligned}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} \cong -g_m\left(R_D||r_{ds}||R_F\right)} \tag{11.7.36}$$

- For the circuit in Figure 11.20, we can obtain the current-gain $A_i$ as follows

$$\begin{aligned} A_i = \frac{i_o}{i_i} &= \frac{v_o/R_D}{v_i/R_i} = \frac{R_i}{R_D}\frac{v_o}{v_i} \\ &= \frac{R_i}{R_D}A_v \end{aligned} \tag{11.7.37}$$

### 11.7.3 Output Resistance

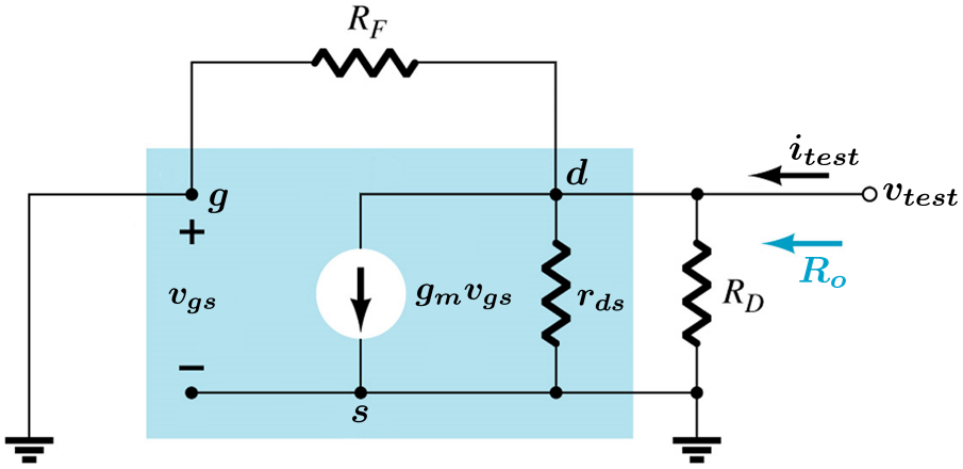



Figure 11.21: Test voltage circuit of Figure 11.20 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 11.21 above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_D||r_{ds}||R_F} \tag{11.7.38}$$

- If a voltage source with source resistance $R_s$ is connected to the input, replace $R_F$ with $\left[\left(R_F + R_s\right)/\left(1 + g_m R_s\right)\right]$ in $R_o$ calculations.

## 11.8 Common-Gate Configuration

Common-gate configuration is given in Figure 11.22 below

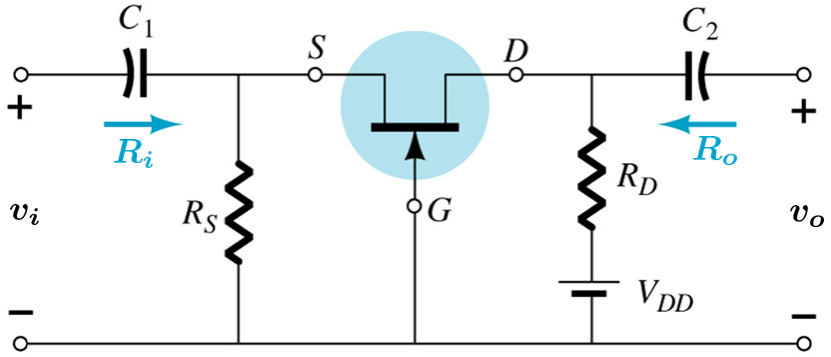



Figure 11.22: Common-gate configuration.

Corresponding SSAC equivalent circuit is shown in Figure 11.23 below

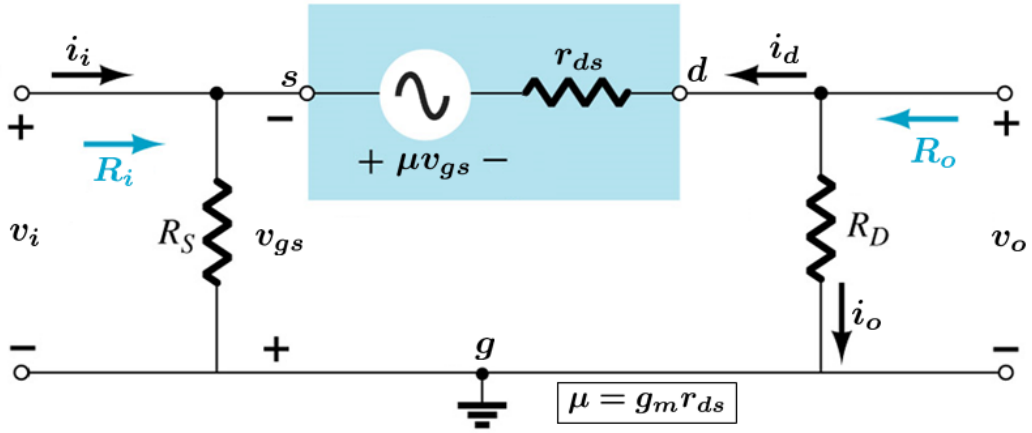



Figure 11.23: Small-signal equivalent circuit of the common-gate circuit in Figure 11.22.

### 11.8.1 Input Resistance

Input resistance $R_i$ is given as

$$
\begin{aligned}
R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} &= \frac{v_i}{v_i/R_S - i_d} && \dots v_i = -v_{gs} \\
&= \frac{v_i}{v_i/R_S + v_i/\left(\frac{R_D+r_{ds}}{\mu+1}\right)} && \dots i_d = \frac{(\mu+1)\,v_{gs}}{R_D + r_{ds}} \\
&= R_S || \frac{R_D + r_{ds}}{1 + g_m r_{ds}} && \dots \mu = g_m r_{ds} \\
&\cong R_S || \frac{1}{g_m} && \dots r_{ds} \geq 10 R_D \text{ and } g_m r_{ds} \gg 1
\end{aligned}
$$

As a result, $R_i$ is given by

$$
\boxed{R_i = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} \cong R_S || \frac{1}{g_m}} \tag{11.8.39}
$$

### 11.8.2 Voltage Gain

No-load voltage gain $A_v$ is given by

$$\begin{aligned} A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} &= \frac{-i_d R_D}{-v_{gs}} && \dots v_i = -v_{gs} \\ &= \frac{(\mu+1)\,R_D}{R_D + r_{ds}} && \dots i_d = \frac{(\mu+1)\,v_{gs}}{R_D + r_{ds}} \\ &= \frac{(g_m r_{ds}+1)\,R_D}{R_D + r_{ds}} && \dots \mu = g_m r_{ds} \\ &\cong g_m R_D && \dots r_{ds} \geq 10R_D \text{ and } g_m r_{ds} \gg 1 \end{aligned} \tag{11.8.40}$$

As a result, $A_v$ is given by

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} \cong g_m R_D} \tag{11.8.41}$$

- For the circuit in Figure 11.23, we can obtain the current-gain $A_i$ as follows

$$\begin{aligned} A_i = \frac{i_o}{i_i} = \frac{v_o/R_D}{v_i/R_i} &= \frac{R_i}{R_D}\frac{v_o}{v_i} \\ &= \frac{R_i}{R_D} A_v \end{aligned} \tag{11.8.42}$$

- If $r_{ds} \geq 10R_D$ and $g_m r_{ds} \gg 1$, current-gain $A_i$ reduces to

$$A_i = g_m \left( R_S || \frac{1}{g_m} \right) \approx 1 \tag{11.8.43}$$

### 11.8.3 Output Resistance

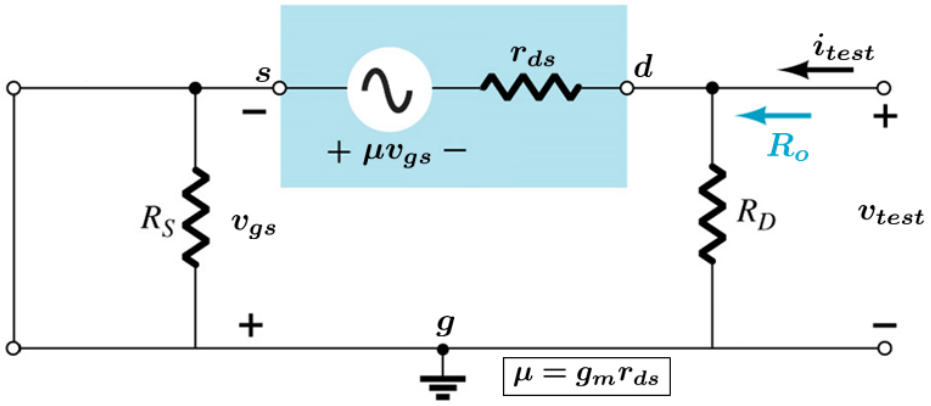



Figure 11.24: Test voltage circuit of Figure 11.23 in order to calculate the output resistance $R_o$.

Output resistance, i.e., Thévenin equivalent resistance, $R_o$ is calculated using the test voltage circuit in Figure 11.24 above. Note that in the circuit $v_{gs} = 0$, so $g_m v_{gs} = 0$ as well.

$$\boxed{R_o = \left.\frac{v_{test}}{i_{test}}\right|_{v_s=0, R_L=v_{test}} = R_D || r_{ds}} \tag{11.8.44}$$

- If $r_{ds} \geq 10R_D$, then $R_o$ simplifies to $R_o = R_D$.
- If a voltage source with source resistance $R_s$ is connected to the input, replace $r_{ds}$ with $([1 + g_m (R_s||R_G)] r_{ds} + R_s||R_G)$ in $R_o$ calculations. We can say that $R_o \approx R_D$ in most cases.

# Chapter 12

# Frequency Response of Amplifiers

## 12.1 First-Order RC Filters

### 12.1.1 First-Order Highpass RC Filter

Consider the first order highpass (HP) RC circuit given in Figure 12.1 below, let us calculate the voltage gain $A = v_o/v_i$. Note that, as the impedance of the capacitor changes with the frequency the gain will change with the frequency.

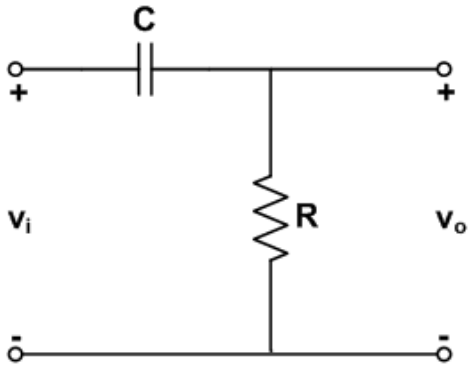



Figure 12.1: First order highpass RC filter.

$$\begin{aligned} A(\omega) = \frac{v_o}{v_i} &= \frac{R}{R + Z_C} && \ldots Z_C = -jX_C = -j\frac{1}{\omega C} \\ &= \frac{1}{1 + \frac{Z_C}{R}} && \ldots \omega = 2\pi f \\ &= \frac{1}{1 - j\frac{1}{\omega CR}} \end{aligned} \tag{12.1.1}$$

$A(\omega)$ is called frequency response of the filter circuit above. As the frequency response $A(\omega)$ is complex, it has a magnitude and phase, i.e.,

$$A(\omega) = |A(\omega)|\, e^{j\angle A(\omega)} \tag{12.1.2}$$

Thus, $A(\omega)$ is called the **frequency response**, $|A(\omega)|$ is called the **magnitude response** and $\angle A(\omega)$ is called the **phase response**.

Given that we know the frequency response of the system. Then, for a sinusoidal input $v_i(t)$

$$v_i(t) = V_m \cos(\omega_0 t), \tag{12.1.3}$$

we obtain the output signal $v_o(t)$ as

$$v_o(t) = |A(\omega_0)| V_m \cos(\omega_0 t + \angle A(\omega_0)). \tag{12.1.4}$$

So, the magnitude and phase of the output determined by the frequency response of the system.

For this highpass system given in (12.1.1), magnitude response $|A(\omega)|$ and phase response $\angle A(\omega)$ are given by

$$|A(\omega)| = \frac{1}{\sqrt{1 + \frac{1}{\omega^2 R^2 C^2}}} \tag{12.1.5}$$

$$\angle A(\omega)| = \arctan\left(\frac{1}{\omega RC}\right) \tag{12.1.6}$$

Note that $\omega \to \infty \Rightarrow |A(\omega)| \to 1$ and $\omega \to 0 \Rightarrow |A(\omega)| \to 0$.

#### 12.1.1.1 Cutoff Frequency

The frequency where the output power drops to half (of the maximum output power) is called the **cutoff frequency** or corner frequency, $\omega_c$. Thus, at the cutoff frequency, the output voltage gain magnitude square will drop to half. As, in this case the maximum gain is one, i.e. $\max |A(\omega)| = 1$,

$$|A(\omega_c)|^2 = \frac{1}{2} \qquad \ldots \text{i.e., } |A(\omega_c)| = \frac{1}{\sqrt{2}}$$

$$\frac{1}{1 + \frac{1}{\omega_c^2 R^2 C^2}} = \frac{1}{2}$$

$$\omega_c = \frac{1}{RC} \qquad \ldots f_c = \frac{1}{2\pi RC}$$

Thus, cutoff frequency $\omega_c$ for the first order highpass RC filter is given by

$$\boxed{\omega_c = \frac{1}{RC}} \tag{12.1.7}$$

Consequently, frequency response of the highpass filter $A(\omega)$ is given by

$$A(\omega) = \frac{1}{1 - j\frac{\omega_c}{\omega}} \tag{12.1.8}$$

$$|A(\omega)| = \frac{1}{\sqrt{1 + \frac{\omega_c^2}{\omega^2}}} \tag{12.1.9}$$

$$\angle A(\omega)| = \arctan\left(\frac{\omega_c}{\omega}\right) \tag{12.1.10}$$

#### 12.1.1.2 Bode Plot

Amplitude response in (12.1.9) above has two asymptotes as shown below

$$\frac{\omega_c^2}{\omega^2} \ll 1 \Rightarrow |A(\omega)| = 1 \tag{12.1.11}$$

$$\frac{\omega_c^2}{\omega^2} \gg 1 \Rightarrow |A(\omega)| = \frac{\omega}{\omega_c} \qquad \ldots |A(\omega_c)| = \frac{\omega_c}{\omega_c} = 1 \tag{12.1.12}$$

These two lines intersect at $\omega = \omega_c$ as shown in Figure 12.2 below.

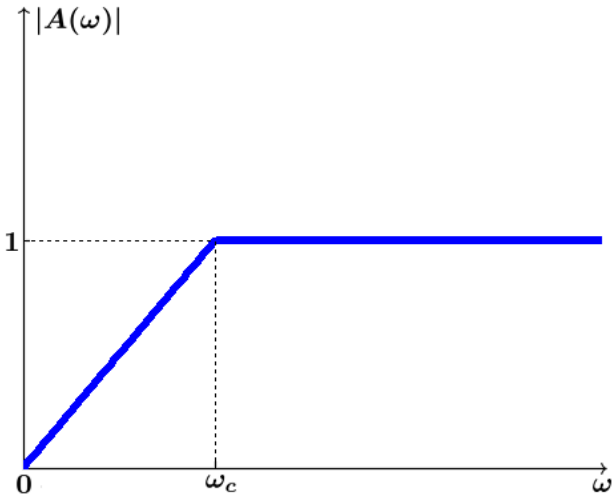



Figure 12.2: Asymptotic Bode plot (scalar) of the first order highpass RC filter in Figure 12.1.

#### 12.1.1.3 Decibels (dB)

The **decibel** (**dB**) is a logarithmic unit used to express the ratio of two values of a physical quantity, often power or intensity. One of these values is often a standard reference value, in which case the decibel is used to express the level of the other value relative to this reference. The term decibel has

its origin in the fact that power and audio levels are related on a logarithmic basis, i.e.,

$$G_{dB} = 10\log_{10}\frac{P_o}{P_i} \tag{12.1.13}$$

$$= 20\log_{10}\left|\frac{V_o}{V_i}\right| \qquad \ldots P = \frac{V^2}{R} \tag{12.1.14}$$

Thus, **magnitude response** in decibels is given by

$$\boxed{|A(\omega)|_{\text{dB}} = 20\log_{10}|A(\omega)|} \tag{12.1.15}$$

Consequently, the **normalized magnitude response** (i.e., maximum value is 1) in decibels is given by

$$\boxed{|\tilde{A}(\omega)|_{\text{dB}} = 20\log_{10}\frac{|A(\omega)|}{\max|A(\omega)|}} \tag{12.1.16}$$

The two asymptotes of the amplitude response in (12.1.9) are expressed in dB as follows

$$\frac{\omega_c^2}{\omega^2} \ll 1 \Rightarrow 20\log_{10}1 = 0\,\text{dB} \tag{12.1.17}$$

$$\frac{\omega_c^2}{\omega^2} \gg 1 \Rightarrow |A(\omega)| = 20\log_{10}\frac{\omega}{\omega_c} = 20\log_{10}\omega - 20\log_{10}\omega_c \tag{12.1.18}$$

These two lines intersect at $\omega = \omega_c$ as shown in Figure 12.3 below.

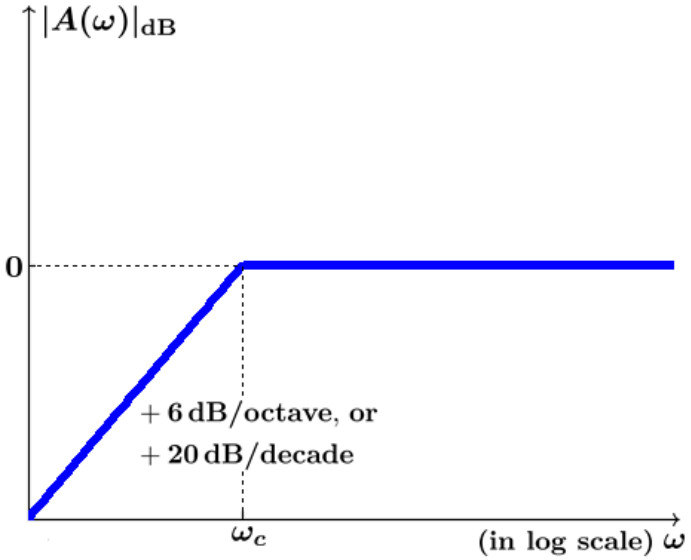



Figure 12.3: Asymptotic Bode plot (dB) of the first order highpass RC filter in Figure 12.1.

As we see from the asymptotic magnitude response in Figure 12.3 above, a **highpass** filter attenuates the low frequencies and keeps the high frequencies intact.

Let us consider the second asymptote (i.e., $20\log_{10}\frac{\omega}{\omega_c}$) and for a given $\omega = \omega_1$ consider the two cases where $\omega_2 = \omega_1/2$ and $\omega_3 = \omega_1/10$, then

$$20\log_{10}\frac{\omega_2}{\omega_c} = 20\log_{10}\frac{\omega_1}{\omega_c} - 20\log_{10}2 \cong 20\log_{10}\frac{\omega_1}{\omega_c} - 6\,\text{dB} \qquad \ldots \text{one octave} \tag{12.1.19}$$

$$20\log_{10}\frac{\omega_3}{\omega_c} = 20\log_{10}\frac{\omega_1}{\omega_c} - 20\log_{10}10 = 20\log_{10}\frac{\omega_1}{\omega_c} - 20\,\text{dB} \qquad \ldots \text{one decade} \tag{12.1.20}$$

A change in frequency by a factor of **two** is equivalent to one **octave**. Similarly, a change in frequency by a factor of **ten** is equivalent to one **decade**.

Thus, the slope of the second asymptote (i.e., $20\log_{10}\frac{\omega}{\omega_c}$) is 6 dB/octave or 20 dB/decade.

So, actual magnitude of the normalized magnitude response at the **cutoff frequency** $\omega_c$ is $|\tilde{A}(\omega_c)| = 1/\sqrt{2}$. Thus, in dBs

$$\boxed{20\log_{10}|\tilde{A}(\omega_c)| = 20\log_{10}\frac{1}{\sqrt{2}} \cong -3\,\text{dB}} \tag{12.1.21}$$

Thus, **cutoff frequency** is **always** 3 dB below the maximum gain.

As a result if we plot (12.1.9) and (12.1.10) against $\omega$, we obtain the **magnitude** and **phase** responses of the first order highpass RC filter as shown in Figure 12.4 below.

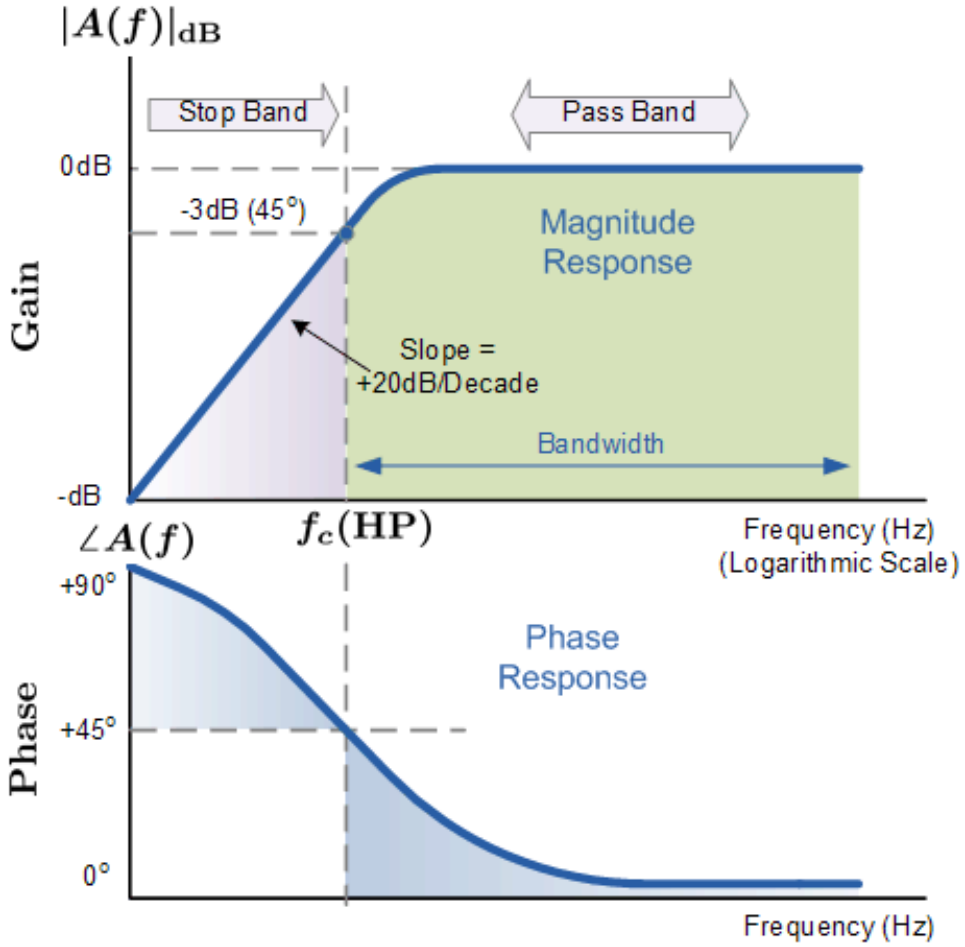



Figure 12.4: Magnitude (top) and phase (bottom) responses of the first order highpass RC filter in Figure 12.1.

### 12.1.2 First-Order Lowpass RC Filter

Consider the first order lowpass (LP) RC circuit given in Figure 12.5 below, let us calculate the voltage gain $A = v_o/v_i$. Note that, as the impedance of the capacitor changes with the frequency the gain

will change with the frequency.

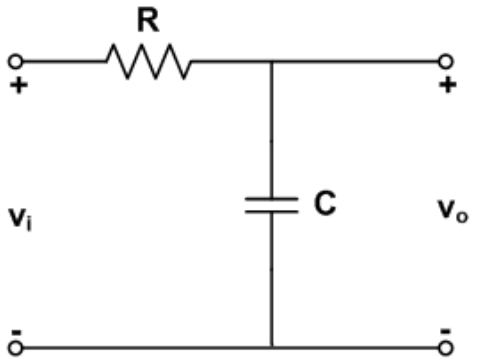



Figure 12.5: First order lowpass RC filter.

$$\begin{aligned} A(\omega) = \frac{v_o}{v_i} &= \frac{Z_C}{Z_C + R} && \ldots Z_C = -jX_C = \frac{1}{j\omega C} \\ &= \frac{1}{1 + \frac{R}{Z_C}} && \ldots \omega = 2\pi f \\ &= \frac{1}{1 + j\omega CR} && (12.1.22) \end{aligned}$$

Thus, **magnitude response** $|A(\omega)|$ and **phase response** $\angle A(\omega)$ are given as

$$|A(\omega)| = \frac{1}{\sqrt{1 + \omega^2 R^2 C^2}} \quad (12.1.23)$$

$$\angle A(\omega)| = -\arctan(\omega RC) \quad (12.1.24)$$

Note that $\omega \to \infty \Rightarrow |A(\omega)| \to 0$ and $\omega \to 0 \Rightarrow |A(\omega)| \to 1$.

#### 12.1.2.1 Cutoff Frequency

Cutoff frequency $\omega_c$ can be found as,

$$\begin{aligned} |A(\omega_c)|^2 &= \frac{1}{2} && \ldots \text{i.e., } |A(\omega_c)| = \frac{1}{\sqrt{2}} \\ \frac{1}{1 + \omega_c^2 R^2 C^2} &= \frac{1}{2} \\ \omega_c &= \frac{1}{RC} && \ldots f_c = \frac{1}{2\pi RC} \end{aligned}$$

Thus, cutoff frequency $\omega_c$ for the first order lowpass RC filter is given by

$$\boxed{\omega_c = \frac{1}{RC}} \quad (12.1.25)$$

Consequently, frequency response of the lowpass filter $A(\omega)$ is given by

$$A(\omega) = \frac{1}{1 + j\frac{\omega}{\omega_c}} \tag{12.1.26}$$

$$|A(\omega)| = \frac{1}{\sqrt{1 + \frac{\omega^2}{\omega_c^2}}} \tag{12.1.27}$$

$$\angle A(\omega)| = -\arctan\left(\frac{\omega}{\omega_c}\right) \tag{12.1.28}$$

#### 12.1.2.2 Bode Plot

The two asymptotes of the amplitude response in (12.1.27) are expressed in dB as follows

$$\frac{\omega^2}{\omega_c^2} \ll 1 \Rightarrow 20\log_{10} 1 = 0\,\text{dB} \tag{12.1.29}$$

$$\frac{\omega^2}{\omega_c^2} \gg 1 \Rightarrow |A(\omega)| = 20\log_{10}\frac{\omega_c}{\omega} = 20\log_{10}\omega_c - 20\log_{10}\omega \tag{12.1.30}$$

These two lines intersect at $\omega = \omega_c$ as shown in Figure 12.6 below.

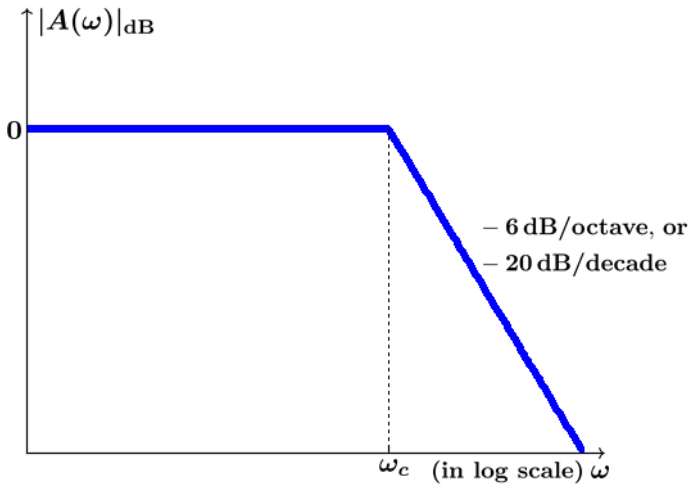



Figure 12.6: Asymptotic Bode plot (dB) of the first order lowpass RC filter in Figure 12.5.

As we see from the asymptotic magnitude response in Figure 12.6 above, a **lowpass** filter keeps the low frequencies intact and attenuates the high frequencies.

Let us consider the second asymptote (i.e., $20\log_{10}\frac{\omega_c}{\omega}$) and for a given $\omega = \omega_1$ consider the two cases where $\omega_2 = 2\omega_1$ and $\omega_3 = 10\omega_1$, then

$$20\log_{10}\frac{\omega_c}{\omega_2} = 20\log_{10}\frac{\omega_c}{\omega_1} - 20\log_{10} 2 \cong 20\log_{10}\frac{\omega_c}{\omega_1} - 6\,\text{dB} \qquad \ldots\text{one octave} \tag{12.1.31}$$

$$20\log_{10}\frac{\omega_c}{\omega_3} = 20\log_{10}\frac{\omega_c}{\omega_1} - 20\log_{10} 10 = 20\log_{10}\frac{\omega_c}{\omega_1} - 20\,\text{dB} \qquad \ldots\text{one decade} \tag{12.1.32}$$

Thus, the slope of the second asymptote (i.e., $20\log_{10}\frac{\omega}{\omega_c}$) is 6 dB/octave or 20 dB/decade.

So, actual magnitude of the normalized magnitude response at the **cutoff frequency** $\omega_c$ is $|\tilde{A}(\omega_c)| = 1/\sqrt{2}$. Thus, in dBs

$$\boxed{20\log_{10}|\tilde{A}(\omega_c)| = 20\log_{10}\frac{1}{\sqrt{2}} \cong -3\,\text{dB}} \tag{12.1.33}$$

Thus, **cutoff frequency** is **always** 3 dB below the maximum gain.

As a result if we plot (12.1.27) and (12.1.28) against $\omega$, we obtain the **magnitude** and **phase** responses of the first order lowpass RC filter as shown in Figure 12.7 below.

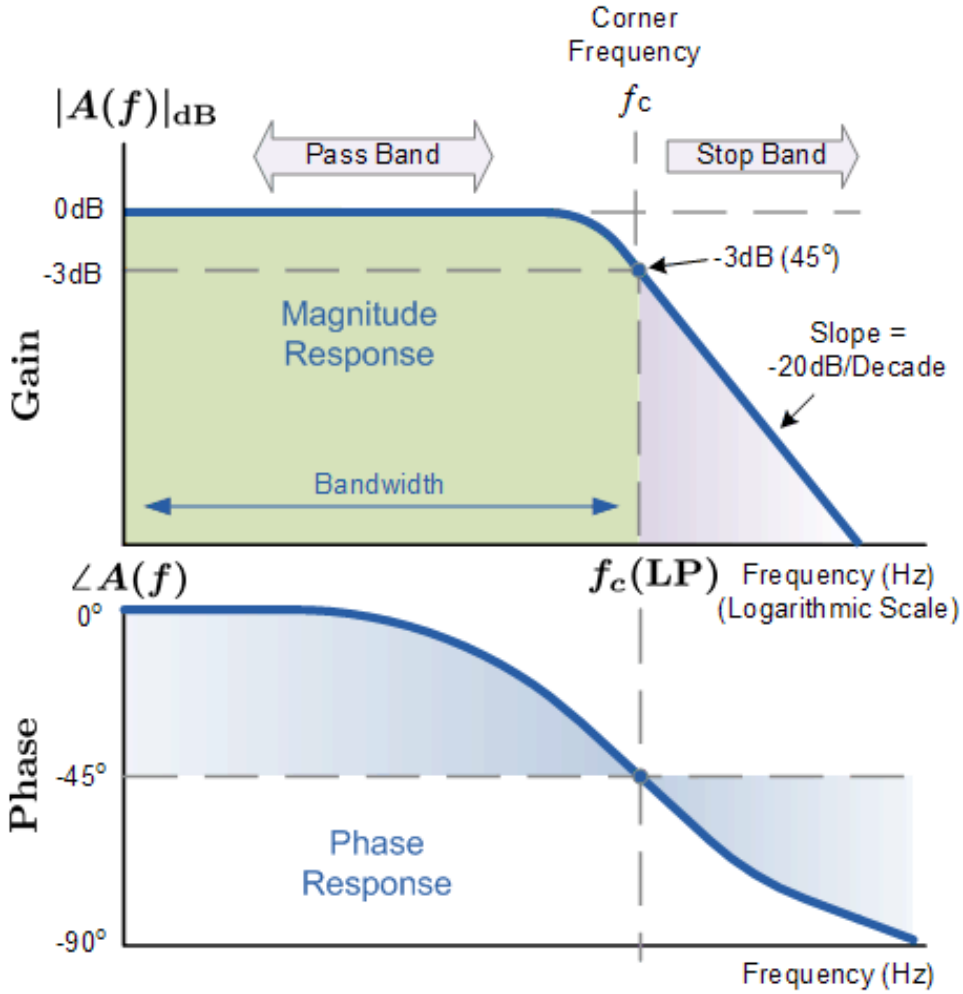



Figure 12.7: Magnitude (top) and phase (bottom) responses of the first order lowpass RC filter in Figure 12.5.

## 12.2 Typical Frequency Response

The magnitudes of the gain response curves of an RC-coupled amplifier system are given in Figure 12.8 below. In the plot low-, high-, and mid-frequency regions are defined. This magnitude response shown in Figure 12.8 below is the response of a **bandpass amplifier**. It amplifies a band of frequencies

(namely midband, or mid-frequency band) and attenuates the low or high frequencies. Note that, the low-frequency part of the amplifier looks like a highpass amplifier and the high-frequency part of the amplifier looks like a lowpass amplifier.Thus, we can obtain a bandpass amplifier by combining a highpass and a lowpass amplifier.

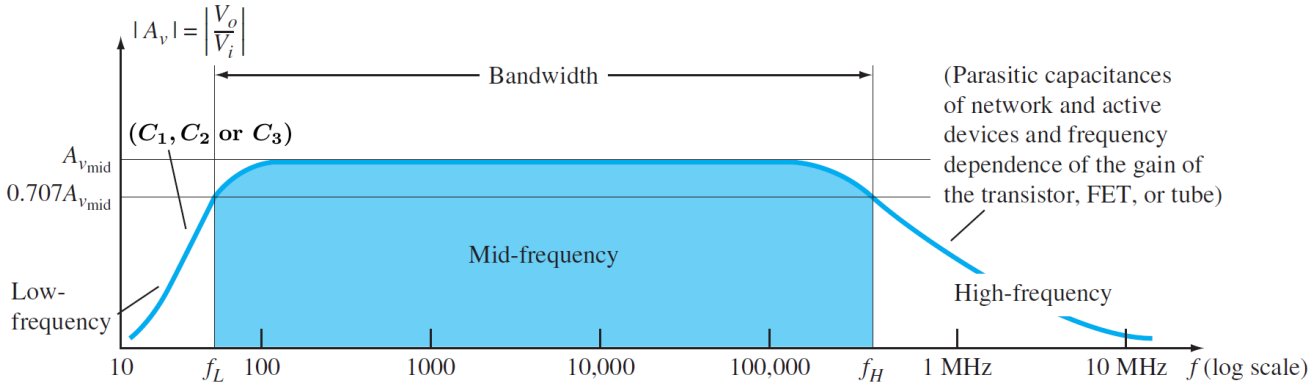



Figure 12.8: Typical magnitude response of a transistor amplifier.

The **purpose of frequency analysis** in this course is to determine the low-frequency cutoff $f_L$ and the high-frequency cutoff $f_H$ of the amplifier. Low-frequency cut-off $f_L$ is determined by the capacitors in the circuit, i.e., $C_1$, $C_2$ and $C_3$, and high-frequency cutoff $f_H$ is determined by the internal device capacitances, wiring capacitances or parasitic capacitances.

Typically, low-frequency capacitors $C_1$, $C_2$ and $C_3$ are in the microFarad ($\mu$F) range, and high-frequency capacitances (wiring capacitances and parasitic capacitances) are in the picoFarad (pF) range.

Consequently, low-frequency capacitors are short-circuit for high-frequency, and high-frequency capacitances are open-circuit for low-frequency. So, low-frequency response and high-frequency response will be dealt with separately. The **bandwidth** (or passband, or midband) of the amplifier is determined as,

$$\boxed{\text{Bandwidth (BW)} = f_H - f_L} \tag{12.2.34}$$

Up to now, we have calculated the mid-frequency (midband) input resistance $R_i = Z_{i_{mid}}$, voltage gain $A_v = A_{v_{mid}}$ and output resistance input resistance $R_o = Z_{o_{mid}}$, where we ignored the low-frequency and high-frequency effects assuming the low-frequency capacitances were short-circuit and high-frequency capacitances were open-circuit.

Scalar and decibel plot of the normalized magnitude response is shown in Figure 12.9 and Figure 12.10 below, respectively.

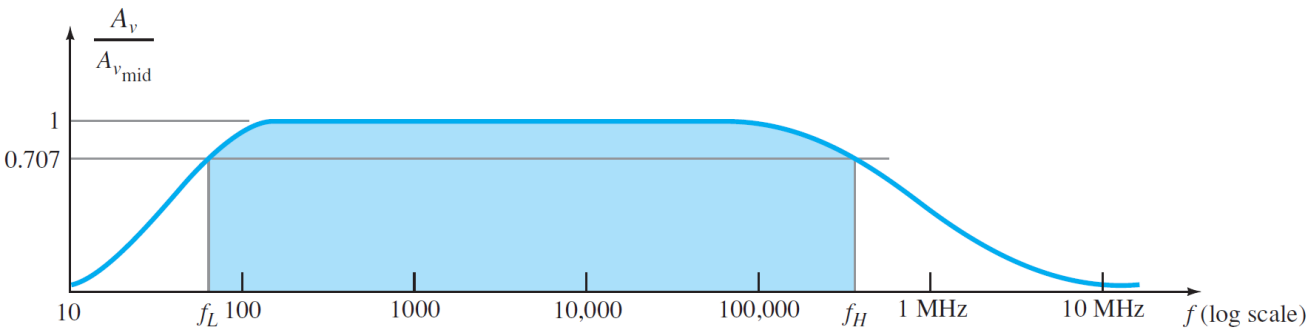



Figure 12.9: Normalized scalar plot of the magnitude response given in Figure 12.8.

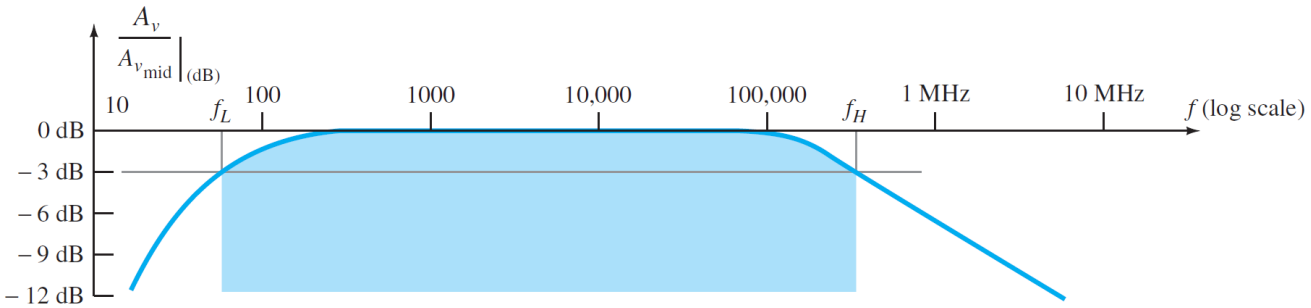



Figure 12.10: Normalized decibel plot of the magnitude response given in Figure 12.8.

## 12.3 Low Frequency Response

### 12.3.1 BJT Amplifiers

For the circuit shown in Figure 12.11 below, the capacitors $C_1$, $C_2$, and $C_3$ will determine the low-frequency response. Capacitors $C_1$ and $C_2$ at the input and output of the circuit are called the **coupling** capacitors, and $C_3$ is called the **bypass** capacitor. We will now examine the impact of each independently in the order listed as first order RC filters.

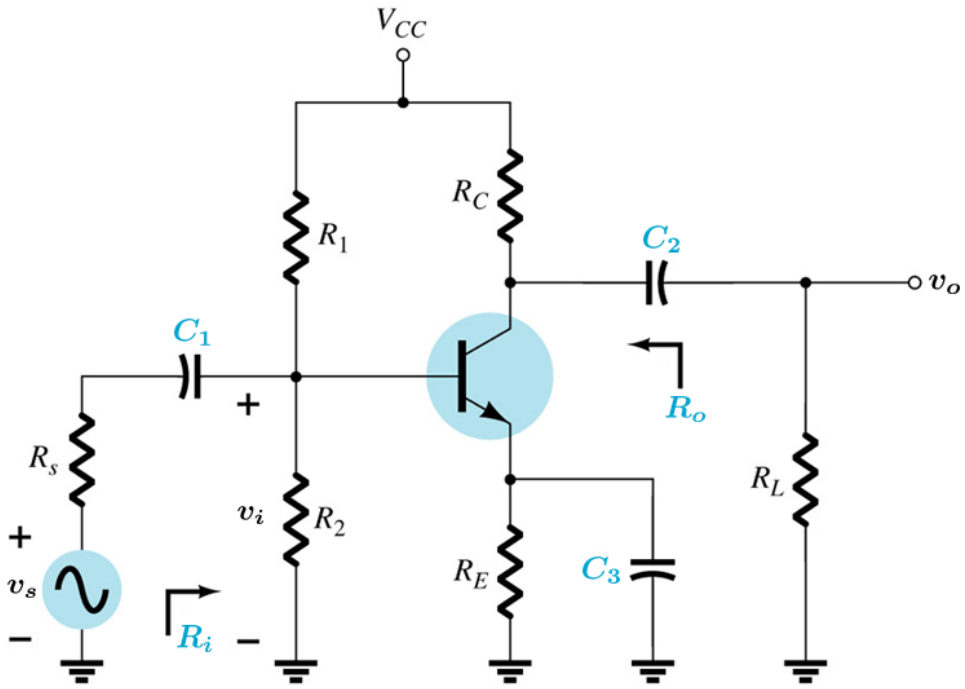



Figure 12.11: A common-emitter voltage-divider bias BJT circuit.

#### 12.3.1.1 Effect of Coupling Capacitor $C_1$

For the BJT circuit shown in Figure 12.11 above, capacitor $C_1$ and the equivalent-resistance of $R_s$ and $R_i$ ($R_{eq_1} = R_s + R_i$) form a first-order highpass filter structure given in Figure 12.1 with a cutoff frequency $f_{L_1}$ of

$$\boxed{f_{L_1} = \frac{1}{2\pi\left(R_s + R_i\right)C_1}} \tag{12.3.35}$$

where $R_s$ is the source (e.g., voltage source) resistance and $R_i$ is the **input resistance** of the amplifier, value of which for this circuit is given by

$$R_i = R_1||R_2||h_{ie}.$$

#### 12.3.1.2 Effect of Coupling Capacitor $C_2$

For the BJT circuit shown in Figure 12.11 above, capacitor $C_2$ and the equivalent-resistance of $R_o$ and $R_L$ ($R_{eq_2} = R_o + R_L$) form a first-order highpass filter structure given in Figure 12.1 with a cutoff frequency $f_{L_2}$ of

$$\boxed{f_{L_2} = \frac{1}{2\pi\left(R_o + R_L\right)C_2}} \tag{12.3.36}$$

where $R_L$ is the load resistance and $R_o$ is the **output resistance** of the amplifier, value of which for this circuit is given by

$$R_o = R_C||1/h_{oe}.$$

#### 12.3.1.3 Effect of Bypass Capacitor $C_3$

For the BJT circuit shown in Figure 12.11 above, capacitor $C_3$ and the equivalent Thévenin resistance $R_{eq_3}$ seen by $C_3$ form a first-order lowpass filter structure given in Figure 12.5 with a cutoff frequency $f_{L_3}$ of

$$\boxed{f_{L_3} = \frac{1}{2\pi R_{eq_3} C_3}} \tag{12.3.37}$$

where $R_{eq_3}$ is the Thévenin resistance seen by $C_3$ (i.e., like the output resistance of the emitter-follower), value of which for this circuit is given by

$$R_{eq_3} = R_E || \frac{R_s || R_1 || R_2 + h_{ie}}{h_{fe} + 1}.$$

#### 12.3.1.4 Combined Effect of $C_1$, $C_2$ and $C_3$

Each cutoff frequency $f_{L_1}$, $f_{L_2}$ and $f_{L_3}$ adds an additional 6 dB/octave slope as shown in Figure 12.12 below. Overall cutoff frequency $f_L$ is higher than the highest value of these three cutoff frequencies, i.e.,

$$\boxed{f_L \geq \max\left(f_{L_1}, f_{L_2}, f_{L_3}\right)} \tag{12.3.38}$$

When the three cut-off frequencies (or the highest cutoff frequency) are a decade apart from each other, than the overall cutoff frequency is almost equal to the highest of these three frequencies as depicted in Figure 12.12 below, i.e.,

$$f_L \approx \max\left(f_{L_1}, f_{L_2}, f_{L_3}\right) \tag{12.3.39}$$

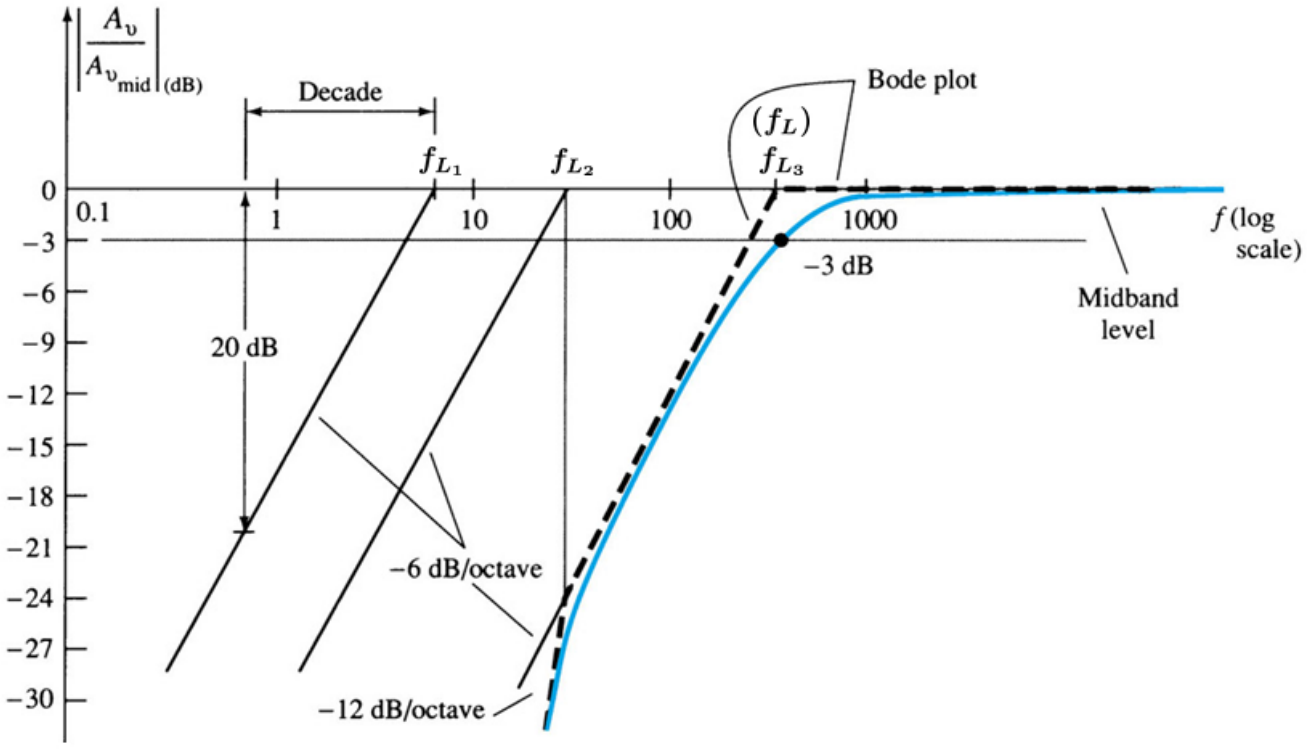



Figure 12.12: Low-frequency plot for the circuit given in Figure 12.11.

As $R_{eq_3}$ normally has the lowest resistance value, generally $f_{L_3}$ holds the highest value. Also as generally $R_i > R_o$, mostly $f_{L_2} > f_{L_1}$. So, generally $f_{L_3} > f_{L_2} > f_{L_1}$.

Even though these assumptions may not hold, we generally select the value of the capacitors $C_1$, $C_2$ and $C_3$ properly to have the cutoff frequencies to be at least a decade apart, e.g., $f_{L_3} > 10f_{L_2} > 10f_{L_1}$, in order to reduce the coupling effect of all three capacitors to the cutoff frequency $f_L$.

If the decade-apart condition do not hold, then the cutoff frequency $f_L$ will move up towards the mid-frequency range and has to be calculated from the overall third-order highpass system by considering the effects of all three-capacitors.

### 12.3.2 FET Amplifiers

For the circuit shown in Figure 12.13 below, the capacitors $C_1$, $C_2$, and $C_3$ will determine the low-frequency response. Capacitors $C_1$ and $C_2$ at the input and output of the circuit are called the **coupling** capacitors, and $C_3$ is called the **bypass** capacitor. We will now examine the impact of each independently in the order listed as first order RC filters.

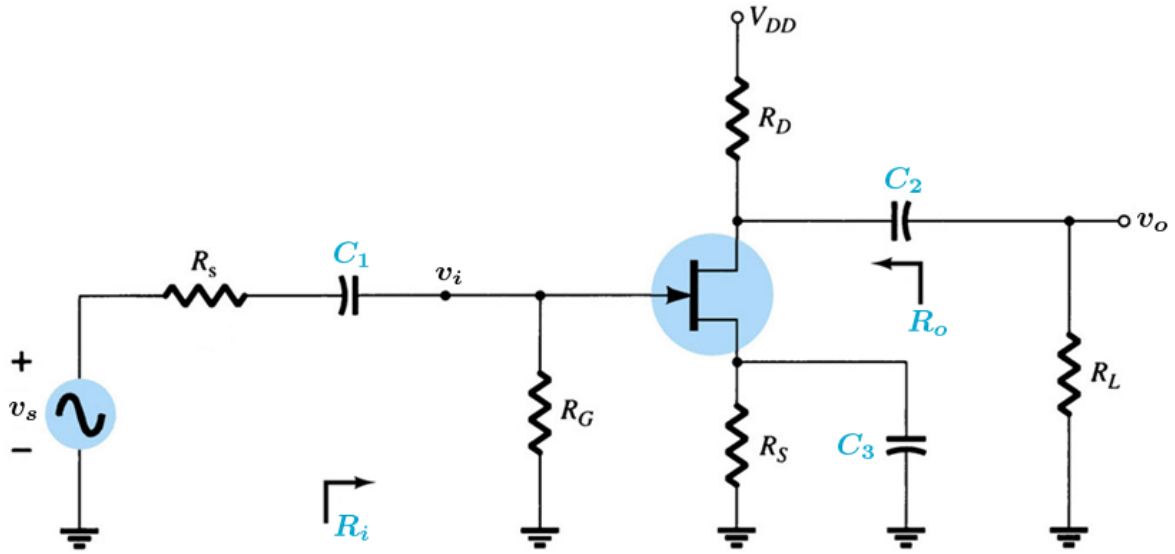



Figure 12.13: A common-source self-bias JFET circuit.

#### 12.3.2.1 Effect of Coupling Capacitor $C_1$

For the JFET circuit shown in Figure 12.13 above, capacitor $C_1$ and the equivalent-resistance of $R_s$ and $R_i$ ($R_{eq_1} = R_s + R_i$) form a first-order highpass filter structure given in Figure 12.1 with a cutoff frequency $f_{L_1}$ of

$$\boxed{f_{L_1} = \frac{1}{2\pi\left(R_s + R_i\right)C_1}} \tag{12.3.40}$$

where $R_s$ is the source (e.g., voltage source) resistance and $R_i$ is the **input resistance** of the amplifier, value of which for this circuit is given by

$$R_i = R_G.$$

#### 12.3.2.2 Effect of Coupling Capacitor $C_2$

For the JFET circuit shown in Figure 12.13 above, capacitor $C_2$ and the equivalent-resistance of $R_o$ and $R_L$ ($R_{eq_2} = R_o + R_L$) form a first-order highpass filter structure given in Figure 12.1 with a cutoff frequency $f_{L_2}$ of

$$\boxed{f_{L_2} = \frac{1}{2\pi\left(R_o + R_L\right)C_2}} \tag{12.3.41}$$

where $R_L$ is the load resistance and $R_o$ is the **output resistance** of the amplifier, value of which for this circuit is given by

$$R_o = R_D||r_{ds}.$$

#### 12.3.2.3 Effect of Bypass Capacitor $C_3$

For the JFET circuit shown in Figure 12.13 above, capacitor $C_3$ and the equivalent Thévenin resistance $R_{eq_3}$ seen by $C_3$ form a first-order lowpass filter structure given in Figure 12.5 with a cutoff frequency $f_{L_3}$ of

$$\boxed{f_{L_3} = \frac{1}{2\pi R_{eq_3} C_3}} \tag{12.3.42}$$

where $R_{eq_3}$ is the Thévenin resistance seen by $C_3$ (i.e., like the output resistance of the source-follower), value of which for this circuit is given by

$$R_{eq_3} = R_S || r_{ds} || \frac{1}{g_m}$$

#### 12.3.2.4 Combined Effect of $C_1$, $C_2$ and $C_3$

Each cutoff frequency $f_{L_1}$, $f_{L_2}$ and $f_{L_3}$ adds an additional 6 dB/octave slope as shown in Figure 12.14 below. Overall cutoff frequency $f_L$ is higher than the highest value of these three cutoff frequencies, i.e.,

$$\boxed{f_L \geq \max\left(f_{L_1}, f_{L_2}, f_{L_3}\right)} \tag{12.3.43}$$

When the three cut-off frequencies (or the highest cutoff frequency) are a decade apart from each other, than the overall cutoff frequency is almost equal to the highest of these three frequencies as depicted in Figure 12.14 below, i.e.,

$$f_L \approx \max\left(f_{L_1}, f_{L_2}, f_{L_3}\right) \tag{12.3.44}$$

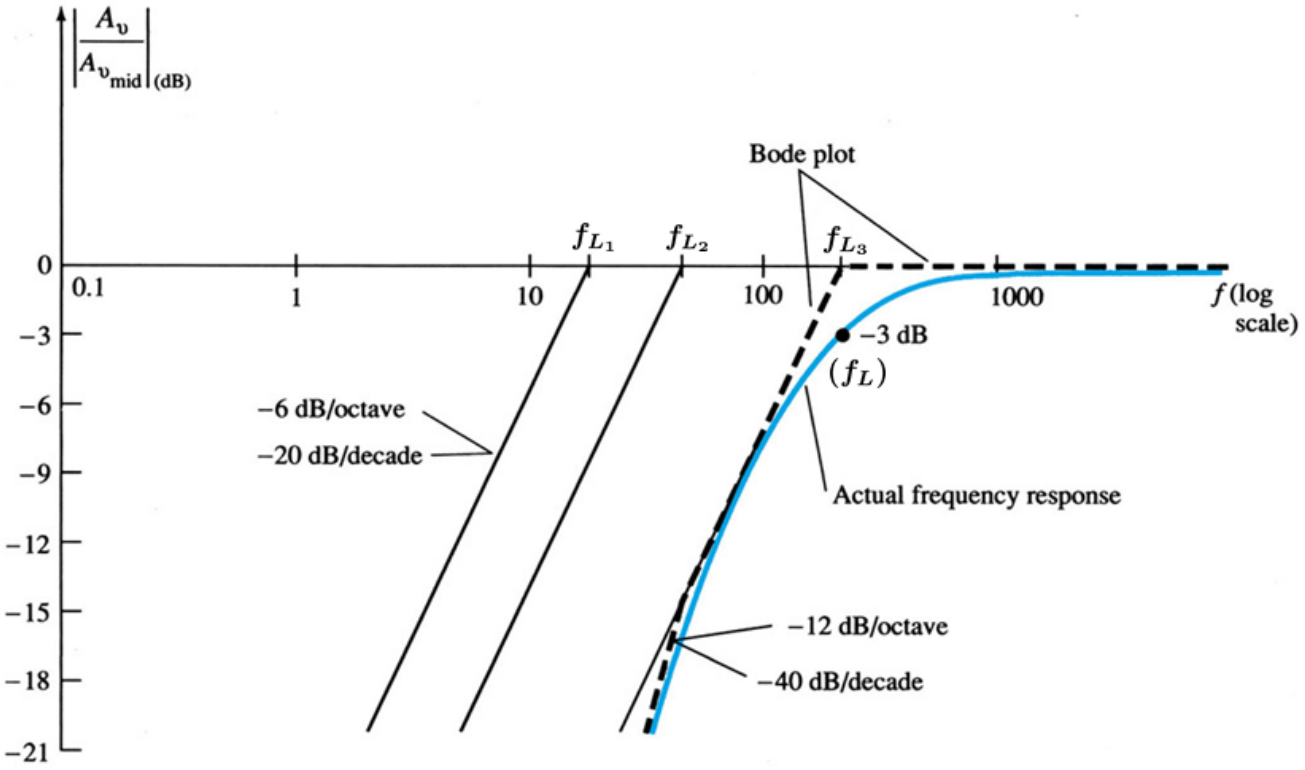



Figure 12.14: Low-frequency plot for the circuit given in Figure 12.13.

As $R_{eq_3}$ has the lowest resistance value, $f_{L_3}$ holds the highest value. Also as $R_i \gg R_o$, $f_{L_2} > f_{L_1}$. So, almost always $f_{L_3} > f_{L_2} > f_{L_1}$.

We generally select the value of the capacitors $C_1$, $C_2$ and $C_3$ properly to have the cutoff frequencies to be at least a decade apart, e.g., $f_{L_3} > 10f_{L_2} > 10f_{L_1}$, in order to reduce the coupling effect of all three capacitors to the cutoff frequency $f_L$.

## 12.4 Miller Effect

For **inverting amplifiers** (phase shift of 180° between input and output, resulting in a negative value for $A_v$), the input and output capacitance is increased by a capacitance level sensitive to the interelectrode capacitance between the input and output terminals of the device and the gain of the amplifier. Thus, Miller effect only occurs in common-emitter and common-source amplifiers.

Capacitance $C_f$ between input and output will be represented by its equivalent Miller capacitance at the input $C_{M_i}$ and at the output $C_{M_o}$.

For noninverting amplifiers such as the common-base and emitter-follower (or common-gate and source-follower) configurations, the Miller effect capacitance is not a contributing concern for high-frequency applications.

#### 12.4.0.1 Miller Input Capacitance $C_{M_i}$

Consider the network shown in Figure 12.15 below, let us calculate the input impedance $Z_i = v_i/i_i$

$$
\begin{aligned}
Z_i = \frac{v_i}{i_i} &= \frac{v_i}{i_1 + i_f} && \ldots i_1 = \frac{v_i}{R_i}, i_f = \frac{v_i - v_o}{Z_{C_f}} \\
&= \frac{v_i}{v_i/R_i + \frac{v_i - A_v v_i}{Z_{C_f}}} && \ldots v_o = A_v v_i, Z_{C_f} = \frac{1}{j\omega C_f} \\
&= R_i || \frac{Z_{C_f}}{1 - A_v} && \ldots Z_{M_i} = \frac{Z_{C_f}}{1 - A_v} \\
&= Z_{M_i} || R_i && \ldots Z_{M_i} = \frac{1}{j\omega C_{M_i}}, C_{M_i} = (1 - A_v)\, C_f
\end{aligned}
$$

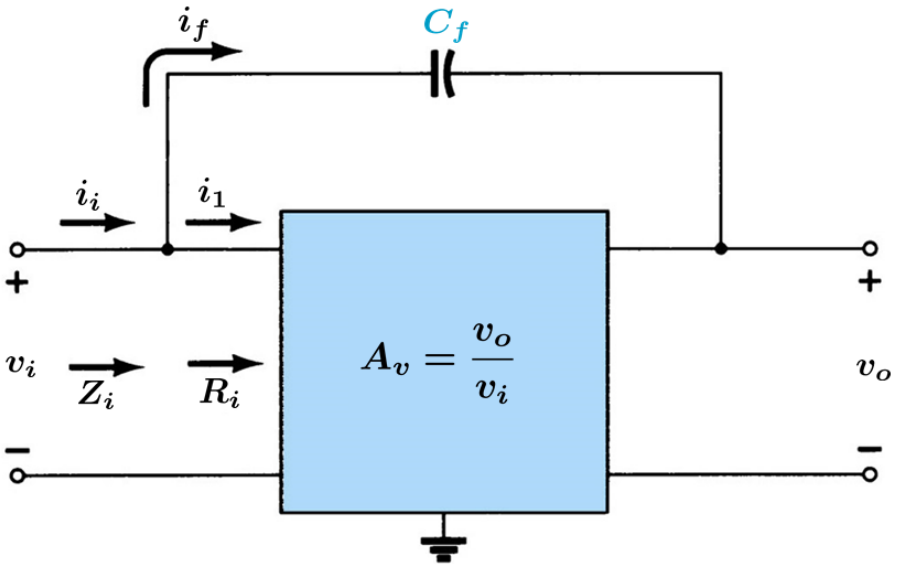



Figure 12.15: Circuit employed in the derivation of an equation for the Miller input capacitance $C_{M_i}$, where $A_v < 0$.

So, Miller input capacitance $C_{M_i}$ is given by

$$\boxed{C_{M_i} = (1 - A_v)\, C_f} \tag{12.4.45}$$

Thus, the feedback capacitance $C_f$ appears as a higher capacitance at the input, increased by a factor of $(1 - A_v)$. Note that, $A_v < 0$.

#### 12.4.0.2 Miller Output Capacitance $C_{M_o}$

Consider the network shown in Figure 12.16 below, let us calculate the output impedance $Z_o = v_o/i_o$

$$
\begin{aligned}
Z_o = \frac{v_o}{i_o} &= \frac{v_o}{i_1 + i_f} && \ldots i_1 = \frac{v_o}{R_o}, i_f = \frac{v_o - v_i}{Z_{C_f}} \\
&= \frac{v_o}{v_o/R_o + \frac{v_o - v_o/A_v}{Z_{C_f}}} && \ldots v_o = A_v v_i, Z_{C_f} = \frac{1}{j\omega C_f} \\
&= R_o || \frac{Z_{C_f}}{1 - \frac{1}{A_v}} && \ldots Z_{M_o} = \frac{Z_{C_f}}{1 - \frac{1}{A_v}} \\
&= R_o || Z_{M_o} && \ldots Z_{M_o} = \frac{1}{j\omega C_{M_o}}, C_{M_o} = \left(1 - \frac{1}{A_v}\right) C_f
\end{aligned}
$$

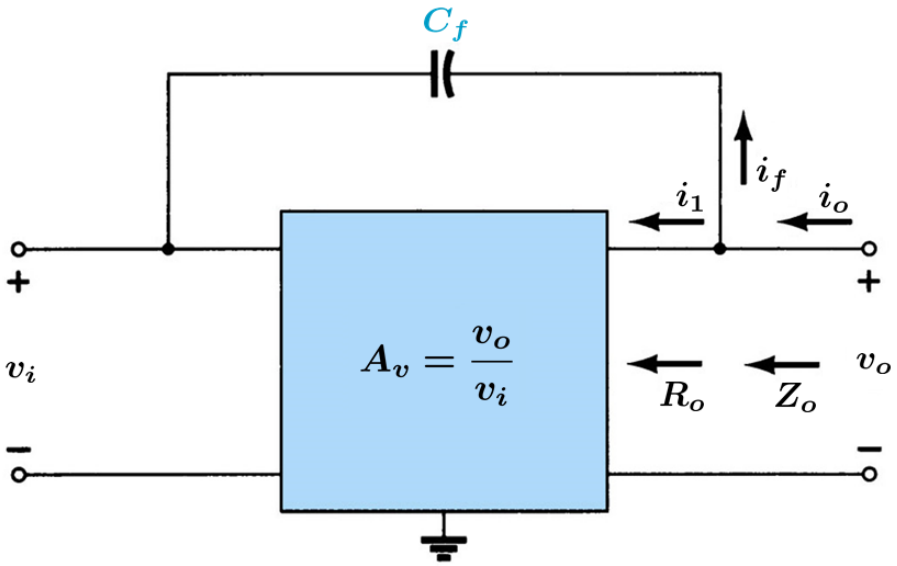



Figure 12.16: Circuit employed in the derivation of an equation for the Miller output capacitance $C_{M_o}$, where $A_v < 0$.

So, Miller output capacitance $C_{M_o}$ is given by

$$
\boxed{C_{M_o} = \left(1 - \frac{1}{A_v}\right) C_f \cong C_f} \tag{12.4.46}
$$

Thus, the feedback capacitance $C_f$ appears as a similar capacitance at the output. Note that, $A_v < 0$ and $|A_v| \gg 1$.

#### 12.4.0.3 Miller Representation

Miller input and output capacitances for the feedback capacitance ($C_f$) remove the feedback and simplify the representation as shown in Figure 12.17 below.

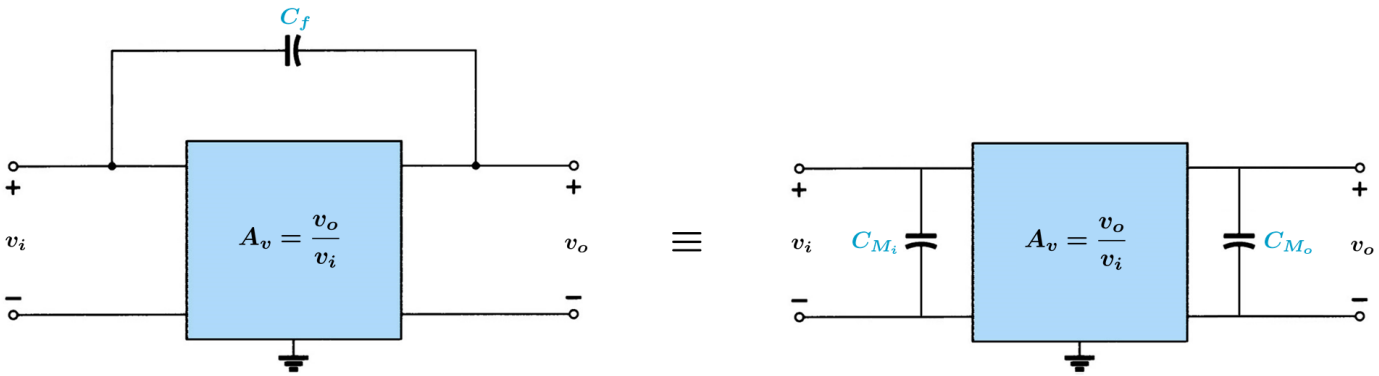



Figure 12.17: Miller representation of the feedback capacitance in negative gain amplifiers.

## 12.5 High Frequency Response

### 12.5.1 BJT Amplifiers

For the high-frequency circuit shown in Figure 12.18 below, there are two factors that define the $-3\,\text{dB}$ cutoff point: the network capacitance (parasitic ($C_{be}, C_{bc}, C_{ce}$) and wiring ($C_{W_i}, C_{W_o}$) capacitance) and the frequency dependence of $h_{fe}$ (or $\beta$). Note that, low-frequency capacitors $C_1$, $C_2$ and $C_3$ are short circuit and have **no effect** in high-frequency analysis.

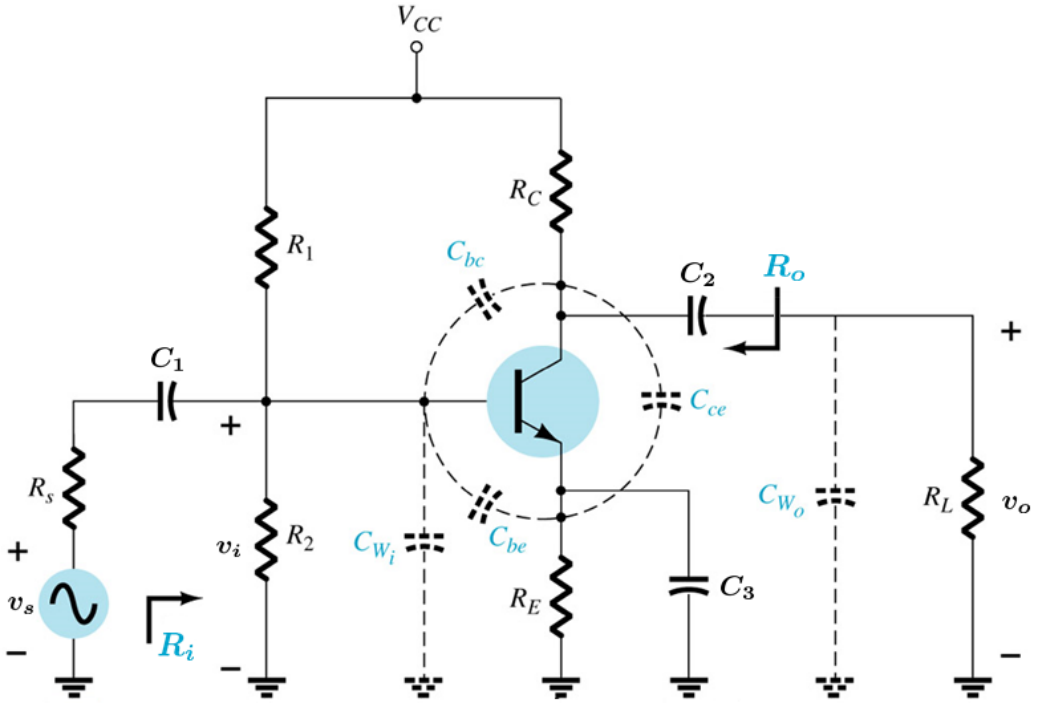



Figure 12.18: A common-emitter voltage-divider bias BJT circuit with the capacitors that affect the high-frequency response.

#### 12.5.1.1 Input Circuit Cutoff Frequency $f_{H_1}$

For the BJT circuit shown in Figure 12.18 above, equivalent total input capacitance $C_{eq_i}$ and the Thévenin equivalent input resistance of $R_{eq_i} = R_s||R_i$ form a first-order lowpass filter structure given

in Figure 12.5 with a cutoff frequency $f_{H_1}$ of

$$\boxed{f_{H_1} = \frac{1}{2\pi \left(R_s || R_i\right) C_{eq_i}}} \tag{12.5.47}$$

with

$$C_{eq_i} = C_{W_i} + C_{M_i} + C_{be} \tag{12.5.48}$$

where $R_s$ is the source (e.g., voltage source) resistance, $R_i$ is the **input resistance** of the amplifier and $C_{M_i}$ is the **Miller input capacitance** given by

$$R_i = R_1 || R_2 || h_{ie}, \tag{12.5.49}$$
$$C_{M_i} = \left(1 - A_V\right) C_{bc}. \tag{12.5.50}$$

#### 12.5.1.2 Output Circuit Cutoff Frequency $f_{H_2}$

For the BJT circuit shown in Figure 12.18 above, equivalent total output capacitance $C_{eq_o}$ and the Thévenin equivalent output resistance of $R_{eq_o} = R_o || R_L$ form a first-order lowpass filter structure given in Figure 12.5 with a cutoff frequency $f_{H_2}$ of

$$\boxed{f_{H_2} = \frac{1}{2\pi \left(R_o || R_L\right) C_{eq_o}}} \tag{12.5.51}$$

with

$$C_{eq_o} = C_{ce} + C_{M_o} + C_{W_o} \tag{12.5.52}$$

where $R_L$ is the load resistance, $R_o$ is the **output resistance** of the amplifier and $C_{M_o}$ is the **Miller output capacitance** given by

$$R_o = R_C || 1/h_{oe}, \tag{12.5.53}$$
$$C_{M_o} = \left(1 - 1/A_V\right) C_{bc} \cong C_{bc}. \tag{12.5.54}$$

#### 12.5.1.3 $h_{fe}$ (or $\beta$) Variation Cutoff Frequency $f_\beta$

The $h_{fe}$ parameter (or $\beta$) of a transistor varies with frequency as shown in Figure 12.19 below and given by

$$h_{fe} = \frac{h_{fe_{mid}}}{1 + j\frac{f}{f_\beta}} \tag{12.5.55}$$

where $f_\beta$ is given by

$$\boxed{f_\beta = \frac{f_T}{h_{fe_{mid}}} \cong \frac{1}{2\pi\, h_{ie} \left(C_{be} + C_{bc}\right)}} \qquad \ldots f_T \cong \frac{1}{2\pi\, r_e \left(C_{be} + C_{bc}\right)} \tag{12.5.56}$$

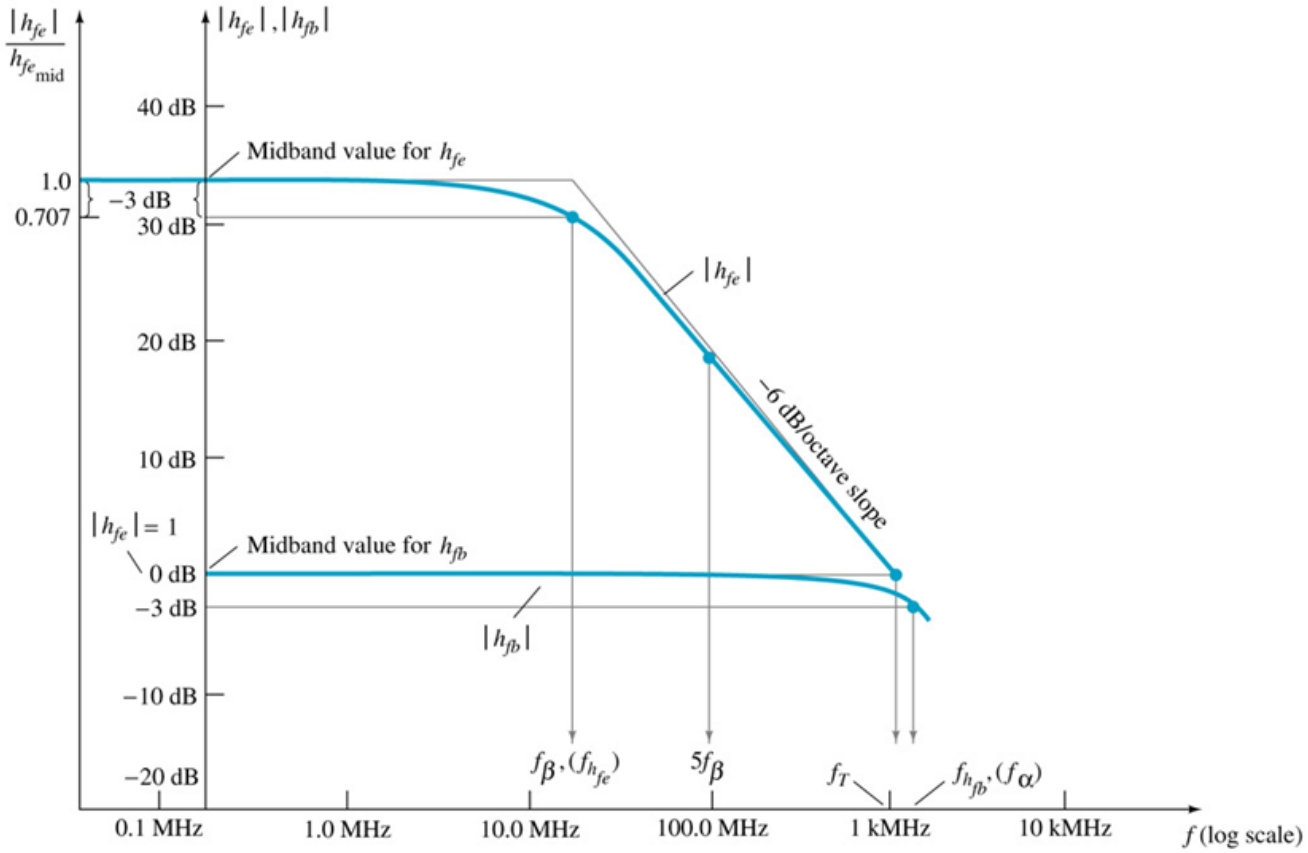



Figure 12.19: $h_{fe}$ and $h_{fb}$ versus frequency in the high-frequency region.

#### 12.5.1.4 Combined Effect of $f_{H_1}$, $f_{H_2}$ and $f_\beta$

Each cutoff frequency $f_{H_1}$, $f_{H_2}$ and $f_\beta$ adds an additional 6 dB/octave slope as shown in Figure 12.20 below. Overall cutoff frequency $f_H$ is lower than the lowest value of these three cutoff frequencies, i.e.,

$$\boxed{f_H \leq \min\left(f_{H_1}, f_{H_2}, f_\beta\right)} \tag{12.5.57}$$

When the three cut-off frequencies (or the lowest cutoff frequency) are a decade apart from each other, than the overall higher cutoff frequency $f_H$ is almost equal to the lowest of these three frequencies as depicted in Figure 12.20 below, i.e.,

$$f_H \approx \min\left(f_{H_1}, f_{H_2}, f_\beta\right) \tag{12.5.58}$$

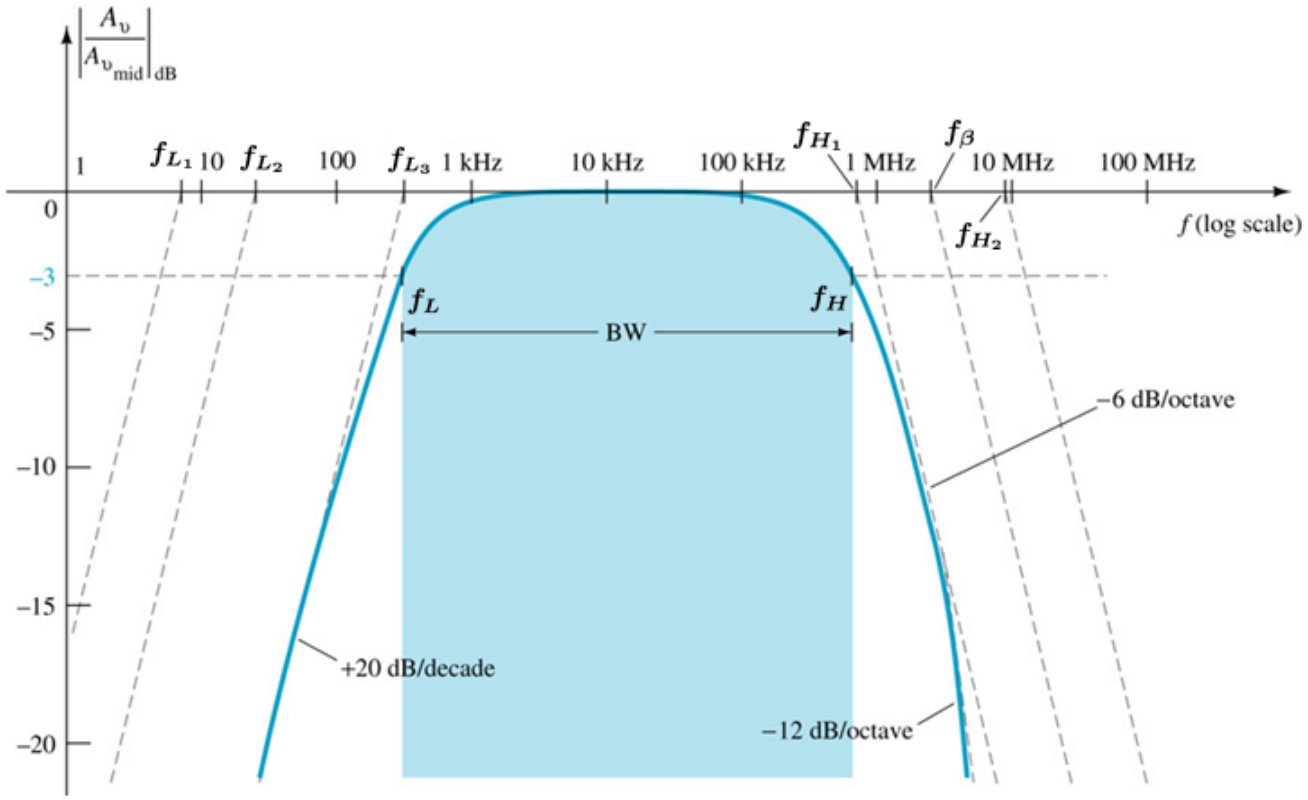



Figure 12.20: Normalized magnitude response (normalized gain vs. frequency) for the circuit given in Figure 12.18.

As Miller input capacitance $C_{M_i}$ has the highest capacitance, almost always $f_{H_1}$ holds the lowest value. Also not always, but generally $f_\beta < f_{H_2}$.

### 12.5.2 FET Amplifiers

For the high-frequency circuit shown in Figure 12.21 below, there are two factors that define the $-3$ dB cutoff point: the network capacitance (parasitic $(C_{gs}, C_{gd}, C_{ds})$ and wiring $(C_{W_i}, C_{W_o})$ capacitance). Note that, low-frequency capacitors $C_1$, $C_2$ and $C_3$ are short circuit and have **no effect** in high-frequency analysis.

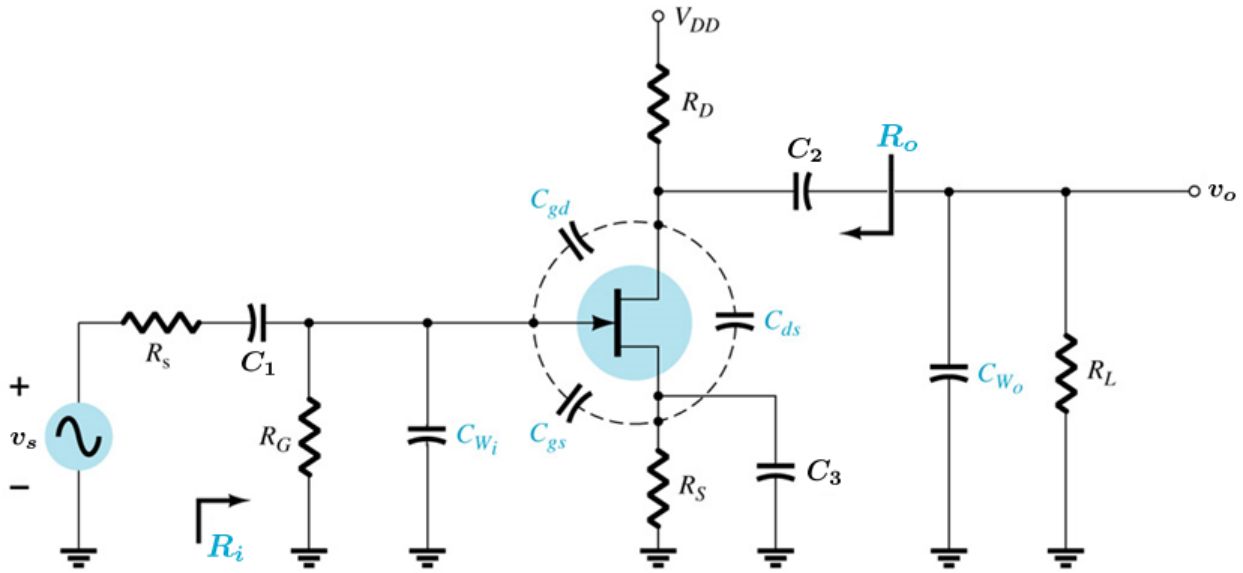



Figure 12.21: A common-source self-bias JFET circuit with the capacitors that affect the high-frequency response.

#### 12.5.2.1 Input Circuit Cutoff Frequency $f_{H_1}$

For the JFET circuit shown in Figure 12.21 above, equivalent total input capacitance $C_{eq_i}$ and the Thévenin equivalent input resistance of $R_{eq_i} = R_s||R_i$ form a first-order lowpass filter structure given in Figure 12.5 with a cutoff frequency $f_{H_1}$ of

$$\boxed{f_{H_1} = \frac{1}{2\pi\left(R_s||R_i\right)C_{eq_i}}} \tag{12.5.59}$$

with

$$C_{eq_i} = C_{W_i} + C_{M_i} + C_{gs} \tag{12.5.60}$$

where $R_s$ is the source (e.g., voltage source) resistance, $R_i$ is the **input resistance** of the amplifier and $C_{M_i}$ is the **Miller input capacitance** given by

$$R_i = R_G, \tag{12.5.61}$$

$$C_{M_i} = \left(1 - A_V\right)C_{gd}. \tag{12.5.62}$$

#### 12.5.2.2 Output Circuit Cutoff Frequency $f_{H_2}$

For the JFET circuit shown in Figure 12.21 above, equivalent total output capacitance $C_{eq_o}$ and the Thévenin equivalent output resistance of $R_{eq_o} = R_o||R_L$ form a first-order lowpass filter structure given in Figure 12.5 with a cutoff frequency $f_{H_2}$ of

$$\boxed{f_{H_2} = \frac{1}{2\pi\left(R_o||R_L\right)C_{eq_o}}} \tag{12.5.63}$$

with

$$C_{eq_o} = C_{ds} + C_{M_o} + C_{W_o} \tag{12.5.64}$$

where $R_L$ is the load resistance, $R_o$ is the **output resistance** of the amplifier and $C_{M_o}$ is the **Miller output capacitance** given by

$$R_o = R_D || r_{ds}, \tag{12.5.65}$$
$$C_{M_o} = (1 - 1/A_V)\, C_{gd} \cong C_{gd}. \tag{12.5.66}$$

#### 12.5.2.3 Combined Effect of $f_{H_1}$ and $f_{H_2}$

Each cutoff frequency $f_{H_1}$ and $f_{H_2}$ adds an additional 6 dB/octave slope. Overall cutoff frequency $f_H$ is lower than the lowest value of these three cutoff frequencies, i.e.,

$$\boxed{f_H \leq \min(f_{H_1}, f_{H_2})} \tag{12.5.67}$$

When the two cut-off frequencies are a decade apart from each other, than the overall higher cutoff frequency $f_H$ is almost equal to the lowest of the two frequencies, i.e.,

$$f_H \approx \min(f_{H_1}, f_{H_2}) \tag{12.5.68}$$

As Miller input capacitance $C_{M_i}$ has the highest capacitance, almost always $f_{H_1} > f_{H_2}$.

## 12.6 Gain-Bandwidth Product

There is a **Figure of Merit** applied to amplifiers called the **Gain-Bandwidth Product** (**GBP**) that is commonly used to initiate the design process of an amplifier. It provides important information about the relationship between the gain of the amplifier and the expected operating frequency range.

The gain-bandwidth product of an amplifier is **constant**. Thus, gain and bandwidth are inversely proportional, i.e., when we increase the gain, the bandwidth decreases. As a result, we can express the gain-bandwidth product (GBP) as follows

$$\text{GBP} = |A_{v_{mid}}| \times \text{BW} \qquad \ldots \text{BW} = f_H - f_L \tag{12.6.69}$$
$$\cong |A_{v_{mid}}| \times f_H \qquad \ldots f_H \gg f_L \tag{12.6.70}$$

For example, $f_T$ is the gain-bandwidth product for $f_\beta$ as it is the cutoff frequency for $h_{fe} = 1$, i.e., $f_\alpha \cong f_T$.

# Chapter 13

# Multistage (Cascaded) Amplifiers

## 13.1 Cascaded Systems

In cascaded (or multistage) systems output of one amplifier is connected to the input to the next amplifier as shown in Figure 13.1 below.

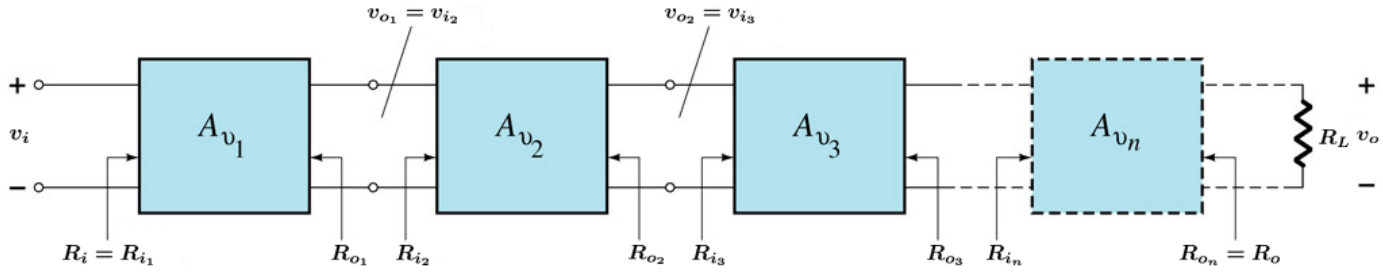



Figure 13.1: A cascaded (or multistage) system.

We would like to represent the overall system as a voltage-gain amplifier as shown in Figure 13.2 below.

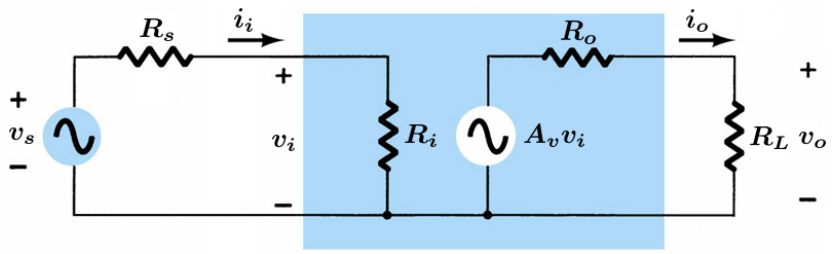



Figure 13.2: Overall representation of the system as a single voltage-gain amplifier.

So, the input resistance $R_i = \frac{v_i}{i_i}$, the output resistance $R_o = \frac{v_{L(\text{open-circuit})}}{i_{L(\text{short-circuit})}}$ and the no-load voltage gain $A_v = \frac{v_{o(\text{no-load})}}{v_i}$ of the whole cascaded system is given by

$$R_i = R_{i_1} \tag{13.1.1}$$

$$R_o = R_{o_n} \tag{13.1.2}$$

$$A_v = A_{v_1} \times \frac{R_{i_2}}{R_{o_1} + R_{i_2}} \times A_{v_2} \times \cdots \times \frac{R_{i_k}}{R_{o_{k-1}} + R_{i_k}} \times A_{v_k} \times \cdots \times \frac{R_{i_n}}{R_{o_{n-1}} + R_{i_n}} \times A_{v_n} \tag{13.1.3}$$

where $R_{i_k}$, $R_{o_k}$ and $A_{v_k}$ are the input resistance, output resistance and no-load gain of the $k$-th stage, respectively, $1 \leq k \leq n$ and $n$ is the maximum number of stages.

**NOTE:** Thus, the input resistance of the current stage acts as a load for the previous stage, or the output resistance of the previous stage acts as a source resistance for the current stage.

Consequently, we can represent the overall no-load voltage-gain $A_v$ in terms of the load-included voltage gains of each stage except the last stage

$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = A_{V_1} \times A_{V_2} \times \cdots A_{V_k} \cdots \times A_{v_n} \tag{13.1.4}$$

where $A_{V_k}$ is the load-included voltage gain of $k$-th stage given by

$$A_{V_k} = A_{v_k}\left(\frac{R_{i_{k+1}}}{R_{o_k} + R_{i_{k+1}}}\right). \tag{13.1.5}$$

Similarly, we can represent the overall no-load voltage-gain $A_v$ in terms of the source-included voltage gains of each stage except the first stage

$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = A_{v_1} \times A_{vs_2} \times \cdots A_{vs_k} \cdots \times A_{vs_n} \tag{13.1.6}$$

where $A_{vs_k}$ is the source-included voltage gain of $k$-th stage given by

$$A_{vs_k} = \left(\frac{R_{i_k}}{R_{o_{k-1}} + R_{i_k}}\right) A_{v_k}. \tag{13.1.7}$$

**Example 13.1:** For the figure below, find the input resistance $R_i$, output resistance $R_o$ and the overall voltage gain $A_{Vs} = v_o/v_s$ of the whole system.

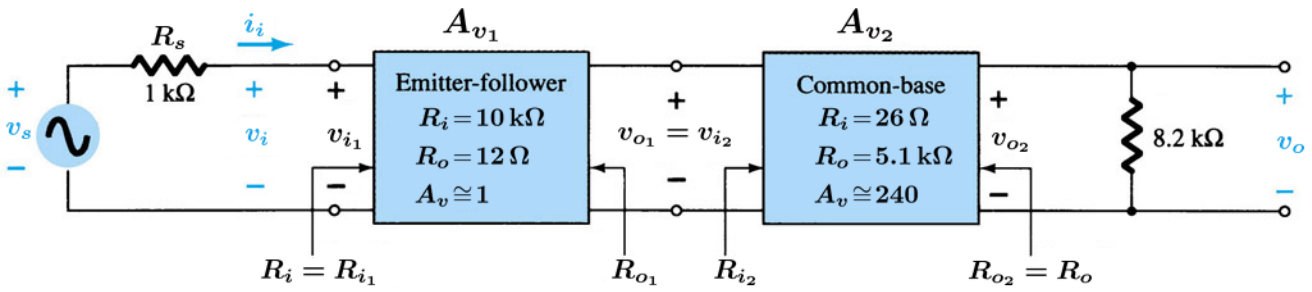



Figure 13.3: A two-stage cascaded system for Example 13.1.

**Solution:** The input resistance $R_i$, output resistance $R_o$ and the total voltage gain $A_{Vs}$ of the overall system are given as follows

$$R_i = R_{i_1} = 10\,\text{k}\Omega, \tag{13.1.8}$$

$$R_o = R_{o_2} = 5.1\,\text{k}\Omega, \tag{13.1.9}$$

$$A_v = A_{v_1}\left(\frac{R_{i_2}}{R_{o_1} + R_{i_2}}\right) A_{v_2} = (1)\left(\frac{26}{12+26}\right)(240) \cong 164.21, \tag{13.1.10}$$

$$A_{Vs} = \left(\frac{R_i}{R_s + R_i}\right) A_v \left(\frac{R_L}{R_o + R_L}\right) = \left(\frac{10k}{1k + 10k}\right)(164.21)\left(\frac{8.2k}{5.1k + 8.2k}\right) \cong 92. \tag{13.1.11}$$

**Homework 13.1:** Calculate the overall voltage gain $A_{Vs}$ by removing the first stagein Figure 13.3, i.e., connecting $R_s$ directly to the second stage. Thus, explain the purpose of the first stage.

## 13.2 AC-Coupled Multistage Amplifiers

In AC-coupled multistage amplifiers, the DC bias circuits are **isolated** from each other by the **coupling capacitors** at the input and output of **each stage**.

Thus,

- The **DC** calculations are **independent** of the cascading.
- The AC calculations for gain and impedance are interdependent.

**Example 13.2:** For the figure below, find the input resistance $R_i$, output resistance $R_o$ and the no-load voltage gain $A_v = v_o/v_i$ of the whole system.

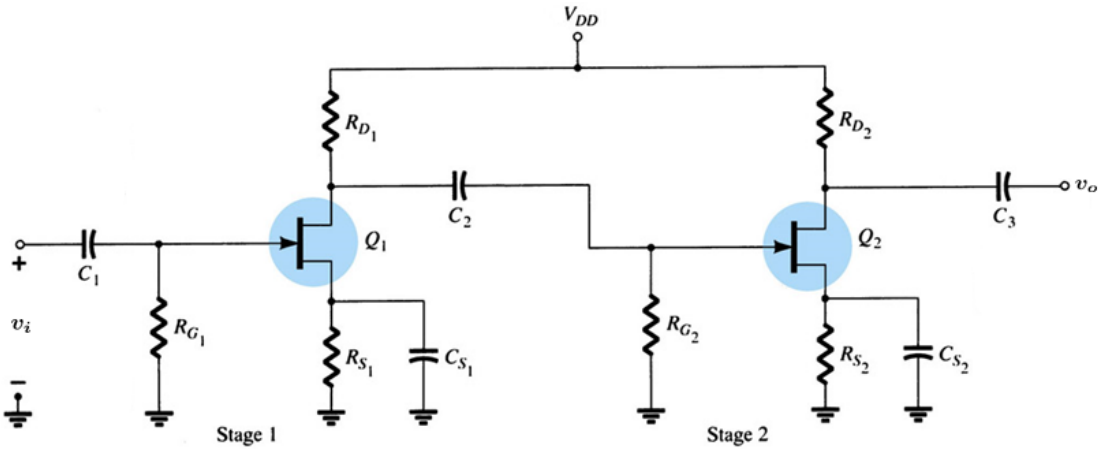



Figure 13.4: An AC-coupled two-stage FET amplifier for Example 13.2.

**Solution:** The input resistance $R_i$, output resistance $R_o$ and the no-load voltage gain $A_v$ of the overall system are given as follows

$$R_i = R_{G_1} \tag{13.2.12}$$
$$R_o = R_{D_2}||r_{ds_2} \tag{13.2.13}$$
$$A_v = \left[-g_{m_2}\left(R_{D_2}||r_{ds_2}\right)\right]\left[-g_{m_1}\left(R_{D_1}||r_{ds_1}||R_{i_2}\right)\right] \tag{13.2.14}$$
$$= g_{m_2}g_{m_1}\left(R_{D_2}||r_{ds_2}\right)\left(R_{D_1}||r_{ds_1}||R_{G_2}\right). \tag{13.2.15}$$

**Example 13.3:** For the figure below, find the input resistance $R_i$, output resistance $R_o$ and the no-load voltage gain $A_v = v_o/v_i$ of the whole system.

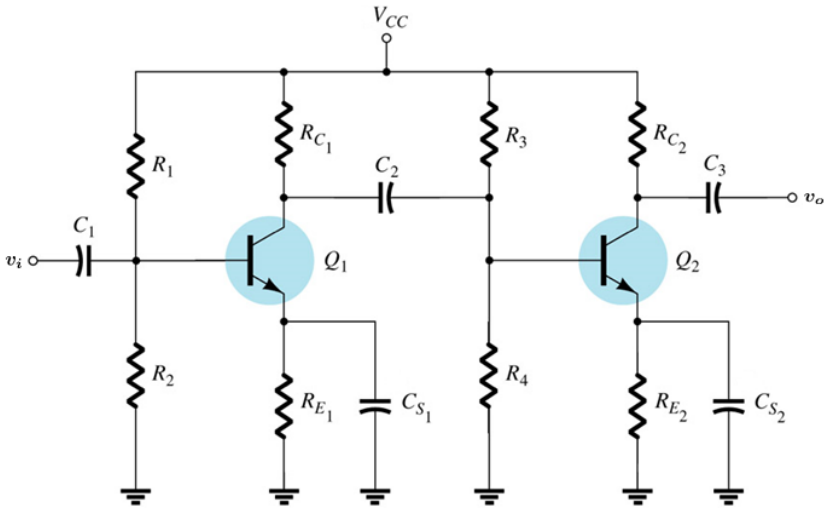



Figure 13.5: An AC-coupled two-stage BJT amplifier for Example 13.3.

**Solution:** The input resistance $R_i$, output resistance $R_o$ and the no-load voltage gain $A_v$ of the overall system are given as follows

$$R_i = R_1||R_2||h_{ie_1} \tag{13.2.16}$$

$$R_o = R_{C_2}||1/h_{oe_2} \tag{13.2.17}$$

$$A_v = \left(-\frac{h_{fe_2}\left(R_{C_2}||1/h_{oe_2}\right)}{h_{ie_2}}\right)\left(-\frac{h_{fe_1}\left(R_{C_1}||1/h_{oe_1}||R_{i_2}\right)}{h_{ie_1}}\right) \tag{13.2.18}$$

$$= \frac{h_{fe_2}h_{fe_1}\left(R_{C_2}||1/h_{oe_2}\right)\left(R_{C_1}||1/h_{oe_1}||R_3||R_4||h_{ie_2}\right)}{h_{ie_2}h_{ie_1}}. \tag{13.2.19}$$

- We can also represent these results in the $r_e$ model as follows

$$R_i = R_1||R_2||\beta_1 r_{e_1} \tag{13.2.20}$$

$$R_o = R_{C_2}||r_{o_2} \tag{13.2.21}$$

$$A_v = \left(\frac{-R_{C_2}||r_{o_2}}{r_{e_2}}\right)\left(-\frac{R_{C_1}||r_{o_1}||R_{i_2}}{r_{e_1}}\right) \tag{13.2.22}$$

$$= \frac{\left(R_{C_2}||r_{o_2}\right)\left(R_{C_1}||r_{o_1}||R_3||R_4||\beta_2 r_{e_2}\right)}{r_{e_2}r_{e_1}}. \tag{13.2.23}$$

**Example 13.4:** For the figure below,

a) Draw AC and DC load lines for both transistors.

b) Calculate the overall voltage gain $A_{Vs} = v_o/v_s$.

c) Find $v_{s(\max)}$ which produces maximum undistorted output voltage.

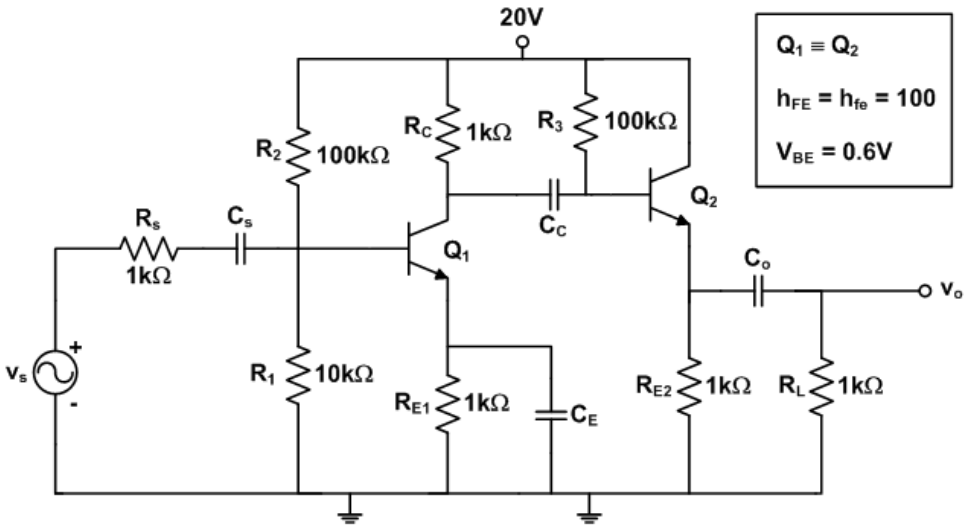



Figure 13.6: An AC-coupled two-stage BJT amplifier for Example 13.4.

**Homework 13.2:** Solve the question given in Example 13.4.

## 13.3 DC-Coupled Multistage Amplifiers

In DC-coupled multistage amplifiers, the DC bias circuits are **not isolated** from each other.

Thus,

- The **DC** calculations are **not independent** of the cascading.
- The AC calculations for gain and impedance are interdependent.

DC-coupled multistage amplifiers are used either to amplify very low frequency signals or to amplify DC signals.

**Example 13.5:** For the figure below,

a) Draw AC and DC load lines for both transistors.

b) Calculate the overall voltage gain $A_{Vs} = v_o/v_s$.

c) Find $v_{s(\max)}$ which produces maximum undistorted output voltage.

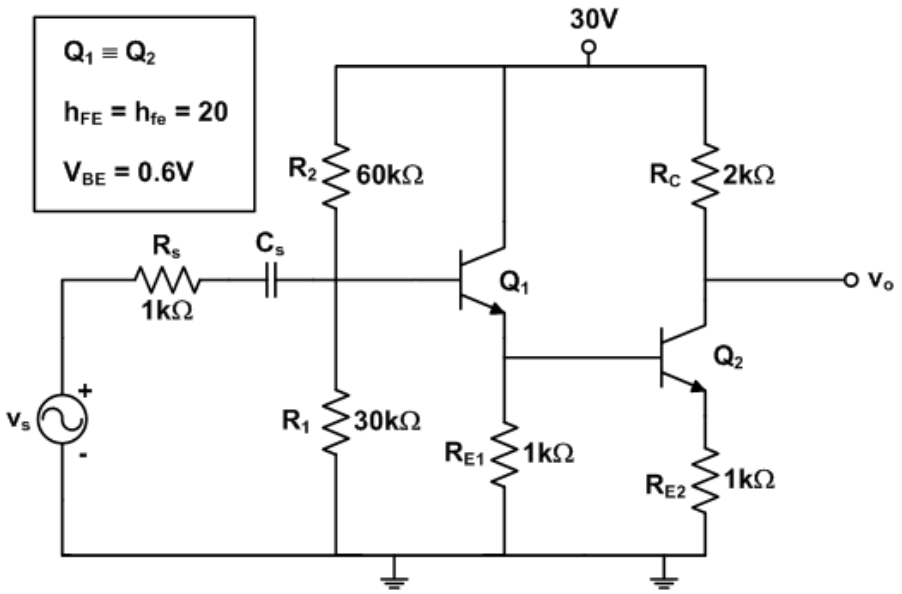



Figure 13.7: A DC-coupled two-stage BJT amplifier for Example 13.5.

**Solution:** a) Let us first start with DC analysis and apply the Thévenin theorem at the base od the first transistor

$$V_{BB_1} = \frac{30k}{30k + 60k}\, 30 = 10\,\text{V} \tag{13.3.24}$$

$$R_{BB_1} = 30k||60k = 20\,\text{k}\Omega \tag{13.3.25}$$

Note that, $I_{E_1} = I_{RE_1} + I_{B_2} \cong I_{RE_1}$ assuming $I_{E_2} \sim I_{E_1}$. So, we can find $I_{RE_1}$ as follows

$$I_{RE_1} \cong \frac{V_{BB_1} - V_{BE_1(ON)}}{R_{E_1} + R_{BB_1}/\left(\beta + 1\right)} = \frac{10 - 0.6}{1k + 20k/21} \cong 4.82\,\text{mA} \tag{13.3.26}$$

Consequently, $I_{CQ_1} \cong I_{RE_1} = 4.82\,\text{mA}$ and $R_{DC_1} \cong R_{E_1} = 1\,\text{k}\Omega$. Also, as $V_{B_2} = V_{E_2} = 4.82\,\text{V}$, we can find $I_{E_2}$ as

$$I_{E_2} = \frac{V_{E_1} - V_{BE_2(ON)}}{R_{E_2}} = \frac{4.82 - 0.6}{1k} \cong 4.22\,\text{mA} \tag{13.3.27}$$

Thus, $I_{E_2} \sim I_{E_1}$ and our assumption holds. Here assuming $\alpha = 20/21 \approx 1$, we obtain $R_{DC_2} \cong R_C + R_{E_2} = 3\,\text{k}\Omega$.

As $R_{ac_1} \cong R_{DC_1} = 1\,\text{k}\Omega$ and $R_{ac_2} = R_{DC_2} = 3\,\text{k}\Omega$, AC and DC load-lines coincide for both transistors, i.e.,

$$v_{CE_1} = V_{CC} - i_{C_1} R_{ac_1} \quad \ldots \text{AC-DC load lines are the same} \quad (13.3.28)$$

$$v_{CE_2} = V_{CC} - i_{C_2} R_{ac_2} \quad \ldots \text{AC-DC load lines are the same} \quad (13.3.29)$$

Consequently, AC (and DC) load-line for the first transistor is shown in Figure 13.8 below

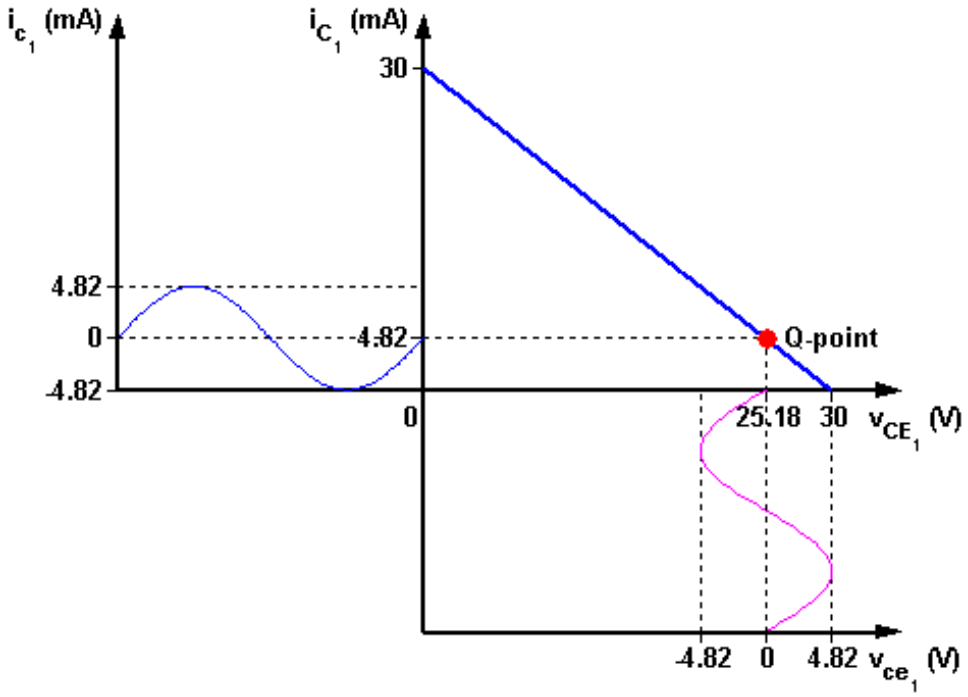



Figure 13.8: AC-DC load-line for the first transistor in Example 13.5.

We can see that maximum undistorted swing for the first transistor is given by

$$v_{CE_{1(\max)}} = \min\left(V_{CEQ_1}, I_{CQ_1} R_{ac_1}\right) = \min\left(25.18, 4.82\right) = 4.82\,\text{V}. \quad (13.3.30)$$

Similarly, AC (and DC) load-line for the second transistor is shown in Figure 13.9 below

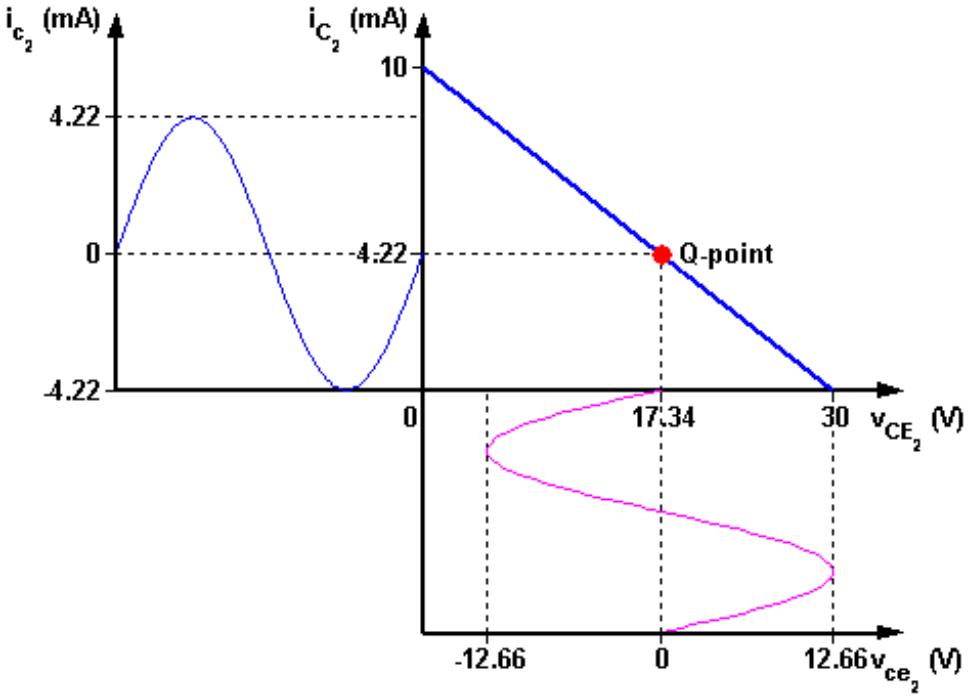



Figure 13.9: AC-DC load-line for the second transistor in Example 13.5.

We can see that maximum undistorted swing for the second transistor is given by

$$v_{CE_{2(\max)}} = \min\left(V_{CEQ_2}, I_{CQ_2} R_{ac_2}\right) = \min\left(17.34, 12.66\right) = 12.66\,\text{V}. \tag{13.3.31}$$

b) Let us first find $h_{ie_1}$, $h_{ie_2}$ and $R_{i_1}$

$$_{ie_1} = h_{fe_1} \frac{\gamma}{I_{CQ_1}} = 20\,\frac{26m}{4.82m} = (20)(5.39) \cong 108\,\Omega \tag{13.3.32}$$

$$h_{ie_2} = \left(h_{fe_2} + 1\right) \frac{\gamma}{I_{CQ_2}} = 21\,\frac{26m}{4.22m} = (21)(6.16) \cong 129\,\Omega \tag{13.3.33}$$

$$R_{i_1} \cong R_1 || R_2 || \left[h_{ie_1} + \left(h_{fe_1} + 1\right) R_{E_1}\right] = 30k || 60k || \left[108 + (21)\,(1k)\right] \cong 10.3\,\text{k}\Omega \tag{13.3.34}$$

Later, let us calculate the no-load gain $A_{v_2} = v_o / v_{i_2} = v_o / v_{o_1}$ of the second stage

$$A_{v_2} = \frac{v_o}{v_{o_1}} = \frac{-h_{fe_2} R_C}{h_{ie_2} + \left(h_{fe_2} + 1\right) R_{E_2}} = \frac{-\,(20)\,(2k)}{129 + (21)\,(1k)} = 1.89 \tag{13.3.35}$$

Now, let us calculate the overall gain $A_{Vs_1} = v_{o_1} / v_s$ of the first stage

$$\begin{aligned} A_{Vs_1} = \frac{v_{o_1}}{v_s} &= \left(\frac{R_{i_1}}{R_s + R_{i_1}}\right)\left(\frac{\left(h_{fe_1} + 1\right) R_{E_1}}{h_{ie_1} + \left(h_{fe_1} + 1\right) R_{E_1}}\right) \\ &= \left(\frac{10.3k}{1k + 10.3k}\right)\left(\frac{(21)\,(1k)}{108 + (21)\,(1k)}\right) \cong 0.91. \end{aligned} \tag{13.3.36}$$

So, the overall voltage gain $A_{Vs}$ is given by

$$A_{Vs} = A_{Vs_1} \times A_{v_2} = (0.91)\,(1.89) = 1.72. \tag{13.3.37}$$

c) From $v_{CE_{1(max)}}$ and $v_{CE_{2(max)}}$ calculated (13.3.30) and (13.3.31) in part (a), and from $A_{v_2}$ and $A_{Vs_1}$ calculated (13.3.35) and (13.3.36) in part (b), we see that the limiting factor comes from the first stage. Because

$$\left(v_{CE_{1(\max)}} < \frac{v_{CE_{2(\max)}}}{A_{v_2}}\right) \Rightarrow \left(4.82 < \frac{12.66}{1.89}\right) \Rightarrow (4.82\,\text{V} < 6.7\,\text{V}) \tag{13.3.38}$$

Consequently,

$$v_{s(\max)} = \frac{v_{CE_{1(\max)}}}{A_{Vs_1}} = \frac{4.82}{0.91} = 5.30\,\text{V}. \tag{13.3.39}$$

**Example 13.6:** For the figure below,

a) Draw AC and DC load lines for both transistors.

b) Calculate the overall voltage gain $A_{Vs} = v_o/v_s$.

c) Find $v_{s(\max)}$ which produces maximum undistorted output voltage.

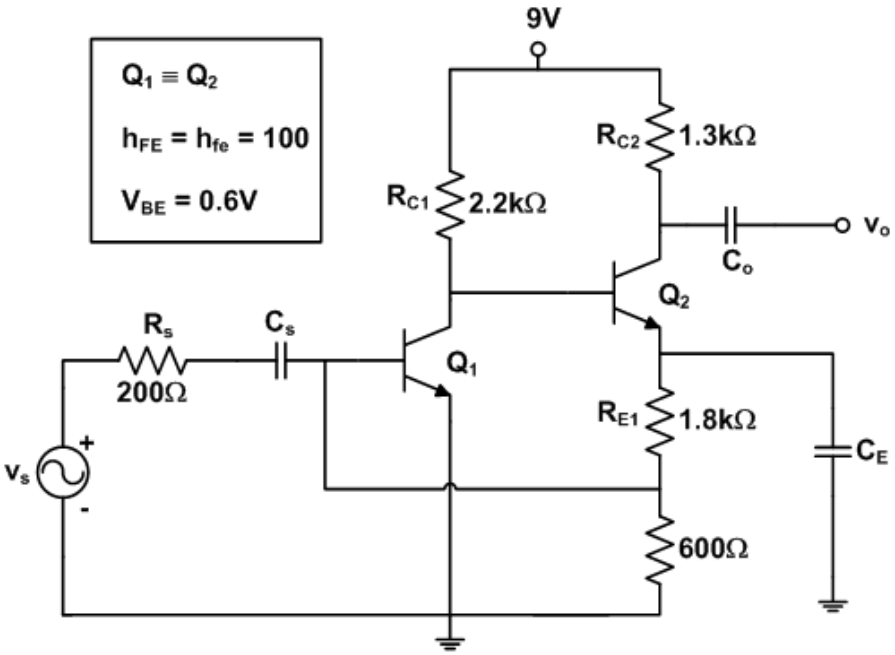



Figure 13.10: A DC-coupled two-stage BJT amplifier for Example 13.6.

**Homework 13.3:** Solve the question given in Example 13.6.

**Example 13.7:** For the figure below,

a) Calculate the overall voltage gain $A_{Vs} = v_o/v_s$.

b) Find the output resistance $R_o$.

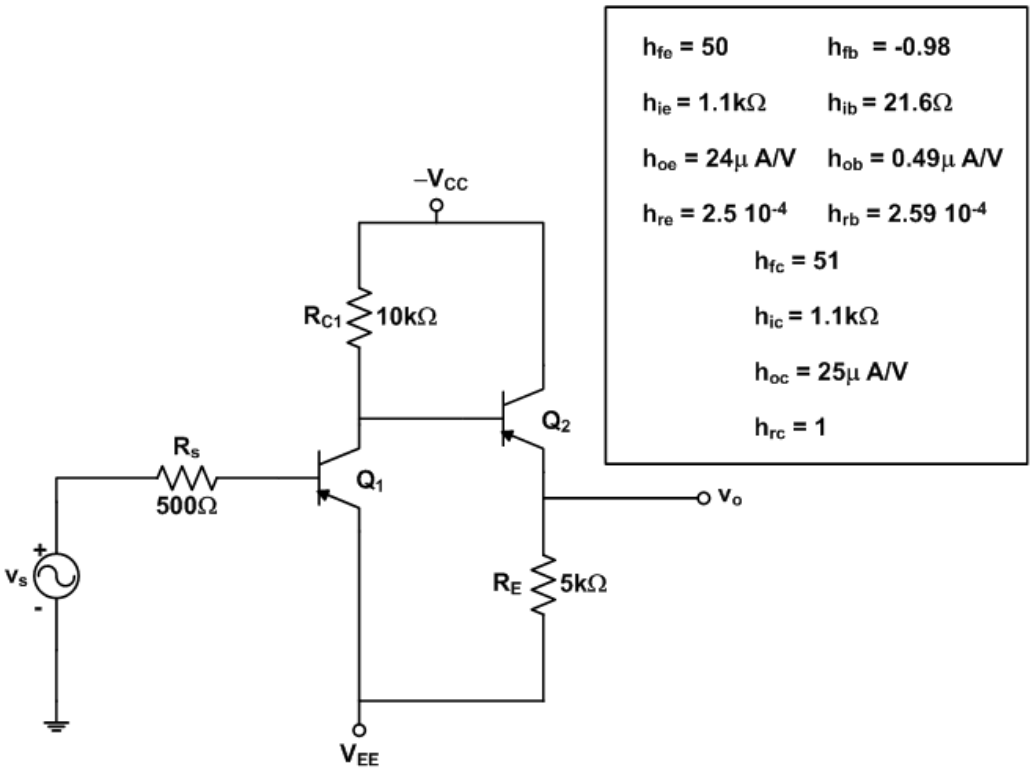



Figure 13.11: A DC-coupled two-stage BJT amplifier for Example 13.7.

**Homework 13.4:** Solve the question given in Example 13.7.

## 13.4 Cascode Amplifier

The cascode configuration is a CE-CB combination, where the collector of the first transistor is connected to the emitter of the second transistor as shown in Figure 13.12 below.

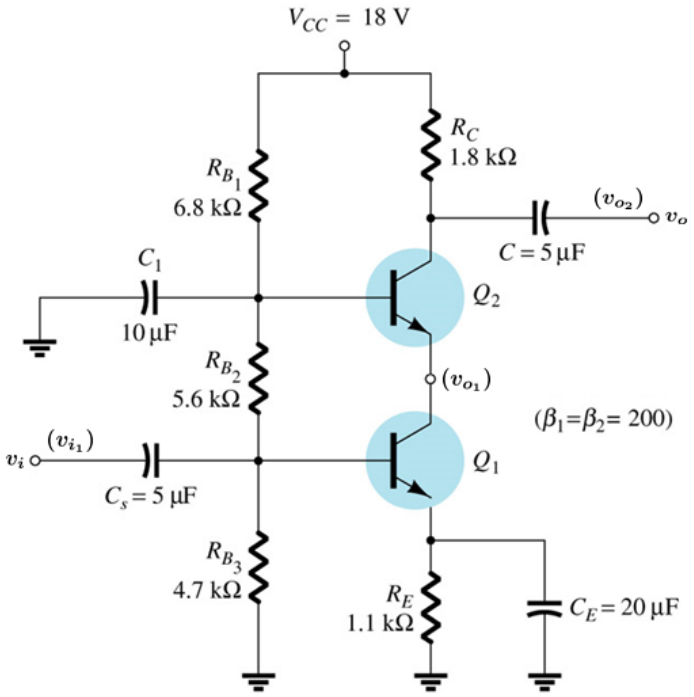



Figure 13.12: A cascode configuration.

The arrangements provide a relatively high-input impedance with low voltage gain for the first CE stage to ensure the input Miller capacitance is at a minimum, whereas the following CB stage provides the high gain.

Therefore, therefore this combination works well in **high frequency** applications.

**Example 13.8:** For the cascode amplifier below, find the input resistance $R_i$, output resistance $R_o$ and the voltage gain $A_v = v_o/v_i$.

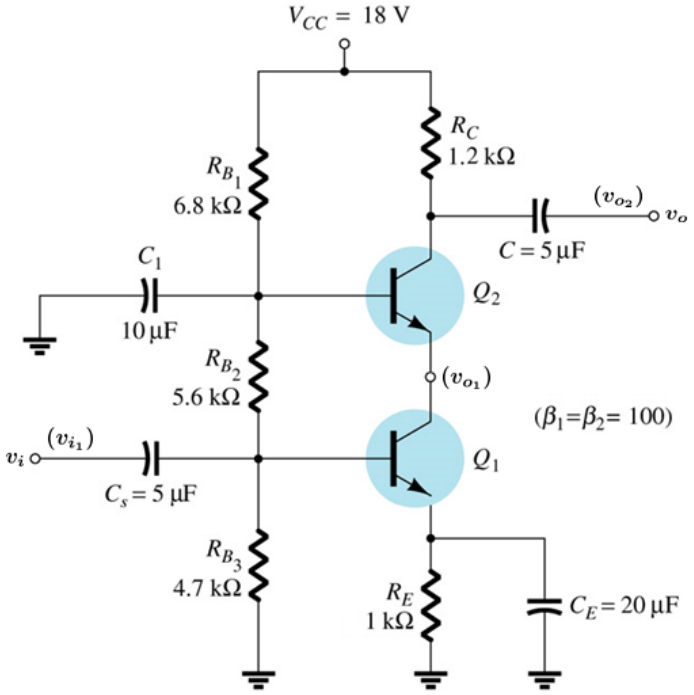



Figure 13.13: A cascode amplifier circuit for Example 13.8.

**Solution:** Let us perform DC analysis first and calculate $I_{EQ_1}$

$$I_{EQ_1} = \frac{V_{B_1} - V_{BE(ON)}}{R_E} \tag{13.4.40}$$

$$\cong \frac{\frac{R_{B_3}}{R_{B_1}+R_{B_2}+R_{B_3}} V_{CC} - V_{BE(ON)}}{R_E} \qquad \text{...ignoring } I_{B_1} \text{ and } I_{B_2} \text{ as } \beta R_E \gg R_{B_3} \tag{13.4.41}$$

$$= \frac{\frac{4.7k}{6.8k+5.6k+4.7k} 18 - 0.7}{1k} = \frac{4.95 - 0.7}{1k} \tag{13.4.42}$$

$$= 4.25\,\text{mA} \tag{13.4.43}$$

$$\tag{13.4.44}$$

As $\alpha = 100/101 \cong 1$, $I_{EQ_1} \cong I_{CQ_1} = I_{EQ_2} \cong I_{CQ_2}$. So, $h_{ie} = h_{ie_1} = h_{ie_2}$ given by

$$h_{ie} = (h_{fe} + 1)\frac{\gamma}{I_{EQ}} = (101)\left(\frac{26m}{4.25m}\right) \cong 618\,\Omega \tag{13.4.45}$$

So, the SSAC equivalent circuit is given in Figure **??** below

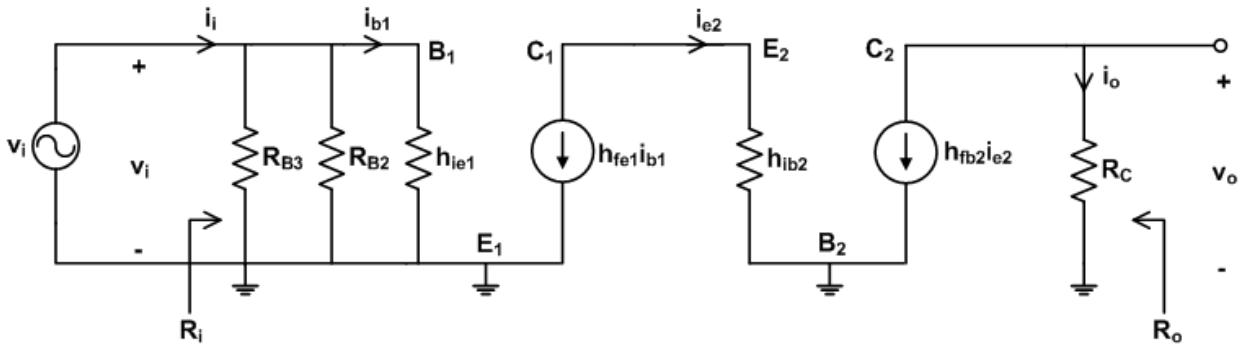



Figure 13.14: SSAC equivalent circuit for Example 13.8.

Thus, we can calculate $R_i$, $R_o$ and $A_v$ as follows

$$R_i = R_{B_3}||R_{B_2}||h_{ie_1} = 4.7k||5.6k||618 \cong 498\,\Omega \tag{13.4.46}$$

$$R_o = R_C = 1.2\,\text{k}\Omega \tag{13.4.47}$$

$$A_v = \left(\frac{v_o}{i_{e_2}}\right)\left(\frac{i_{e_2}}{i_{b_1}}\right)\left(\frac{i_{b_1}}{v_i}\right) \tag{13.4.48}$$

$$= (-h_{fb_2}R_C)\,(-h_{fe_1})\left(\frac{1}{h_{ie_1}}\right) \qquad \ldots h_{fb} = -1 \tag{13.4.49}$$

$$= -\frac{(100)\,(1.2k)}{0.618k} = -194. \tag{13.4.50}$$

**Homework 13.5:** Show that the voltage gain $A_{V_1} = v_{o_1}/v_i = -1$ for the first stage of the amplifier. Consequently, comment on the Miller effect.

## 13.5 Darlington Pair

A very popular connection of *npn* two bipolar junction transistors for operation as one **superbeta** *npn* transistor is the Darlington connection shown in Figure 13.15 below.

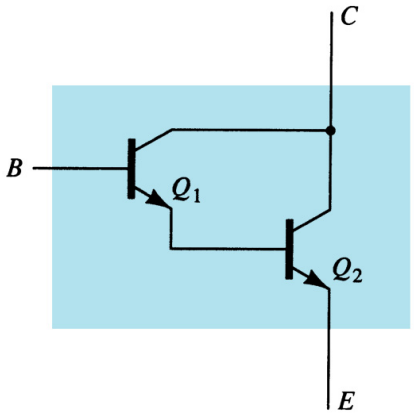



Figure 13.15: Darlington combination.

The main feature of the Darlington connection is that the composite transistor as shown in Figure 13.16 below acts as a single unit with a current gain that is the product of the current gains of the individual transistors.

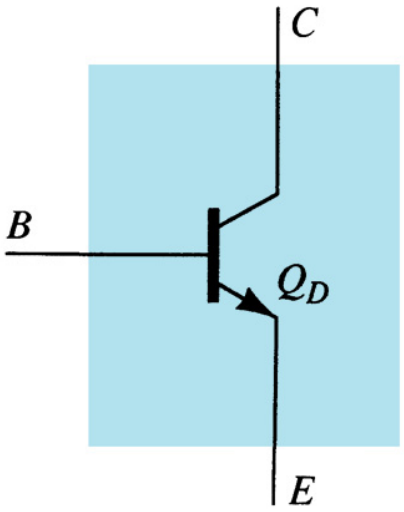



Figure 13.16: Single *npn* transistor representation of the Darlington pair.

Consequently, current gain $\beta_D$ and base-emitter turn-on voltage $V_{BE_D(ON)}$ are given as follows

$$\beta_D = \beta_1\beta_2 + \beta_1 + \beta_2 \approx \beta_1\beta_2 \tag{13.5.51}$$

$$V_{BE_D(ON)} = 2V_{BE(ON)} \tag{13.5.52}$$

Such that $I_C = \beta_D I_B$ and $I_E = (\beta_D + 1)\, I_B$ when both transistors are in the forward active mode.

**Homework 13.6:** Show that expressions (13.5.51) and (13.5.52) above for $\beta_D$ and $V_{BE_D(ON)}$ are correct.

## 13.6 Feedback Pair

The feedback pair connection shown in Figure 13.17 below is a two-transistor circuit that operates like the Darlington circuit.

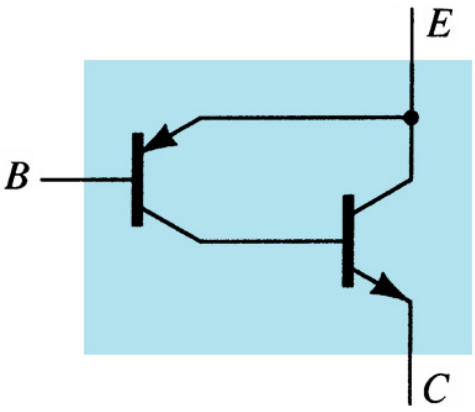



Figure 13.17: Feedback pair connection.

Notice that the feedback pair uses a *pnp* transistor driving an *npn* transistor, the two devices acting effectively much like one *pnp* transistor as shown in Figure 13.18 below. As with a Darlington connection, the feedback pair also provides a very high current gain.

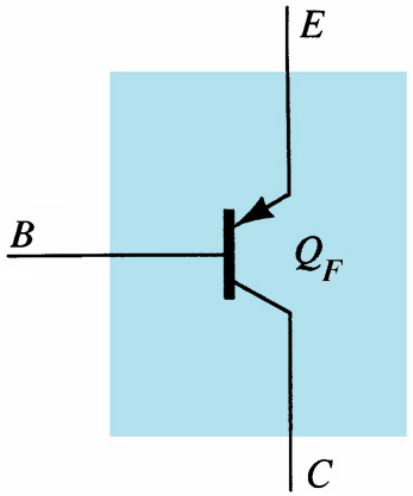



Figure 13.18: Single *pnp* transistor representation of the feedback pair.

Consequently, current gain $\beta_F$ and emitter-base turn-on voltage $V_{BE_F(ON)}$ are given as follows

$$\beta_F = \beta_1\beta_2 + \beta_1 \approx \beta_1\beta_2 \tag{13.6.53}$$

$$V_{BE_F(ON)} = V_{BE(ON)} \tag{13.6.54}$$

Such that $I_C = \beta_F I_B$ and $I_E = (\beta_F + 1)\, I_B$ when both transistors are in the forward active mode.

**Homework 13.7:** Show that expressions (13.6.53) and (13.6.54) above for $\beta_F$ and $V_{BE_F(ON)}$ are correct.