TRANSISTORS

The first transistor was investigated in 1947. The name of the transistor comes from transfer resistor. The transistor transfers the current from small resistance to high resistance and thus provides amplification. The two main transistors:

I. BJT : Bipolar Junction Transistors
II. FET : Field Effect Transistors

I. BJT Structure

BJT is a three terminal device which is made up of n and p type materials as:

\[ \text{E} \rightarrow \text{PnP} \rightarrow \text{C} \]

\[ \text{E} \rightarrow \text{nPN} \rightarrow \text{C} \]

- pnp type BJT
- npn type BJT

E: Emitter
B: Base (thin region with respect to side regions)
C: Collector

Transistor Operation:

Transistors can be used in normal mode, in saturation mode and in cut-off mode. In this part we will analyse the normal mode operation of the transistor (pnp type).
Due to the forward biasing of the $V_{EB}$ potential, majority carriers ($+$) diffuse into the n-type material. n-type material is very thin and thus has high resistance. Thus, very small number of these carriers flow through base terminal. The magnitude of base current is on the order of microamperes. The remaining large number of carriers will diffuse across the p-type material due to $V_{CB}$ potential to form the collector current. According to KCL:

$$I_E = I_C + I_B$$

can be written.

However, collector current is composed of two components due to the majority and minority carriers. The minority current component is called as "leakage current" and shown with $I_{Co}$. ($I_C$ current when emitter terminal is open). Generally $I_C$ is on the order of milliampers and $I_{Co}$ in micro or nanoamperes. However $I_{Co}$ highly depends on temperature and for wide temperature range applications.
Thus:

\[ I_c = I_{c,\text{majority}} + I_{c,\text{minority}} \]

**Amplification by Transistor:**

Transistor circuits can be used to amplify input signals.

Assume that \( I_c \approx I_E \) (\( I_E = I_c + I_B \) small)

\[ V_L = R_L \cdot I_E = 10V \]

\[ \Rightarrow \frac{V_L}{V_i} = \frac{10V}{200\,\text{mV}} = 50 \Rightarrow \text{means that } V_i \text{ is amplified by 50 at the output.} \]

For a given transistor:

\[ \alpha = \frac{\Delta I_c}{\Delta I_E} \approx \frac{I_c}{I_E} \quad 0.9 < \alpha < 0.98 \]

\[ I_E = I_c + I_B \Rightarrow I_B = -(I_c + I_E) \]

\[ I_c = \frac{I_{C0}}{1-\alpha} + \frac{\alpha I_B}{1-\alpha} \]

if \( I_B = 0 \Rightarrow I_c = I_{CE0} = \frac{I_{C0}}{1-\alpha} \quad I_B = 0 \]
and forward current amplification factor $\beta$:

\[ \beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{and} \quad \beta \approx \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha} \]

Symbols of the Transistor:

- pnp type
- nnp type

Arrow direction indicates the pnp or nnp type.

I. Common-Base Transistor Circuit:

- pnp
- nnp

In common base configuration base is the common point.

For this case:

\[ V_{EB} = 0.7V \]
Saturation region means that very high $I_c$ current due to small change in the $V_{cb}$ potential. ($I_c = I_{c\text{-max}}$, small $V_{cb}$).

Cut-off region means that negligible collector current ($I_c \approx 0$).

The remaining region is called as active region. For amplification purpose transistor is used in this region.

Common base characteristics of the 'npn' type transistor can be directly obtained by changing the current directions and voltage polarities.

II. Common-Emitter Circuit:

- *pnp type* -

- *npn type* -

Emitter is the common point of the circuit. Main transistor characteristics for pnp type:

- $I_c$ ($\text{mA}$)

- $I_\text{c}$ ($\mu\text{A}$) $= 20\mu\text{A}$

- $I_\text{c}$ ($\mu\text{A}$) $= 10\mu\text{A}$

- $I_\text{c}$ ($\mu\text{A}$) $= 5\mu\text{A}$

- $V_{be} = 0$

- $V_{o} = 0.7\text{V}$

$V_{be} \approx 0.7\text{V}$ can be taken.

- *npn characteristics are in similar form* -

-45- (Common-Collector can be similarly)
DC Biasing of the BJT

BJT's can be used in normal mode for amplification purposes and in saturation or cut-off modes for logic circuit applications. For normal mode (linear region) operation of a BJT, it must be properly biased to set the desired operating voltages and currents in the circuit. Operating point of the BJT in normal mode is generally chosen approximately the mid point of the device characteristic as:

\[ I_{\text{max}} \times V_{\text{max}} < P_{\text{max}} \]

condition must be considered.

And for maximum swing opportunity, middle point of the normal mode region can be safely chosen as the operating point \((I_q, V_q)\).

Examples of DC Biasing Circuits:

I.) Common Base DC Biasing:

\[ V_{\text{EE}} - I_{E} R_{E} - V_{EB} = 0 \]

\[ V_{EB} \approx 0.7 \text{ can be ignored. Thus} \]

\[ I_{E} \approx \frac{V_{EE}}{R_{E}} \]
Output loop: \( V_{cc} - I_c R_c - V_{ce} = 0 \); \( I_c = \beta I_B \leq \beta \frac{V_{cc}}{R_B} \)

\[ \Rightarrow V_{ce} = -V_{cc} + I_c R_c \]

**Common Collector DC Biasing**: can be similarly analysed with the common emitter case. This type of connection has high input and low output impedance thus suitable for impedance balancing.

**Graphical DC Biasing Analysis**:

Until this point we have determined dc currents and voltages on transistor mathematically. In this part we will see how the same results can be obtained graphically. For the graphical analysis load line must be obtained and then intersected with the current-voltage \((I_c, V_{ce})\) characteristic of the transistor.
The intersection point of load line and $I_B$ curve gives the operating point (or quiescent point) of the circuit as:

Load line eqn of CE case from output loop:

$$I_C = -\frac{1}{R_c} V_{CE} + \frac{V_{CC}}{R_c} = mx + n$$

can be obtained.

$$I_{C_{\text{max}}} = \frac{V_{CC}}{R_c}$$

$$V_{CE_{\text{max}}} = V_{CC}$$

Q point gives the dc $I_C$ current and $V_{CE}$ voltage as $I_{EQ}$ and $V_{CEQ}$.

**Notes:**

1.) If $I_B$ current is increased, Q point gets closer to the vertical axis. In such a case $I_C$ current is high and $V_{CE}$ is very small. This case ($V_{CE} < V_{CE\text{-sat}} \leq 0.2V$, and $I_C > I_C^*$) is called as "saturation" of the transistor.

Saturation can be achieved by forward biasing of the base junctions. In saturation transistor seems to be the short circuit.

2.) If $I_B$ current is reduced nearly to zero ($I_B \to 0$) then $I_C \to 0$ and $V_{CE} \to V_{CE\text{-max}} = V_{CC}$, and Q point gets closer to the horizontal axis. This case is called as "cut-off" mode of transistor. Cut-off can be achieved by reverse biasing of the base junctions. In cut-off transistor be OFF.
For normal (or active) mode operation of the transistor (one of the junctions is forward and another is reverse biased) which is required for amplifier circuits, a point must be chosen near to the mid point of the characteristics. Otherwise distortion at the output can be observed as:

Additional $I_\text{B}$ input in AC form.

Clipped $V_{CE}$ waveform due to small $I_\text{E}$, ($V_{CE}$ cannot exceed $V_{cc}$ and thus clipped!) :: cut-off

Q.E: A point near to vertical axis:

$I_\text{C}$ output is clipped due to $I_\text{B}$ current corresponding to saturation region ($I_\text{B} > \theta$)
Ex: For the given circuit find:

a) DC load line eqn. and Q point.

b) $V_{CE}$, $I_c$, $I_{cR_C}$ and $I_E$ graphically.

**Load line eqn:**

\[
\begin{align*}
I_c &= 0 \Rightarrow V_{CE} = V_{cc} = 15 \text{ V} \\
V_{CE} &= 0 \Rightarrow I_c = \frac{V_{cc}}{R_c} = \frac{15}{3} = 5 \text{ mA}
\end{align*}
\]

\[I_B = \frac{V_{cc}}{R_B} = \frac{15}{100} = 150 \mu\text{A}\]

(drawn on the given $V_{ce}$- $I_c$ graph)

From Q point $V_{CE} = 7 \text{ V}$ \Rightarrow $I_{cR_C} = V_{cc} - V_{CE}$

\[= 15 - 7 = 8\]

\[I_c = \frac{8 \text{ V}}{3 \text{ K}} = 2.6 \text{ mA} \approx I_E\]

**Design of DC Biasing Circuits:**

Until now, we have analysed given circuits and determined voltages and currents. In this part we will deal with the design of the biasing circuit elements in order to obtain desired Q point operation.

A simple design example:
\[ I_{CQ} = \beta I_{EQ} + (1+\beta) I_{EQ} \]
\[ = \beta I_{EQ} = 100 \times 0.08 \text{ mA} = 8 \text{ mA} \]

From output circuit:
\[ V_{CEQ} = 10 - 1 \text{ k} \cdot 8 \text{ mA} \]
\[ = 2 \text{ V} > V_{CE\text{-sat}} \]

For this selection \((V_{BB} = 1.4 \text{ V})\), \(V_{CEQ} > V_{CE\text{-sat}}\). Thus transistor is not in saturation!

b) Now, let us choose \(V_{BB} = 10 \text{ V}\):
\[ I_{EQ} = \frac{10 - 0.6}{10 \text{ k}} = 0.94 \text{ mA} \]
\[ I_{CQ} = 100 \times 0.94 \text{ mA} = 94 \text{ mA} \]
\[ V_{CEQ} = 10 - 1 \text{ k} \cdot 94 \text{ mA} = -84 \text{ V} < V_{CE\text{-sat}} \]

Thus, for this case transistor is in saturation. \((-\text{ve} V_{CE}\text{ means saturation for npn type BJT!})\). Saturation can be achieved by forward biasing of the both junctions. After transistor goes into saturation, then
\[ I_c < \beta I_b \] \((i.e. I_c \neq \beta I_b)\)

means that we can not increase \(I_c\) as much as we desire after saturation is started.

Note: For the \(V_{BB} = 1.4\) case if \(I_c\) current was obtained as \(I_c \approx 0\) (but not), transistor was said to be in cut-off. But \(I_c = 8 \text{ mA} \neq 0\). Thus transistor is in active region!
Ex: For the given circuit $\beta = 75$, $V_{CE} = 10\,V$, $I_C = 10\,mA$ and $V_{CE\text{-max}} = 40\,V$. Find $R_b$ and $R_c$ for desired Q point operation.

![Circuit diagram]

Capacitors are open for dc case!

From output circuit: $I_{CQ}R_c + V_{CEQ} = V_{CC}$

$$R_c = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{20 - 10\,V}{10\,mA} = 1\,K$$

to find $R_b$ : $I_B = \frac{I_C}{\beta} = \frac{10\,mA}{75} = 133\,\mu A$

from input circuit: $R_b = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 - 0.7}{133\,\mu A} = 145k$

Ex: Analyse the given circuit and indicate whether transistor is in saturation or not.

![Circuit diagram]

$I_C = 0$

$V_o = 0.6\,V$ ($= V_{BE}$)

$\beta = 100$

$V_{CE\text{-sat}} = 0.1\,V$

$1.4\,V \leq V_{BB} \leq 10\,V$

a) Sln: Let us choose $V_{BB} = 1.4\,V$, Thus from input circuit:

$$I_{BQ} = \frac{1.4 - 0.6}{10\,k} = 0.08\,mA$$
Assume a self biased circuit:

\[ I_{BQ} = \frac{V_{cc} - V_{BE}}{R_B} \]

\[ I_C = \beta I_B + (1+\beta) I_{CQ} \]

\[ V_{CE} = V_{cc} - I_C R_C \]

If \( T \uparrow \); \( V_{BE} \uparrow \), \( I_{CQ} \uparrow \), \( \beta \uparrow \), \( \Rightarrow I_C \uparrow \)

\( I_C \) depends on temperature. In order to decrease stability of \( I_C \) on temperature another bias circuit can be used as an alternative as:

\[ V_{BB} = \frac{R_2}{R_2 + R_1} \cdot V_{cc} \quad \text{\textit{j} Thévenin voltage} \]

\[ R_B = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2} \]

\textbf{Input loop:} \(- V_{BB} + V_{BE} + I_{BQ} R_B + R_C (I_{BQ} + I_{CQ}) = 0\)

and \( I_{CQ} = \beta I_{BQ} + (1+\beta) I_{CQ} \)
DC Bias Stability of BJT Amplifiers:

BJT Amplifier circuits are sensitive to the temperature changes due to the variation of $\beta$, $I_{CO}$, and $V_{BE}$ with temperature. In order to decrease sensitivity some stabilisation techniques have been used.

Stability factors as the measure of sensitivity can be defined as:

$$S_{I_{CO}} = \frac{\delta I_c}{\delta I_{CO}}$$
$$S_{\beta} = \frac{\delta I_c}{\delta \beta}$$
$$S_{V_{BE}} = \frac{\delta I_c}{\delta V_{BE}}$$

due to $I_c = (I_{CO}, \beta, V_{BE}, R_B, R_c, R_E, V_{cc} \ldots)$ and thus:

$$\delta I_c = \delta I_{CO} \left( \frac{\delta I_c}{\delta I_{CO}} \right) + \delta \beta \left( \frac{\delta I_c}{\delta \beta} \right) +$$
$$+ \delta V_{BE} \left( \frac{\delta I_c}{\delta V_{BE}} \right) + \ldots$$

which can be thought of the measure of how sensitive collector current is to changes in a parameter value.

For a silicon transistor:

<table>
<thead>
<tr>
<th>$S_i$</th>
<th>$^\circ C$</th>
<th>-65</th>
<th>25</th>
<th>175</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CO}$ (mA)</td>
<td>$1.75 \times 10^{-3}$</td>
<td>1</td>
<td>3300</td>
<td></td>
</tr>
<tr>
<td>$\beta$</td>
<td>25</td>
<td>55</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>$V_{BE}$</td>
<td>0.78</td>
<td>0.6</td>
<td>0.225</td>
<td></td>
</tr>
</tbody>
</table>

Ideally $S$ factors must be zero but they never!
\[ \Rightarrow I_{Bq} = \frac{I_{Cq} - (1+\beta)I_{C0}}{\beta} \]

Insert \( I_{Bq} \) into the above eqn:

\[ \Rightarrow I_{Cq} = \beta \frac{V_{BB} - V_{BE}}{R_E + R_E} + \frac{R_E + R_B}{R_E + (1+\beta)R_E} I_{C0} \quad (\ast) \]

Therefore, stability factors can be obtained from (\ast):

\[ S_{I_{C0}} = \frac{\delta I_{Cq}}{\delta I_{C0}} = (1+\beta) \frac{R_E + R_B}{R_E + (1+\beta)R_E} \]

\[ S_{V_{BE}} = \frac{\delta I_{Cq}}{\delta V_{BE}} = -\frac{\beta}{R_E + (1+\beta)R_E} \]

and \( S_{\beta} = \frac{\delta I_{Cq}}{\delta \beta} \). We may use this for to determine \( S_{\beta} \), for single \( \beta \) value.

If we know \( \beta_{\text{min}} < \beta < \beta_{\text{max}} \) we may use:

\[ S_{\beta} = \frac{\delta I_{Cq}}{\delta \beta} \propto \frac{\Delta I_{Cq}}{\Delta \beta} \]

Thus;

\[ I_{Cq_{\text{max}}} = \beta_{\text{max}} \frac{V_{BB} - V_{BE}}{R_E + (1+\beta_{\text{max}})R_E} \]

\[ I_{Cq_{\text{min}}} = \beta_{\text{min}} \frac{V_{BB} - V_{BE}}{R_E + (1+\beta_{\text{min}})R_E} \]
\[
\frac{I_{CQ_{\text{max}}} - I_{CQ_{\text{min}}}}{I_{CQ_{\text{min}}}} = \frac{\beta_{\text{max}} - \beta_{\text{min}}}{\beta_{\text{min}}} \cdot \frac{R_E + R_e}{R_e + (1 + \beta_{\text{max}})R_e}
\]

\[
\frac{\Delta I_{CQ}}{I_{CQ_{\text{min}}}} = \frac{\Delta \beta}{\beta_{\text{min}}} \cdot \frac{R_E + R_e}{R_e + (1 + \beta_{\text{max}})R_e}
\]

\[
\frac{\Delta I_{CQ}}{I_{CQ_{\text{min}}}} = S = \frac{V_{BE} - V_{BE}}{\Delta \beta} \cdot \frac{R_E + R_e}{R_e + (1 + \beta_{\text{min}})R_e} = \frac{V_{BE} - V_{BE}}{R_e + (1 + \beta_{\text{max}})R_e}
\]

\[
\Delta I_{CQ} = S \beta = \frac{V_{BE} - V_{BE}}{\Delta \beta} \cdot \frac{R_E + R_e}{R_e + (1 + \beta_{\text{min}})R_e} = \frac{V_{BE} - V_{BE}}{I_{CQ_{\text{min}}} / \beta_{\text{min}}}
\]

At this point we can make some approximation on \( S \) factors as:

1.) If \( \beta + 1 \approx \beta \) and \( R_E \gg (1 + \beta) R_E \)

\[
S_{I_CQ} = \beta \frac{R_E + R_e}{R_e + (1 + \beta) R_e} \approx \beta (1 + \frac{R_e}{R_E})
\]

2.) If \((1 + \beta) R_E \gg R_E \Rightarrow S_{I_CQ} \) is minimal

and \( S_{I_CQ} = \beta \frac{R_E + R_e}{(1 + \beta) R_E} \approx 1 + \frac{R_e}{R_E} \)

3.) If \( R_E \gg (1 + \beta) R_E \); \( S_{V_{BE}} \approx -\frac{\beta}{R_E} \)

4.) If \((1 + \beta) R_E \gg R_E \); \( I_{CQ} = \frac{V_{BE} - V_{BE}}{R_E} + \frac{R_E + R_e}{R_E} I_{CQ} \)

5.) If \( V_{BE} \gg V_{BE} \); \( I_{CQ} \approx \frac{V_{BE}}{R_E} + (\frac{\gamma}{\gamma}) I_{CQ} \approx \frac{V_{BE}}{R_E} \)

-56-
For the given structure (named as B independent cat),
Re resistor is called as feedback resistor, and type of feedback is current feedback:

\[ \frac{R_e}{R_1} \]

Re is both in input loop and output loop and thus provides feedback and improved stability.

Assume:

\[ T \uparrow \Rightarrow I_c \uparrow \Rightarrow V_e = I_c R_e \uparrow \]

\[ (V_{BE} = V_B - V_e) \cap I_B \cap I_c = \beta I_B \cap \]

Thus, increase in \( I_c \) due to temperature can be compensated by including \( R_e \) resistor, resulting with more stable circuit operation.

Another type of feedback called as "Voltage feedback" can also be used to increase stability as:

\[ R_f \text{ is called as feedback resistor and behaves as; } \]

\[ T \uparrow \Rightarrow I_c \Rightarrow V_c \Rightarrow I_B \]

\[ I_B \cap \Rightarrow I_c \cap \]

Thus, increase in \( I_c \) due to temperature can be compensated as a result of feeding back of the \( V_c \) to the input loop by means of \( R_f \) resistor. In this case feedback is "Voltage feedback" and \( R_f \) is feedback resistor.
Analysis of the voltage feedback circuit:

Input loop: \( V_{cc} = R_c \cdot I'_c + R_f \cdot I_B + V_{be} \)

\( I'_c = I_c + I_B \) and we know that \( I_c = \beta I_B + (1+\beta) I_C \)

\( \Rightarrow I_B = \frac{I_c - (1+\beta) I_C}{\beta} \)

If \((\beta+1) \approx \beta\) and \((1+\beta) R_c \gg R_f \Rightarrow \)

\[
I_{ca} = \frac{V_{cc} - V_{be}}{R_c} + \frac{R_c + R_f}{R_c} \cdot I_C
\]

If \(I_{ca} \approx 0\) and \(V_{cc} \gg V_{be} \Rightarrow I_{ca} \approx \frac{V_{cc}}{R_c} \)

Assume \(I' \approx I_c\), from output loop:

\[-V_{cc} + I_c \cdot R_c + V_{ce} = 0\]

\(\Rightarrow V_{ce} \approx V_{cc} - I_c \cdot R_c \approx V_{cc} - \frac{V_{cc}}{R_c} \cdot R_c \approx 0\)

\(V_{ce} = 0\) means that if \(R_c(1+\beta) \gg R_f\) is chosen, amount of feedback increases and makes output nearly zero. Therefore this type of circuit must be designed carefully for stabilisation purpose. (Output \(\approx 0\) means reduced gain even though stabilisation increases.)

If \((\beta+1) R_c \gg R_f\)

\[S_{I(Co)} = 1 + \frac{R_f}{R_c}\] can be obtained for this circuit.
In some applications voltage and current feedbacks can be combined as:

For the given circuit if \( V_{cc} = 20 \text{V} \), \( R_c = 800 \Omega \), \( R_f = 50 \text{K} \), \( R_e = 200 \Omega \), find \( I_{c_0} \), and conditions to make \( S_B \), \( S_{v_{be}} \) and \( S_{I_{c_0}} \) minimum.

Assume that for \( 50 \leq B \leq 200 \):

<table>
<thead>
<tr>
<th></th>
<th>25°C</th>
<th>155°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{c_0} ) (μA)</td>
<td>0.1</td>
<td>0.11</td>
</tr>
<tr>
<td>( V_{be} ) (mv)</td>
<td>600</td>
<td>350</td>
</tr>
</tbody>
</table>

\[
\Delta I_{c_0} = I_{c_0_{max}} - I_{c_0_{min}}
\]

Sin:
It can be shown that:

\[
S_{I_{c_0}} = (1 + B) \frac{R_c + R_e + R_f}{(1 + B)(R_c + R_f) + R_e}
\]

\[
S_{v_{be}} = -\frac{\beta}{(1 + \beta)(R_c + R_e) + R_f}
\]

\[
S_B = \frac{I_{c_0_{min}}(R_c + R_e + R_f)}{\beta_{min} \left[ (1 + \beta_{max})(R_c + R_e) + R_f \right]}
\]

\[
\Rightarrow I_{c_0_{min}} \approx 9.6 \text{ mA (using } \beta_{min} \text{ value)}
\]

\[
S_{I_{c_0}} = 25.75, \quad S_{v_{be}} = -0.495 \cdot 10^{-3}, \quad S_B = 0.089 \cdot 10^{-3}
\]

-59-
and; \[ \Delta I_c = S I_{c0} \Delta I_{co} + S_{\beta} \Delta \beta + S_{V_{BE}} \Delta V_{BE} \]

using the given table;

\[ \Delta I_{co} = 0.01 \mu A \]
\[ \Delta \beta = 150 \]
\[ \Delta V_{BE} = 250 \text{ mV} \]
\[ \Delta I_c = 5.974 \text{ mA} \text{ can be obtained.} \]

\[ I_{co \ max} = I_{cq \ min} + \Delta I_{cq} = 9.6 + 5.974 \]
\[ \approx 15.6 \text{ mA} \]

**Ex:** In order to obtain stable dc characteristics in the given circuit find \( R_1 \) and \( R_2 \).

\[ V_{cc} = 9V \]
\[ R_c = 1k \]
\[ R_e = 200\Omega \]
\[ \beta = 100 \]
\[ I_{co} = 0 \]
\[ V_{CEq} = 4.5V \]
\[ I_{cq} = 3.75 \text{ mA} \]

\[ V_{BB} = \frac{V_{cc} \cdot R_2}{R_1 + R_2} \]
\[ R_B = R_1 \| R_2 \]

If we choose \((1+\beta)R_e \gg R_B\) circuit becomes stable!

\((I_{cq} \text{ does not change much!})\)

For; \( R_B = (1+\beta)R_e \)

\[ (1+\beta) \cdot 200 \cdot 0.1 = R_B = 2k = R_1 \| R_2 \]

\[-V_{BB} + V_{R_B} + V_o + 200 I_{cq} = 0 \Rightarrow V_{BB} = V_o + 200 I_{cq} \]
\[ R_B = 2K = R_1/R_2 \]  \hspace{1em} (1)

\[ V_{BB} = V_{cc} \frac{R_2}{R_2} = V_0 + 200 \text{ ICQ} \]  \hspace{1em} (-V_{BB} + V_{RB} + V_0 + 200 \text{ ICQ} = 0)

\[ \Rightarrow \frac{R_2}{R_1 + R_2} = \frac{V_0 + 200 \text{ ICQ}}{V_{cc}} \]  \hspace{1em} (2)

From (1) and (2):

\[ R_1 = 12.4 \text{ K} \]
\[ R_2 = 2.4 \text{ K} \]

\[ V_{RB} = 2K \text{ ICQ} = 75 \text{ mV} \]
\[ V_{BB} = 1.45 \text{ V} \]

**Stability of Transistor Circuits with Active Components:**

Active component: diode, transistor, thermistor...

**-V_{BE} Compensation with Diode:**

- Diode is forward biased using \( V_D \)

- Diode and transistor are made up of the same material and thus \( V_{BE} = V_0 \)

- Due to \( V_{BE} = V_0 \), IC is independent from variations of \( V_{BE} \) as:

- **61**
\[ I_c = \beta I_B + (1+\beta) I_{co} \]

\[ I_c = \frac{\beta \left[ V_{bb} - (V_{be} - V_o) \right] + (R_B + R_e) (1+\beta) I_{co}}{R_B + (1+\beta) R_e} \]

\[ V_{be} - V_o = 0 \quad \text{Thus;} \]

\[ I_c = \frac{\beta V_{bb} + (R_B + R_e) (1+\beta) I_{co}}{R_B + (1+\beta) R_e} \]

Assume that \((1+\beta) R_e \gg R_B\) and \(\beta \gg 1\);

\[ \Rightarrow I_c = \frac{V_{bb}}{R_e} + \left(1 + \frac{R_B}{R_e}\right) I_{co} \]

\[ \text{constant} \]

Thus, \(I_c\) is not affected by \(V_{be} \).

--- Ico Compensation with Diode: 

Ico current increases with temperature especially for Ge type transistors, resulting with increased collector current. In order to compensate this increase a diode which is made up of the same material with the transistor can be used as:

- Diode and transistor are affected from temperature similarly (both are Ge type) thus;
If $T \uparrow$, diode $I_s \uparrow$, transistor $I_s'$ in CB junction $\Rightarrow$ ; $I_c \downarrow$

$T \uparrow \Rightarrow I_s \uparrow$, $I_B \downarrow \Rightarrow I_c \downarrow$

$I_B + I_s = I$ ; $I_B = I - I_s$

$I_c = \beta I_B + (1 + \beta) I_{co}$

$$I_c = \beta \frac{V_{cc}}{R} - I_s \uparrow + (1 + \beta) I_{co}$$

Assume that $V_0 = V_{be}$ ;

$\Rightarrow I_s = I_{co}$ and if $\beta \gg 1$

$I_c = \beta \left[ \frac{V_{cc}}{R} - I_s \uparrow \right] - \beta I_{co}$

$$= \beta \frac{V_{cc}}{R} ; \text{remains constant}$$

---

**$I_c$ Compensation without using $R_E$**

The resistance $R_E$ decreases the ac gain of the transistor amplifier but provides stability. In order to increase stability without using $R_E$ and providing high gain such a structure can be used:  

- **BC shorted transistor**
  acts like a diode.
  
  Thus $V_0 = V_{be2}$ : which makes $I_c2$ is stable for temperature variations.
\[ I_{c1} = I - I_{B1} - I_{B2} \quad \text{or;} \]
\[ I_{c1} = \frac{V_{cc} - V_{be}}{R_1} - (I_{B1} + I_{B2}) \]

Assume that \( V_{cc} \gg V_{be} \) and \( (I_{B1} + I_{B2}) << I_{c1} \)

\[ I_{c1} \approx \frac{V_{cc}}{R_1} \approx \text{constant} \quad \text{means that input of Q2 is constant.} \]

If \( Q1 = Q2 \Rightarrow I_{c1} = I_{c2} = \text{constant} \).

It is experimentally shown that if \( Q1 \neq Q2 \), stability of the structure for temperature is gain very good within \( \% 5 \).

**AC Analysis of the BJT Circuits:**

In the previous sections we have analysed BJT amplifier circuits for only dc type sources and determined dc operating point \( Q \left( I_{cQ}, V_{CEQ} \right) \). In this section we will extend our analysis for ac type sources in order to determine voltage and current gain \( (V_o/V_i, I_o/I_i) \) of the given structures.

In order to perform ac analysis, we have to firstly:

- Kill the voltage sources by grounding them.
- Short the capacitors due to \( \frac{1}{wc} \).
Definition: \( h_{ie} = \text{transistor's ac input impedance} \)
\[
h_{ie} = \frac{V_{be}}{i_b}
\]

Representations:
\[
\begin{align*}
I_c & \quad \{ \text{DC} \} \quad \{ i_c \} \quad \text{AC} \quad \{ i_C \} \quad \text{DC+AC} \\
V_{CE} & \quad \{ \text{DC} \} \quad V_{ce} \quad \{ \text{AC} \} \quad V_{CE} \quad \{ \text{DC+AC} \}
\end{align*}
\]

For the given circuit, ac analysis gives:
\[
V_i = V_{be} + R_E i_b \quad (R_E = 0 \text{ if } C_3 \text{ is present})
\]
\[
= h_{ie} i_b + R_E (1+\beta) i_b
\]
\[
= (h_{ie} + R_E (1+\beta)) i_b
\]
\[
\frac{V_o}{V_i} = \text{Gain} = \frac{-i_c R_c}{[h_{ie} + (1+\beta) R_E] i_b} = \frac{-\beta R_c}{h_{ie} + (1+\beta) R_E} = V_{\text{gain}}=A_v
\]

If \( R_E = 0 \) (i.e. \( R_E \) is shorted by \( C_3 \)) \( A_v \) is maximum.

and equal to:
\[
A_v = \frac{-\beta R_c}{h_{ie}}
\]
$V_{CE} = V_{CEQ} + V_c$

$i_C = I_{CQ} + i_c$

$V_{Ce} = -i_C R_C$

\[ V_{CEQ} = V_{cc} - (R_c + R_e) I_c \]  \hspace{1cm} \text{DC equation (1)}

$V_{ce} = V_{CE} - V_{CEQ}$

$i_c = i_C - I_{CQ}$

\[ V_C = V_{CEQ} + R_c I_{CQ} - R_c i_c \]  \hspace{1cm} \text{AC equation (2)}

From (1) & (2) total eqn:

\[ V_{CE} = V_{cc} - R_e I_{CQ} - R_c i_c \]  \hspace{1cm} \text{AC+DC eqn.}

$V_{CE} = 0 \Rightarrow i_C = \frac{V_{cc} - R_e I_{CQ}}{R_C}$

$i_C = 0 \Rightarrow V_{CE} = V_{cc} - R_e I_{CQ}$

AC and DC load lines differ due to $R_e$. Because $R_e$ is present in the dc circuit only, but not in ac circuit.

Now, let us apply above expressions to a practical amplifier circuit:

\[ \text{Ex:} \]

Let us start with the dc analysis:
Now, let us apply above equations to a practical amplifier circuit:

**DC Analysis:**
where:

\[ R_B = R_1 \parallel R_2 \]

\[ V_{BB} = V_{cc} \cdot \frac{R_2}{R_1 + R_2} \]

\[ I_C = I_e = I_c \]

\[ V_{CE} = V_{cc} - (R_c + R_e) I_c \] \[ \text{dc eqn.} \]

**AC Analysis:**
1. \( \frac{1}{j\omega C} = 0 \): capacitors are shorted
2. DC voltage sources are killed (due to superposition):

\[ V_{ce} = -R' i_c = ac \]

\[ = V_{CE} - V_{CEQ} \]

\[ i_c = I_c - I_{cq} = ac \]

\[ V_{ce} = -R_c' i_c = R'(i_c - I_{cq}) \]

\[ \Rightarrow \]

\[ V_{ce} = V_{CEQ} + R' I_{cq} - R' i_c \]
if $i_C = 0 \Rightarrow U_{CE} = V_{CEq} + R' I_C$ \\
$U_{CE} = 0 \Rightarrow i_C = \frac{V_{CEq} + R' I_C}{R'} = V_{CEq} \cdot \frac{R'}{R' + I_C}$

We have found that:

$V_{CEq} = V_{CC} - (R_c + R_e - R') I_{CQ}$ from dc analysis. Thus $U_{CE}$ can be given in the form:

$U_{CE} = V_{CC} - (R_c + R_e - R') I_{CQ} - R' i_C \Rightarrow \text{ac. eqn.}$

if $U_{CE} = 0 \Rightarrow i_C = \left(\frac{V_{CC} - (R_c + R_e - R') I_{CQ}}{R'}\right)$. $R' i_C = 0 \Rightarrow U_{CE} = V_{CC} - \left[\frac{R_c + R_e - R'}{R'}\right] I_{CQ}$ can be found.

\[\text{Ex:} \]

\begin{align*}
V_{CC} &= 30V \\
R_c &= 1k \\
C_c &= \text{...} \\
R_e &= 470\Omega \\
C_e &= \text{...} \\
R_L &= 1k
\end{align*}

\[\begin{align*}
I_{BE} &= 50\mu A \\
I_{CQ} &= 15\text{ mA} \\
V_{CEq} &= \text{14V} \\
\alpha &= 1
\end{align*}\]

\(a\)
\(b\)

draw AC and DC load lines.

If $i_C = 50\mu A \sin \omega t$ find $i_C$ and $U_{CE}$.

DC analysis:

Assume that (you may!)

$R_B \ll (1+\beta) R_e$ \\
and thus $V_{BB}$ is very small.

\(\Rightarrow\) it is not so much important to know $R_B$ ($\ll (1+\beta) R_e$)
under such conditions:

$$I_E = \frac{V_{BB}}{R_E} \quad (V_{BE} \text{ and } V_{BB} \text{ are ignored!})$$

$$V_{CEA} = 30 - 1.47 \cdot I_{CE} \quad (\text{of } V_{CC} = (R_e + R_0)I_{CE})$$

dc load line eqn.

**AC Analysis:**

\[ V_{CE} = -R' \cdot i_c = -0.5 \cdot i_c = 0 \]  
\[ V_{CE} = V_{CE} - V_{CEA} = -0.5 \cdot i_c \]  
\[ V_{CE} = 11 + (-0.5 \cdot (i_c - I_{CE})) \]  
\[ V_{CE} = 11 + 0.5 \cdot 13 - 0.5 \cdot i_c \]

\[ V_{CE} = 17.5 - 0.5 \cdot i_c \]  
\[ \Rightarrow i_c = 0 \Rightarrow V_{CE} = 17.5 \text{ V} \]  
\[ V_{CE} = 0 \Rightarrow i_c = 35 \text{ mA} \]  

required for drawing!

\[ i_b \approx i_i \quad (\text{due to small } h_{ie} \text{ with respect to } \text{big } R_b) \]

\[ \Rightarrow i_i = 50 \text{ mA} \sin \omega t = i_b. \]

\[ i_b_{\text{max}} = 50 \text{ mA} \]
\[ i_b_{\text{min}} = -50 \text{ mA} \]

\[ \Rightarrow I_{BQ} + i_b_{\text{max}} = 50 + 50 = 100 \text{ mA} \]
\[ I_{BQ} - i_b_{\text{min}} = 50 - 50 = 0 \text{ mA} \]
If we show these results graphically:

\[ i_C = I_{ce} + i_c = 13 \, mA + 13 \, mA \sin \omega t \]

\[ A_I = B = \frac{i_C}{i_b} = \frac{i_c}{i_b_{\text{max}}} = \frac{13 \, mA}{260 \, \mu A} = 50 \, \mu \]

\[ V_{CE} = V_{CEQ} + V_{ce} = 11 \, V + 6.5 \, \sin \omega t \]

\[ i_C (oc) \]

\[ (-13 \, mA, +13 \, mA) \]

\[ V_{CE} \]

\[ (-6.5 \, V, 6.5 \, V) \]

\[ (4.5 \, V, 13.5 \, V) \]

\[ I_{CO} = 100 \, \mu A \]

\[ I_b = 50 \, \mu A \]

\[ \text{dc load line} \]

\[ Q \text{ point must be very near to the middle region as much as possible to avoid distortion of the output!} \]
Ex: For the given circuit:

a.) Find Q point for maximum undistorted current swing.

b.) Draw ac and dc load lines.

\[ V_{cc} = V_{ceq} + I_{ce} (R_{e} + r_{e}) \]

\[ 15 = V_{ceq} + I_{ce} \cdot 1500 \]

\[ (i_{c} - I_{ca}) = -\frac{1}{R_{c}} (V_{ce} - V_{ceq}) \]

Thus \( i_{c}^{\max} \) is possible when \( V_{ceq} = 0 \)

\[ \Rightarrow i_{c}^{\max} = I_{ca} + \frac{V_{ceq}}{R_{c}} \]

If we choose \( i_{c}^{\max} = 2I_{ca} \):

\[ I_{c}^{\max} = 2I_{ca} = I_{ca} + \frac{V_{ceq}}{R_{c}} \]

\[ \Rightarrow I_{ca} = \frac{V_{ceq}}{R_{c}} \]

\[ 15 = V_{ceq} + 1500I_{ca} \]

\[ I_{ca} = 6\text{mA} \text{, } V_{ceq} = 6\text{V} \Rightarrow Q(6\text{V}, 6\text{mA}) \]

\[ V_{ce} = V_{cc} - R_{e} I_{ca} - R_{c} i_{c} \]

\[ i_{c} = 0 \Rightarrow V_{ce} = 15 - 500 \cdot 6 = 12\text{V} \]

\[ V_{ce} = 0 \Rightarrow 0 = 15 - 500 \cdot 6 = 1\text{K} \cdot i_{c} \]

\[ i_{c} = \frac{12}{1\text{K}} = 12\text{mA} \]

b.) \[ i_{c} \]

\[ 12 \quad 10 \quad 8 \quad 6 \quad 4 \quad 2 \quad 0 \]

\[ 15 \quad V_{ce} \]

\[ 6 \quad 12 \quad 15 \]

\[ DC \text{ eqn.:} \]

\[ V_{cc} = V_{ceq} + I_{ce} (R_{e} + r_{e}) \]

\[ 15 = V_{ceq} + I_{ce} \cdot 1500 \]