Cascaded Systems

In cascaded (or multistage) systems output of one amplifier is connected to the input of the next amplifier as shown below.

We would like to represent the overall system as a voltage-gain amplifier as shown below.
So, the input resistance $R_i = \frac{v_i}{i_i}$, the output resistance $R_o = \frac{v_L(\text{open-circuit})}{i_L(\text{short-circuit})}$, and the no-load voltage gain $A_v = \frac{v_o(\text{no-load})}{v_i}$ of the whole cascaded system is given by

\[
R_i = R_{i1}
\]
\[
R_o = R_{o_n}
\]
\[
A_v = A_{v1} \times \frac{R_{i2}}{R_{o1} + R_{i2}} \times A_{v2} \times \cdots \times \frac{R_{ik}}{R_{o_{k-1}} + R_{ik}} \times A_{vk} \times \cdots \times \frac{R_{in}}{R_{o_{n-1}} + R_{in}} \times A_{vn}
\]

where $R_{ik}$, $R_{ok}$, and $A_{vk}$ are the input resistance, output resistance and no-load gain of the $k$-th stage, respectively, $1 \leq k \leq n$ and $n$ is the maximum number of stages.

**NOTE:** Thus, the input resistance of the current stage acts as a load for the previous stage, or the output resistance of the previous stage acts as a source resistance for the current stage.

Consequently, we can represent the overall no-load voltage-gain $A_v$ in terms of the load-included voltage gains of each stage except the last stage

\[
A_v = \left. \frac{v_o}{v_i} \right|_{R_L=\infty} = A_{V1} \times A_{V2} \times \cdots A_{Vk} \times \cdots \times A_{vn}
\]

where $A_{Vk}$ is the load-included voltage gain of $k$-th stage given by

\[
A_{Vk} = A_{vk} \left( \frac{R_{i{k+1}}}{R_{ok} + R_{i{k+1}}} \right).
\]
Similarly, we can represent the overall no-load voltage-gain \( A_v \) in terms of the source-included voltage gains of each stage except the first stage

\[
A_v = \left. \frac{v_o}{v_i} \right|_{R_L = \infty} = A_{v1} \times A_{v2} \times \cdots A_{v_{k-1}} \times A_{v_{k} \ldots} \times A_{v_{n}}
\]

where \( A_{v_{k}} \) is the source-included voltage gain of \( k \)-th stage given by

\[
A_{v_{k}} = \left( \frac{R_{i_{k}}}{R_{o_{k-1}} + R_{i_{k}}} \right) A_{v_{k}}.
\]

Example 1: For the figure above, find the input resistance \( R_i \), output resistance \( R_o \) and the overall voltage gain \( A_{V_s} = v_o/v_s \) of the whole system.

Solution: The input resistance \( R_i \), output resistance \( R_o \) and the total voltage gain \( A_{V_s} \) of the overall system are given as follows

\[
R_i = R_{i1} = 10 \, k\Omega, \\
R_o = R_{o2} = 5.1 \, k\Omega, \\
A_v = A_{v1} \left( \frac{R_{i2}}{R_{o1} + R_{i2}} \right) A_{v2} = (1) \left( \frac{26}{12 + 26} \right) (240) \simeq 164.21, \\
A_{V_s} = \left( \frac{R_i}{R_s + R_i} \right) A_v \left( \frac{R_L}{R_o + R_L} \right) = \left( \frac{10k}{1k + 10k} \right) (164.21) \left( \frac{8.2k}{5.1k + 8.2k} \right) \simeq 92.
\]

Homework 8: Calculate the overall voltage gain \( A_{V_s} \) by removing the first stage. Thus, explain the purpose of the first stage.
AC-Coupled Multistage Amplifiers

In AC-coupled multistage amplifiers, the DC bias circuits are isolated from each other by the coupling capacitors at the input and output of each stage.

Thus,

- The DC calculations are independent of the cascading.
- The AC calculations for gain and impedance are interdependent.

Example 2: For the figure above, find the input resistance $R_i$, output resistance $R_o$ and the no-load voltage gain $A_v = v_o/v_i$ of the whole system.

Solution: The input resistance $R_i$, output resistance $R_o$ and the no-load voltage gain $A_v$ of the overall system are given as follows

$$R_i = R_G$$
$$R_o = R_D||r_{ds}$$
$$A_v = \left[ -g_m \left( R_D||r_{ds} \right) \right] \left[ -g_m \left( R_D||r_{ds} \right) \right]$$
$$= g_m g_m \left( R_D||r_{ds} \right) \left( R_D||r_{ds} \right).$$
Example 3: For the figure above, find the input resistance $R_i$, output resistance $R_o$ and the no-load voltage gain $A_v = v_o/v_i$ of the whole system.

Solution: The input resistance $R_i$, output resistance $R_o$ and the no-load voltage gain $A_v$ of the overall system are given as follows

$$R_i = R_1 || R_2 || h_{ie1}$$

$$R_o = R_{C2} || 1/h_{oe2}$$

$$A_v = \left( \frac{h_{fe2}(R_{C2} || 1/h_{oe2})}{h_{ie2}} \right) \left( \frac{h_{fe1}(R_{C1} || 1/h_{oe1} || R_{i2})}{h_{ie1}} \right)$$

$$= \frac{h_{fe2} h_{fe1}(R_{C2} || 1/h_{oe2})(R_{C1} || 1/h_{oe1} || R_3 || R_4 || h_{ie2})}{h_{ie2} h_{ie1}}.$$
DC-Coupled Multistage Amplifiers

In DC-coupled multistage amplifiers, the DC bias circuits are not isolated from each other. Thus,

- The DC calculations are not independent of the cascading.
- The AC calculations for gain and impedance are interdependent.

DC-coupled multistage amplifiers are used either to amplify very low frequency signals or to amplify DC signals.

Example 5: For the figure above,

a) Draw AC and DC load lines for both transistors.

b) Calculate the overall voltage gain $A_{Vs} = \frac{v_o}{v_s}$.

 c) Find $v_s(\text{max})$ which produces maximum undistorted output voltage.
Solution: a) Let us first start with DC analysis and apply the Thévenin theorem at the base of the first transistor.

\[ V_{BB1} = \frac{30k}{30k + 60k} 30 = 10V \]
\[ R_{BB1} = \frac{30k}{60k} = 20k \Omega \]

Note that, \( I_{E1} = I_{RE1} + I_{B2} \approx I_{RE1} \) assuming \( I_{E2} \sim I_{E1} \). So, we can find \( I_{RE1} \) as follows:

\[ I_{RE1} \approx \frac{V_{BB1} - V_{BE1(ON)}}{R_{E1} + R_{BB1}/(\beta + 1)} = \frac{10 - 0.6}{1k + 20k/21} \approx 4.82 \text{mA} \]

Consequently, \( I_{CQ1} \approx I_{RE1} = 4.82 \text{mA} \) and \( R_{DC1} \approx R_{E1} = 1k \Omega \). Also, as \( V_{B2} = V_{E2} = 4.82 \text{V} \), we can find \( I_{E2} \) as

\[ I_{E2} = \frac{V_{E1} - V_{BE2(ON)}}{R_{E2}} = \frac{4.82 - 0.6}{1k} \approx 4.22 \text{mA} \]

Thus, \( I_{E2} \sim I_{E1} \) and our assumption holds. Here assuming \( \alpha = 20/21 \approx 1 \), we obtain \( R_{DC2} \approx R_{C1} + R_{E2} = 3k\Omega \).

As \( R_{ac1} \approx R_{DC1} = 1k \Omega \) and \( R_{ac2} = R_{DC2} = 3k\Omega \), AC and DC load-lines coincide for both transistors, i.e.,

\[ v_{CE1} = V_{CC} - i_{C1}R_{ac1} \quad \ldots \text{AC-DC load lines are the same} \]
\[ v_{CE2} = V_{CC} - i_{C2}R_{ac2} \quad \ldots \text{AC-DC load lines are the same} \]
Consequently, AC (and DC) load-line for the first transistor is shown below.

\[ v_{CE1(\text{max})} = \min \left( V_{CEQ1}, I_{CQ1} R_{ac1} \right) = \min (25.18, 4.82) = 4.82 \text{ V}. \]

Similarly, AC (and DC) load-line for the second transistor is shown below.

\[ v_{CE2(\text{max})} = \min \left( V_{CEQ2}, I_{CQ2} R_{ac2} \right) = \min (17.34, 12.66) = 12.66 \text{ V}. \]
b) Let us first find $h_{ie1}, h_{ie2}$ and $R_i$

$$h_{ie1} = h_{fe1} \frac{\gamma}{I_{CQ1}} = 20 \frac{26m}{4.82m} = (20)(5.39) \approx 108 \Omega$$

$$h_{ie2} = (h_{fe2} + 1) \frac{\gamma}{I_{CQ2}} = 21 \frac{26m}{4.22m} = (21)(6.16) \approx 129 \Omega$$

$$R_i \approx R_1||R_2||[h_{ie1} + (h_{fe1} + 1) R_{E1}] = 30k||60k||[108 + (21)(1k)] \approx 10.3k \Omega$$

Later, let us calculate the no-load gain $A_{v2} = v_o/v_{i2} = v_o/v_{o1}$ of the second stage

$$A_{v2} = \frac{v_o}{v_{o1}} = -h_{fe2} R_C = \frac{-20(2k)}{129 + (21)(1k)} = 1.89$$

Now, let us calculate the overall gain $A_{Vs1} = v_{o1}/v_s$ of the first stage

$$A_{Vs1} = \frac{v_{o1}}{v_s} = \left(\frac{R_i}{R_s + R_i}\right) \left(\frac{(h_{fe1} + 1) R_{E1}}{h_{ie1} + (h_{fe1} + 1) R_{E1}}\right)
= \left(\frac{10.3k}{1k + 10.3k}\right) \left(\frac{21(1k)}{108 + (21)(1k)}\right) \approx 0.91.$$

So, the overall voltage gain $A_{Vs}$ is given by

$$A_{Vs} = A_{Vs1} \times A_{v2} = (0.91)(1.89) = 1.72.$$

c) From $v_{CE1(max)}$ and $v_{CE2(max)}$ calculated in part (a), and from $A_{v2}$ and $A_{Vs1}$ calculated in part (b), we see that the limiting factor comes from the first stage. Because

$$\left(v_{CE1(max)} < \frac{v_{CE2(max)}}{A_{v2}}\right) \Rightarrow \left(4.82 < \frac{12.66}{1.89}\right) \Rightarrow (4.82V < 6.7V)$$

Consequently,

$$v_{s(max)} = \frac{v_{CE1(max)}}{A_{Vs1}} = \frac{4.82}{0.91} = 5.30V.$$
**Example 6:** For the figure above,

a) Draw AC and DC load lines for both transistors.

b) Calculate the overall voltage gain \( A_{Vs} = \frac{v_o}{v_s} \).

c) Find \( v_s(\text{max}) \) which produces maximum undistorted output voltage.

**Homework 10:** Solve the question given in Example 6.

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**Example 7:** For the figure above,

a) Calculate the overall voltage gain \( A_{Vs} = \frac{v_o}{v_s} \).

b) Find the output resistance \( R_o \).

**Homework 11:** Solve the question given in Example 7.
Cascode Amplifier

The cascode configuration is a CE-CB combination, where the collector of the first transistor is connected to the emitter of the second transistor as shown below.

The arrangements provide a relatively high-input impedance with low voltage gain for the first CE stage to ensure the input Miller capacitance is at a minimum, whereas the following CB stage provides the high gain.

Therefore, therefore this combination works well in high frequency applications.

Example 8: For the cascode amplifier above, find the input resistance \( R_i \), output resistance \( R_o \) and the voltage gain \( A_v = v_o/v_i \).
Solution: Let us perform DC analysis first and calculate \( I_{EQ1} \)

\[
I_{EQ1} = \frac{V_{B1} - V_{BE(ON)}}{R_E} \\
\cong \frac{R_{B3}}{R_{B1} + R_{B2} + R_{B3}} \frac{V_{CC} - V_{BE(ON)}}{R_E} \\
= \frac{4.7k}{6.8k + 5.6k + 4.7k} \frac{18 - 0.7}{1k} = \frac{4.95 - 0.7}{1k} = 4.25 \text{ mA}
\]

As \( \alpha = 100/101 \cong 1 \), \( I_{EQ1} \cong I_{CQ1} = I_{EQ2} \cong I_{CQ2} \). So, \( h_{ie} = h_{ie1} = h_{ie2} \) given by

\[
h_{ie} = (h_{fe} + 1) \frac{\gamma}{I_{EQ}} = (101) \left( \frac{26m}{4.25m} \right) \cong 618 \Omega
\]

So, the SSAC equivalent circuit is given below.
Thus, we can calculate $R_i$, $R_o$ and $A_v$ as follows

$$R_i = R_{B3} || R_{B2} || h_{ie1} = 4.7k || 5.6k || 618 \cong 498 \Omega$$

$$R_o = R_C = 1.2 \text{k}\Omega$$

$$A_v = \left(\frac{v_o}{i_{e2}}\right) \left(\frac{i_{e2}}{i_{b1}}\right) \left(\frac{i_{b1}}{v_i}\right)$$

$$= (-h_{fb2} R_C) (-h_{fe1}) \left(\frac{1}{h_{ie1}}\right)$$

$$= - \frac{(100)(1.2k)}{0.618k} = -194.$$  

**Homework 12:** Show that the voltage gain $A_{V1} = v_{o1}/v_i = -1$ for the first stage of the amplifier. Consequently, comment on the Miller effect.

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**Darlington Pair**

A very popular connection of $npn$ two bipolar junction transistors for operation as one *superbeta* $npn$ transistor is the Darlington connection shown below.

The main feature of the Darlington connection is that the composite transistor as shown below acts as a single unit with a current gain that is the product of the current gains of the individual transistors.
Consequently, current gain $\beta_D$ and base-emitter turn-on voltage $V_{BE_D(ON)}$ are given as follows:

\[
\beta_D = \beta_1 \beta_2 + \beta_1 + \beta_2 \approx \beta_1 \beta_2
\]

\[
V_{BE_D(ON)} = 2V_{BE(ON)}
\]

Such that $I_C = \beta_D I_B$ and $I_E = (\beta_D + 1) I_B$ when both transistors are in the forward active mode.

**Homework 13:** Show that above expressions for $\beta_D$ and $V_{BE_D(ON)}$ are correct.

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**Feedback Pair**

The feedback pair connection shown below is a two-transistor circuit that operates like the Darlington circuit.

Notice that the feedback pair uses a $pnp$ transistor driving an $nnp$ transistor, the two devices acting effectively much like one $pnp$ transistor as shown below. As with a Darlington connection, the feedback pair also provides a very high current gain.
Consequently, current gain $\beta_F$ and emitter-base turn-on voltage $V_{BE_F(ON)}$ are given as follows:

$$\beta_F = \beta_1 \beta_2 + \beta_1 \approx \beta_1 \beta_2$$

$$V_{BE_F(ON)} = V_{BE(ON)}$$

Such that $I_C = \beta_F I_B$ and $I_E = (\beta_F + 1) I_B$ when both transistors are in the forward active mode.

**Homework 14:** Show that above expressions for $\beta_F$ and $V_{BE_F(ON)}$ are correct.