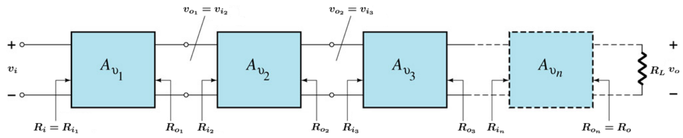
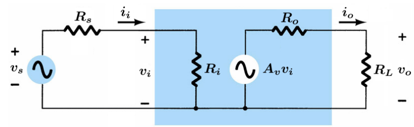
Contents

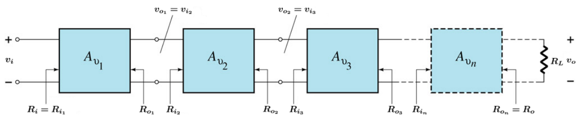
Cascaded Systems

In cascaded (or multistage) systems output of one amplifier is connected to the input to the next amplifier as shown below.



We would like to represent the overall system as a voltage-gain amplifier as shown below.



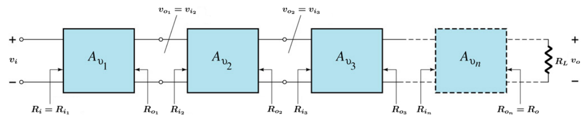


So, the input resistance $R_i = \frac{v_i}{i_i}$, the output resistance $R_o = \frac{v_{L(\text{open-circuit})}}{i_{L(\text{short-circuit})}}$ and the no-load voltage gain $A_v = \frac{v_{o(\text{no-load})}}{v_i}$ of the whole cascaded system is given by

$$R_i = R_{i_1}$$
$$R_o = R_{o_n}$$
$$A_v = A_{v_1} \times \frac{R_{i_2}}{R_{o_1} + R_{i_2}} \times A_{v_2} \times \cdots \times \frac{R_{i_k}}{R_{o_{k-1}} + R_{i_k}} \times A_{v_k} \times \cdots \times \frac{R_{i_n}}{R_{o_{n-1}} + R_{i_n}} \times A_{v_n}$$

where R_{i_k}, R_{o_k} and A_{v_k} are the input resistance, output resistance and no-load gain of the k-th stage, respectively, $1 \leq k \leq n$ and n is the maximum number of stages.

NOTE: Thus, the input resistance of the current stage acts as a load for the previous stage, or the output resistance of the previous stage acts as a source resistance for the current stage.

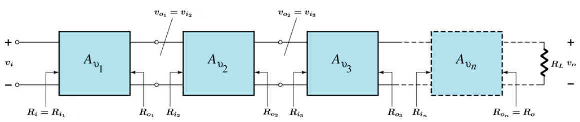


Consequently, we can represent the overall no-load voltage-gain A_v in terms of the load-included voltage gains of each stage except the last stage

$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = A_{V_1} \times A_{V_2} \times \cdots A_{V_k} \cdots \times A_{v_n}$$

where A_{V_k} is the load-included voltage gain of k-th stage given by

$$A_{V_k} = A_{v_k}\left(\frac{R_{i_{k+1}}}{R_{o_k} + R_{i_{k+1}}}\right).$$

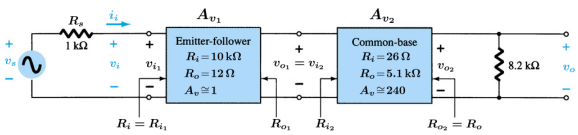


Similarly, we can represent the overall no-load voltage-gain A_v in terms of the source-included voltage gains of each stage except the first stage

$$A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = A_{v_1} \times A_{vs_2} \times \cdots A_{vs_k} \cdots \times A_{vs_n}$$

where A_{vs_k} is the source-included voltage gain of k-th stage given by

$$A_{vs_k} = \left(\frac{R_{i_k}}{R_{o_{k-1}} + R_{i_k}}\right) A_{v_k}.$$



Example 1: For the figure above, find the input resistance R_i, output resistance R_o and the overall voltage gain $A_{Vs} = v_o/v_s$ of the whole system.

Solution: The input resistance R_i, output resistance R_o and the total voltage gain A_{Vs} of the overall system are given as follows

$$R_i = R_{i_1} = 10\,\text{k}\Omega,$$
$$R_o = R_{o_2} = 5.1\,\text{k}\Omega,$$
$$A_v = A_{v_1}\left(\frac{R_{i_2}}{R_{o_1} + R_{i_2}}\right) A_{v_2} = (1)\left(\frac{26}{12+26}\right)(240) \cong 164.21,$$
$$A_{Vs} = \left(\frac{R_i}{R_s + R_i}\right) A_v \left(\frac{R_L}{R_o + R_L}\right) = \left(\frac{10k}{1k + 10k}\right)(164.21)\left(\frac{8.2k}{5.1k + 8.2k}\right) \cong 92.$$

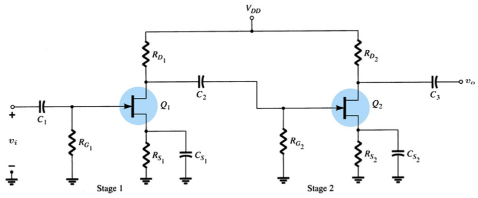
Homework 8: Calculate the overall voltage gain A_{Vs} by removing the first stage. Thus, explain the purpose of the first stage.

AC-Coupled Multistage Amplifiers

In AC-coupled multistage amplifiers, the DC bias circuits are **isolated** from each other by the **coupling capacitors** at the input and output of **each stage**.

Thus,

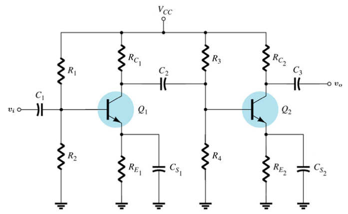
- The **DC** calculations are **independent** of the cascading.
- The AC calculations for gain and impedance are interdependent.



Example 2: For the figure above, find the input resistance R_i, output resistance R_o and the no-load voltage gain $A_v = v_o/v_i$ of the whole system.

Solution: The input resistance R_i, output resistance R_o and the no-load voltage gain A_v of the overall system are given as follows

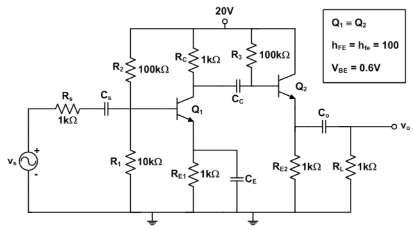
$$\begin{aligned} R_i &= R_{G_1} \\ R_o &= R_{D_2} || r_{ds_2} \\ A_v &= \left[-g_{m_2}\left(R_{D_2}||r_{ds_2}\right)\right]\left[-g_{m_1}\left(R_{D_1}||r_{ds_1}||R_{i_2}\right)\right] \\ &= g_{m_2} g_{m_1}\left(R_{D_2}||r_{ds_2}\right)\left(R_{D_1}||r_{ds_1}||R_{G_2}\right). \end{aligned}$$



Example 3: For the figure above, find the input resistance R_i, output resistance R_o and the no-load voltage gain $A_v = v_o/v_i$ of the whole system.

Solution: The input resistance R_i, output resistance R_o and the no-load voltage gain A_v of the overall system are given as follows

$$\begin{aligned} R_i &= R_1||R_2||h_{ie_1} \\ R_o &= R_{C_2}||1/h_{oe_2} \\ A_v &= \left(-\frac{h_{fe_2}\left(R_{C_2}||1/h_{oe_2}\right)}{h_{ie_2}}\right)\left(-\frac{h_{fe_1}\left(R_{C_1}||1/h_{oe_1}||R_{i_2}\right)}{h_{ie_1}}\right) \\ &= \frac{h_{fe_2}h_{fe_1}\left(R_{C_2}||1/h_{oe_2}\right)\left(R_{C_1}||1/h_{oe_1}||R_3||R_4||h_{ie_2}\right)}{h_{ie_2}h_{ie_1}}. \end{aligned}$$



Example 4: For the figure above,

a) Draw AC and DC load lines for both transistors.
b) Calculate the overall voltage gain $A_{Vs} = v_o/v_s$.
c) Find $v_{s(\text{max})}$ which produces maximum undistorted output voltage.

Homework 9: Solve the question given in Example 4.

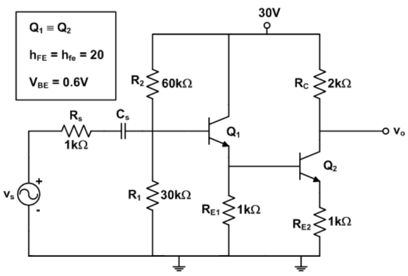
DC-Coupled Multistage Amplifiers

In DC-coupled multistage amplifiers, the DC bias circuits are **not isolated** from each other.

Thus,

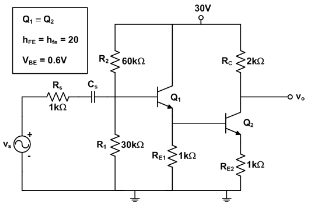
- The **DC** calculations are **not independent** of the cascading.
- The AC calculations for gain and impedance are interdependent.

DC-coupled multistage amplifiers are used either to amplify very low frequency signals or to amplify DC signals.



Example 5: For the figure above,

a) Draw AC and DC load lines for both transistors.
b) Calculate the overall voltage gain $A_{Vs} = v_o/v_s$.
c) Find $v_{s(\text{max})}$ which produces maximum undistorted output voltage.

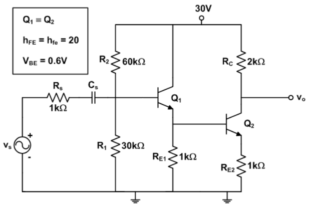


Solution: a) Let us first start with DC analysis and apply the Thévenin theorem at the base od the first transistor

$$V_{BB_1} = \frac{30k}{30k+60k} 30 = 10\,\text{V}$$
$$R_{BB_1} = 30k \| 60k = 20\,\text{k}\Omega$$

Note that, $I_{E_1} = I_{RE_1} + I_{B_2} \cong I_{RE_1}$ assuming $I_{E_2} \sim I_{E_1}$. So, we can find I_{RE_1} as follows

$$I_{RE_1} \cong \frac{V_{BB_1} - V_{BE_1(ON)}}{R_{E_1} + R_{BB_1}/(\beta+1)} = \frac{10-0.6}{1k+20k/21} \cong 4.82\,\text{mA}$$



Consequently, $I_{CQ_1} \cong I_{RE_1} = 4.82\,\text{mA}$ and $R_{DC_1} \cong R_{E_1} = 1\,\text{k}\Omega$. Also, as $V_{B_2} = V_{E_2} = 4.82\,\text{V}$, we can find I_{E_2} as

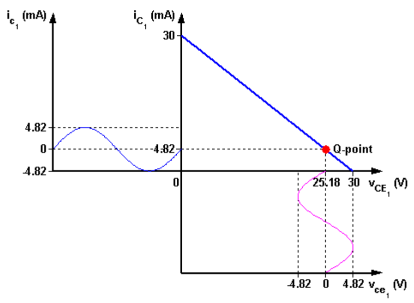
$$I_{E_2} = \frac{V_{E_1} - V_{BE_2(ON)}}{R_{E_2}} = \frac{4.82-0.6}{1k} \cong 4.22\,\text{mA}$$

Thus, $I_{E_2} \sim I_{E_1}$ and our assumption holds. Here assuming $\alpha = 20/21 \approx 1$, we obtain $R_{DC_2} \cong R_C + R_{E_2} = 3\,\text{k}\Omega$.

As $R_{ac_1} \cong R_{DC_1} = 1\,\text{k}\Omega$ and $R_{ac_2} = R_{DC_2} = 3\,\text{k}\Omega$, AC and DC load-lines coincide for both transistors, i.e.,

$$v_{CE_1} = V_{CC} - i_{C_1} R_{ac_1} \qquad \text{...AC-DC load lines are the same}$$
$$v_{CE_2} = V_{CC} - i_{C_2} R_{ac_2} \qquad \text{...AC-DC load lines are the same}$$

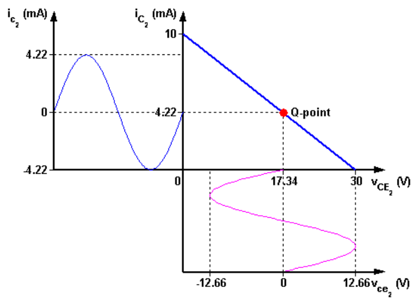
Consequently, AC (and DC) load-line for the first transistor is shown below



We can see that maximum undistorted swing for the first transistor is given by

$$v_{CE_{1(\mathbf{max})}} = \min\left(V_{CEQ_1}, I_{CQ_1} R_{ac_1}\right) = \min(25.18, 4.82) = 4.82\,\text{V}.$$

Similarly, AC (and DC) load-line for the second transistor is shown below



We can see that maximum undistorted swing for the second transistor is given by

$$v_{CE_{2(\mathbf{max})}} = \min\left(V_{CEQ_2}, I_{CQ_2} R_{ac_2}\right) = \min(17.34, 12.66) = 12.66\,\text{V}.$$

b) Let us first find h_{ie_1}, h_{ie_2} and R_{i_1}

$$_{ie_1} = h_{fe_1} \frac{\gamma}{I_{CQ_1}} = 20 \frac{26m}{4.82m} = (20)(5.39) \cong 108\,\Omega$$
$$h_{ie_2} = \left(h_{fe_2}+1\right) \frac{\gamma}{I_{CQ_2}} = 21 \frac{26m}{4.22m} = (21)(6.16) \cong 129\,\Omega$$
$$R_{i_1} \cong R_1 \| R_2 \| \left[h_{ie_1} + \left(h_{fe_1}+1\right) R_{E_1}\right] = 30k \| 60k \| \left[108 + (21)(1k)\right] \cong 10.3\,\text{k}\Omega$$

Later, let us calculate the no-load gain $A_{v_2} = v_o/v_{i_2} = v_o/v_{o_1}$ of the second stage

$$A_{v_2} = \frac{v_o}{v_{o_1}} = \frac{-h_{fe_2} R_C}{h_{ie_2} + \left(h_{fe_2}+1\right) R_{E_2}} = \frac{-(20)(2k)}{129 + (21)(1k)} = 1.89$$

Now, let us calculate the overall gain $A_{Vs_1} = v_{o_1}/v_s$ of the first stage

$$A_{Vs_1} = \frac{v_{o1}}{v_s} = \left(\frac{R_{i_1}}{R_s + R_{i_1}}\right)\left(\frac{\left(h_{fe_1}+1\right) R_{E_1}}{h_{ie_1} + \left(h_{fe_1}+1\right) R_{E_1}}\right)$$
$$= \left(\frac{10.3k}{1k+10.3k}\right)\left(\frac{(21)(1k)}{108+(21)(1k)}\right) \cong 0.91.$$

So, the overall voltage gain A_{Vs} is given by

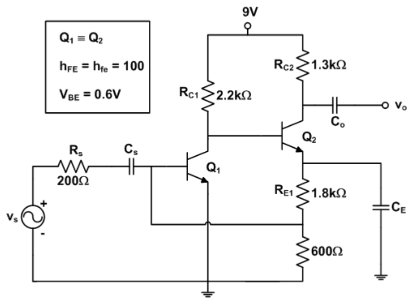
$$A_{Vs} = A_{Vs_1} \times A_{v_2} = (0.91)(1.89) = 1.72.$$

c) From $v_{CE_{1(max)}}$ and $v_{CE_{2(max)}}$ calculated in part (a), and from A_{v_2} and A_{Vs_1} calculated in part (b), we see that the limiting factor comes from the first stage. Because

$$\left(v_{CE_{1(\mathbf{max})}} < \frac{v_{CE_{2(\mathbf{max})}}}{A_{v_2}}\right) \Rightarrow \left(4.82 < \frac{12.66}{1.89}\right) \Rightarrow (4.82\,\text{V} < 6.7\,\text{V})$$

Consequently,

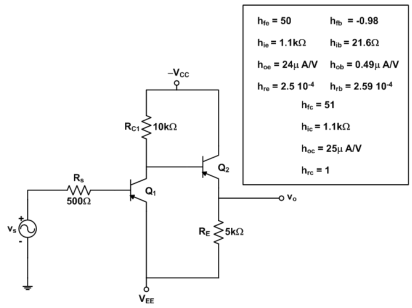
$$v_{s(\mathbf{max})} = \frac{v_{CE_{1(\mathbf{max})}}}{A_{Vs_1}} = \frac{4.82}{0.91} = 5.30\,\text{V}.$$



Example 6: For the figure above,

a) Draw AC and DC load lines for both transistors.
b) Calculate the overall voltage gain $A_{Vs} = v_o/v_s$.
c) Find $v_{s(\mathbf{max})}$ which produces maximum undistorted output voltage.

Homework 10: Solve the question given in Example 6.



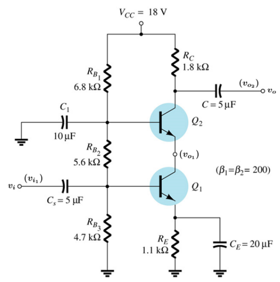
Example 7: For the figure above,

a) Calculate the overall voltage gain $A_{Vs} = v_o/v_s$.
b) Find the output resistance R_o.

Homework 11: Solve the question given in Example 7.

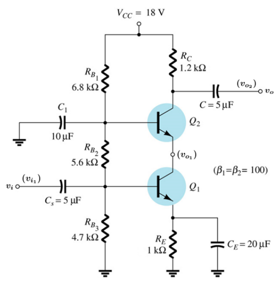
Cascode Amplifier

The cascode configuration is a CE-CB combination, where the collector of the first transistor is connected to the emitter of the second transistor as shown below.

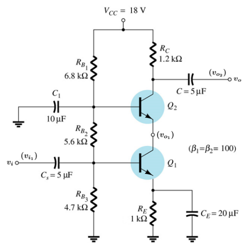


The arrangements provide a relatively high-input impedance with low voltage gain for the first CE stage to ensure the input Miller capacitance is at a minimum, whereas the following CB stage provides the high gain.

Therefore, therefore this combination works well in **high frequency** applications.



Example 8: For the cascode amplifier above, find the input resistance R_i, output resistance R_o and the voltage gain $A_v = v_o/v_i$.



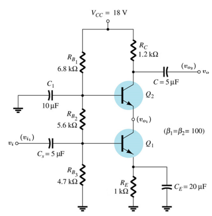
Solution: Let us perform DC analysis first and calculate I_{EQ_1}

$$I_{EQ_1} = \frac{V_{B_1} - V_{BE(ON)}}{R_E}$$

$$\cong \frac{\frac{R_{B_3}}{R_{B_1}+R_{B_2}+R_{B_3}} V_{CC} - V_{BE(ON)}}{R_E} \quad \ldots \text{ignoring } I_{B_1} \text{ and } I_{B_2} \text{ as } \beta R_E \gg R_{B_3}$$

$$= \frac{\frac{4.7k}{6.8k+5.6k+4.7k} 18 - 0.7}{1k} = \frac{4.95 - 0.7}{1k}$$

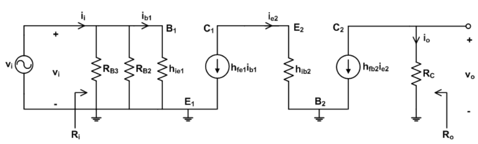
$$= 4.25\,\text{mA}$$

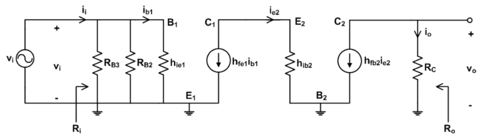


As $\alpha = 100/101 \cong 1$, $I_{EQ_1} \cong I_{CQ_1} = I_{EQ_2} \cong I_{CQ_2}$. So, $h_{ie} = h_{ie_1} = h_{ie_2}$ given by

$$h_{ie} = (h_{fe} + 1)\frac{\gamma}{I_{EQ}} = (101)\left(\frac{26m}{4.25m}\right) \cong 618\,\Omega$$

So, the SSAC equivalent circuit is given below





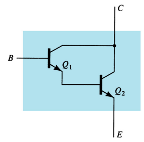
Thus, we can calculate R_i, R_o and A_v as follows

$$R_i = R_{B_3}||R_{B_2}||h_{ie_1} = 4.7k||5.6k||618 \cong 498\,\Omega$$
$$R_o = R_C = 1.2\,\text{k}\Omega$$
$$A_v = \left(\frac{v_o}{i_{e_2}}\right)\left(\frac{i_{e_2}}{i_{b_1}}\right)\left(\frac{i_{b_1}}{v_i}\right)$$
$$= \left(-h_{fb_2}R_C\right)\left(-h_{fe_1}\right)\left(\frac{1}{h_{ie_1}}\right) \qquad \ldots h_{fb} = -1$$
$$= -\frac{(100)\,(1.2k)}{0.618k} = -194.$$

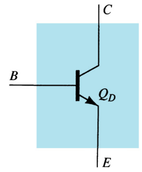
Homework 12: Show that the voltage gain $A_{V_1} = v_{o_1}/v_i = -1$ for the first stage of the amplifier. Consequently, comment on the Miller effect.

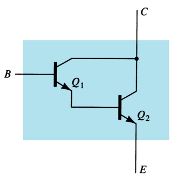
Darlington Pair

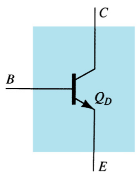
A very popular connection of npn two bipolar junction transistors for operation as one **superbeta** npn transistor is the Darlington connection shown below.



The main feature of the Darlington connection is that the composite transistor as shown below acts as a single unit with a current gain that is the product of the current gains of the individual transistors.







Consequently, current gain β_D and base-emitter turn-on voltage $V_{BE_D(ON)}$ are given as follows

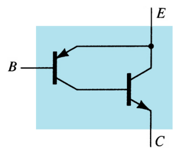
$$\beta_D = \beta_1\beta_2 + \beta_1 + \beta_2 \approx \beta_1\beta_2$$
$$V_{BE_D(ON)} = 2V_{BE(ON)}$$

Such that $I_C = \beta_D I_B$ and $I_E = (\beta_D + 1)\, I_B$ when both transistors are in the forward active mode.

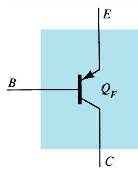
Homework 13: Show that above expressions for β_D and $V_{BE_D(ON)}$ are correct.

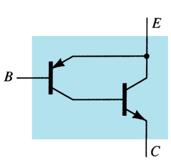
Feedback Pair

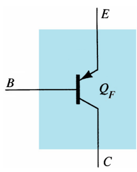
The feedback pair connection shown below is a two-transistor circuit that operates like the Darlington circuit.



Notice that the feedback pair uses a pnp transistor driving an npn transistor, the two devices acting effectively much like one pnp transistor as shown below. As with a Darlington connection, the feedback pair also provides a very high current gain.







Consequently, current gain β_F and emitter-base turn-on voltage $V_{BE_F(ON)}$ are given as follows

$$\beta_F = \beta_1\beta_2 + \beta_1 \approx \beta_1\beta_2$$
$$V_{BE_F(ON)} = V_{BE(ON)}$$

Such that $I_C = \beta_F I_B$ and $I_E = (\beta_F + 1)\, I_B$ when both transistors are in the forward active mode.

Homework 14: Show that above expressions for β_F and $V_{BE_F(ON)}$ are correct.