Emitter-Coupled Logic (ECL)

Basic ECL Inverter/Non-inverter (ECL Current Switch)

According to inverting output: 
\[ V_{in} = V_{in} - 0.05 \]
\[ V_{in} = V_{in} + 0.05 \]

Basic ECL Inverter/Non-inverter VTC

\[ V_{OH} = V_{CC} \]
\[ V_{IL} = V_{IL} \frac{V_{BE(SAT)} + V_{RC(SAT)} - V_{BC(SAT)}}{R_{E}} \]

Example

Calculate the critical VTC points for the ECL current switch:
\[ V_{CC} = 5V, \ V_{IL} = 0V, \ V_{BB} = 2.6V, \ R_{C1} = R_{C2} = R_{E} = 1k\Omega, \]
\[ V_{BE(ECL)} = 0.75V, \ V_{HIL} = 0.8V, \ V_{HIL} = 0.6V \]

\[ V_{OH} = 5V \]
\[ V_{IL} = 2.55V \]
\[ V_{IL} = 3.2V \]
\[ V_{OH} = 3.10V \]
\[ V_{OH} = 2.65V \]
\[ V_{HIL} = V_{HIL} = 2.6V \]
Basic ECL NOR/OR Gate

\[ V_{OL} = \frac{V_{OL}(ECL)}{R_{C1} + (\beta + 1)R_{BS}} - \frac{V_{BS}(ECL)}{R_{C1}} \]

\[ V_{OH} = -0.76V \]

\[ V_{IL} = -1.225V \]

\[ V_{IH} = -1.125V \]

\[ V_{LS} = 0.79V \]

\[ V_{LS} = 0.325V \]

\[ V_{LS} = 0.475V \]

\[ V_{NMH} = 0.365V \]

\[ V_{NMH} = 0.53V \]

\[ V_{NMH} = 0.75V \]

MECL I NOR/OR Gate

\[ V_{OL} = \frac{V_{OL}(ECL)}{R_{C1} + (\beta + 1)R_{BS}} - \frac{V_{BS}(ECL)}{R_{C1}} \]

\[ V_{OH} = -0.76V \]

\[ V_{IL} = -1.225V \]

\[ V_{IH} = -1.125V \]

\[ V_{LS} = 0.79V \]

\[ V_{LS} = 0.325V \]

\[ V_{LS} = 0.475V \]

\[ V_{NMH} = 0.365V \]

\[ V_{NMH} = 0.53V \]

\[ V_{NMH} = 0.75V \]

Example

Find the logical swing, noise margins and noise immunities for the MECL I circuit above.

\[ \beta = 49, V_{BE(ECL)} = 0.75V, V_{BE(FA)} = 0.75V, V_{BE(SAT)} = 0.8V, V_{BC(SAT)} = 0.6V \]

\[ V_{IL} = -1.25V \]

\[ V_{IH} = -1.125V \]

\[ V_{IL} = -1.55V \]

\[ V_{IH} = -0.76V \]
**MECL I Fanout**

\[
\text{IOH} = \frac{V_{OH} - V_{IL}}{R_{DN}}
\]

\[
\text{IBN} = \frac{V_{BE} - V_{BE}}{R_{BN}}
\]

\[
\text{IEE} = \frac{V_{BE}}{R_{EE}}
\]

\[
\text{IRE} = \frac{V_{BE}}{R_{RE}}
\]

\[
\text{IRDN} = \frac{V_{BE}}{R_{DN}}
\]

**Fan-out Example**

Find the maximum fan-out for the MECL I circuit above

\[
\beta_F = 49, \ V_{BECL} = 0.75V, \ V_{BEFA} = 0.75V, \ V_{BESAT} = 0.8V, \ V_{BCSAT} = 0.6V
\]

Assume load gates reduce \( V_{OH} \) by 0.03 volts.

\[
V_{OH} = -0.79V
\]

\[
\text{IRDN} = 2.205 mA
\]

\[
\text{IBN} = 148 \mu A
\]

\[
\text{IEE} = 7.4 mA
\]

\[
\text{IRE} = 5.2 mA
\]

\[
N = \frac{\text{IRDN}}{\text{IRE}} = 87
\]

**Power Dissipation Example**

Find the average power dissipated in the MECL I circuit above

\[
\text{IPM} = 2.64 mA
\]

\[
\text{IPE} = 2.98 mA
\]

\[
\text{IPX} = 35.6 mW
\]

**Other ECL Gates**
**DeMorgan’s Theorems**

- NOR and OR using ANDs and NANDs
  - NOR: \( \overline{A + B} = \overline{A} \cdot \overline{B} \)
  - OR: \( A + B = \overline{\overline{A} \cdot \overline{B}} \)

- NAND and AND using ORs and NORs
  - NAND: \( \overline{A \cdot B} = \overline{A} + \overline{B} \)
  - AND: \( A \cdot B = \overline{\overline{A} + \overline{B}} \)

**Example**

Implement the following logic using only ECL gates

\[(A + B)(C + D)\]

Solution:

\[(A + B)(C + D) \equiv (A + B) \cdot (C + D)\]

**Collector Dotting Wired-AND Gates**

**Complex Logic Gates with Collector Dotting**

Any combination of OR-ANDing is possible with the collector dotting design method using the following rules:

1. ORing of signals is performed by multiple input BJT current switches.
2. ANDing of ORed signals is performed by placing multiple current switch input sections in parallel.
3. A single output buffer is taken from the common collector of all current switch reference BJTs.
4. A single bias network similar to that shown in Figure 15.3a is connected to the common base and collector of the reference BJT in all current switch input sections.
**Example**

Series Gating – Basic ECL NAND/AND Current Switch

**Complex Logic Gates with Series Gating**

Any combination of OR-ANDing along with the complementing OR-AND-inverting can be obtained by obeying the following five steps:

1. ORing of signals is performed by parallel input EETs in a single emitter coupled switch.
2. ANDing of ORed signals is performed by series gating the individual current switches.
3. Output buffers are taken from both collector of the top current switch.
4. A multiple bias reference circuit is needed for each level of series gating (ANDing); the temperature compensating bias network of Figure 15.9a provides two bias voltages $V_{EB}$ and $V_{EB}$.
5. Inputs to emitter coupled switches below the top switch need to be divided down in a manner similar to $V_{CC}$ through $R_{EB}$, $R_{E1}$, and $R_{E2}$ in Figure 15.9a.