ELE 312
Digital Electronics

http://www.ee.hacettepe.edu.tr/~usezen/ele312/

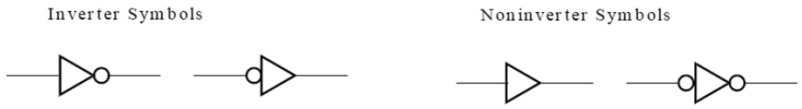
Textbooks

- DeMassa and Ciccone, ***Digital Integrated Circuits***, John Wiley & Sons.
- Taub and Schilling, ***Digital Integrated Electronics***, McGraw-Hill

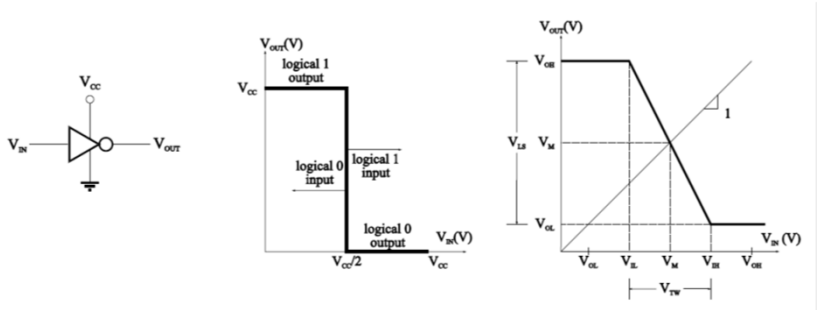
Contents

Properties of Digital Integrated Circuits

Most important elements: Inverter and Noninverter



Idealized Inverter and Voltage Transfer Characteristics (VTCs)

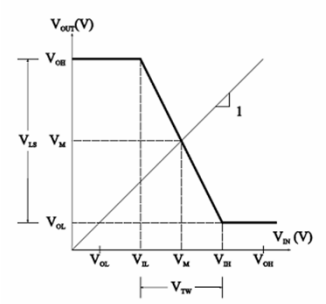


Noise Margins

High noise margin (for logical level 1) $\mathbf{V_{NMH} = V_{OH} - V_{IH}}$

Low noise margin (for logical level 0) $\mathbf{V_{NML} = V_{IL} - V_{OL}}$

Noise Sensitivities



(For logical level 1) $\mathbf{V_{NSH} = V_{OH} - V_M}$

(For logical level 0) $\mathbf{V_{NSL} = V_M - V_{OL}}$

Noise Immunities

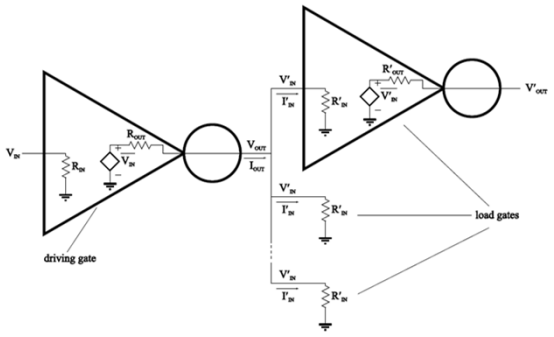
(For logical level 1) $\mathbf{V_{NIH} = \frac{V_{NSH}}{V_{LS}}}$

(For logical level 0) $\mathbf{V_{NIL} = \frac{V_{NSL}}{V_{LS}}}$

FAN-IN and FAN-OUT

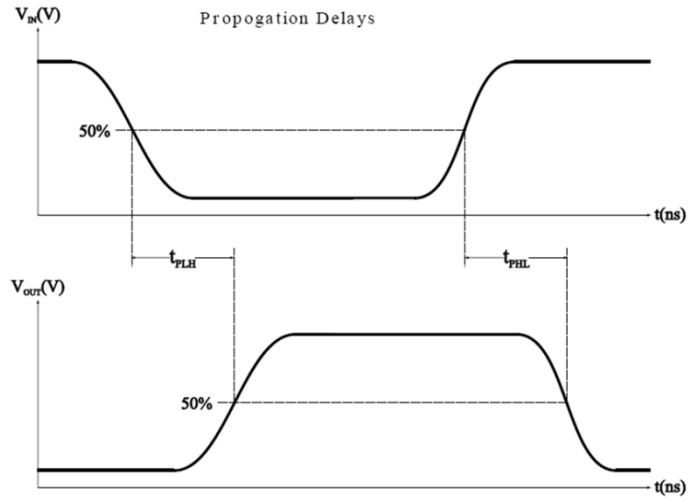
$$N_{\mathbf{high}} = \left\lfloor \frac{I_{\mathbf{OUT(high)}}}{I'_{\mathbf{IN(high)}}} \right\rfloor$$

$$N_{\mathbf{low}} = \left\lfloor \frac{I_{\mathbf{OUT(low)}}}{I'_{\mathbf{IN(low)}}} \right\rfloor$$

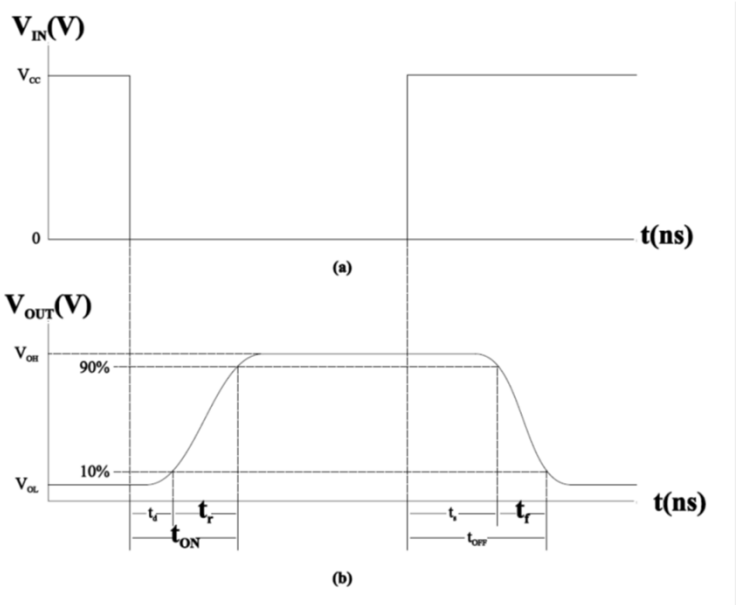


Maximum fan-out: $N_{\mathbf{max}} = \mathbf{min}\left(N_{\mathbf{high\ (max)}}, N_{\mathbf{low\ (max)}}\right)$

Propagation Delays

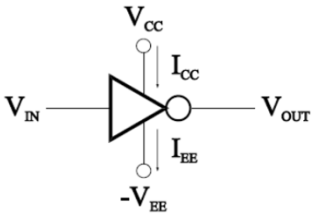


Rise and fall times and turn-on and turn-off times



Power dissipation

Average Power Dissipation = Average Power Supplied



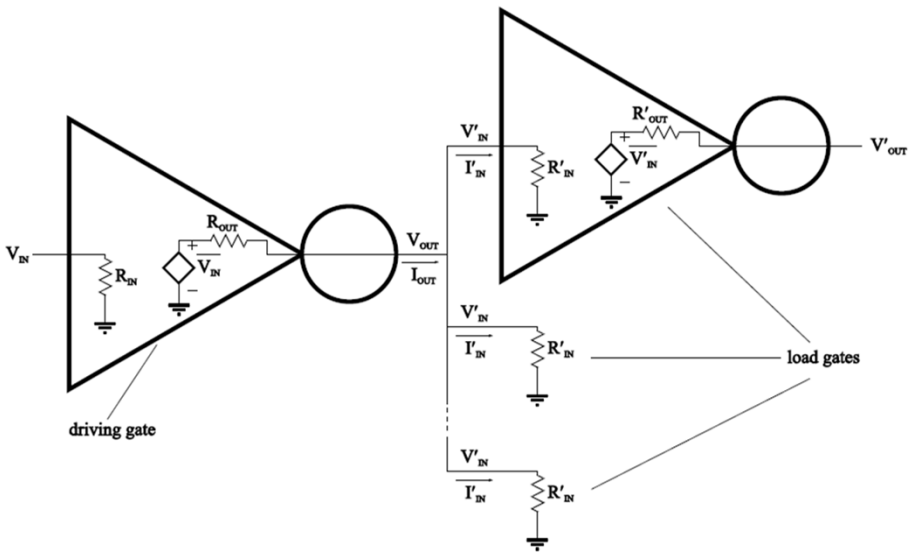
$$P_{CC} = I_{CC} V_{CC}$$

$$P_{EE} = I_{EE} V_{EE}$$

$$P_{CC(avg)} = \frac{P_{CC(OH)} + P_{CC(OL)}}{2}$$

$$P_{CC(avg)} = \frac{I_{CC(OH)} + I_{CC(OL)}}{2} V_{CC}$$

Logic Element Equivalent Circuit and Fan-out



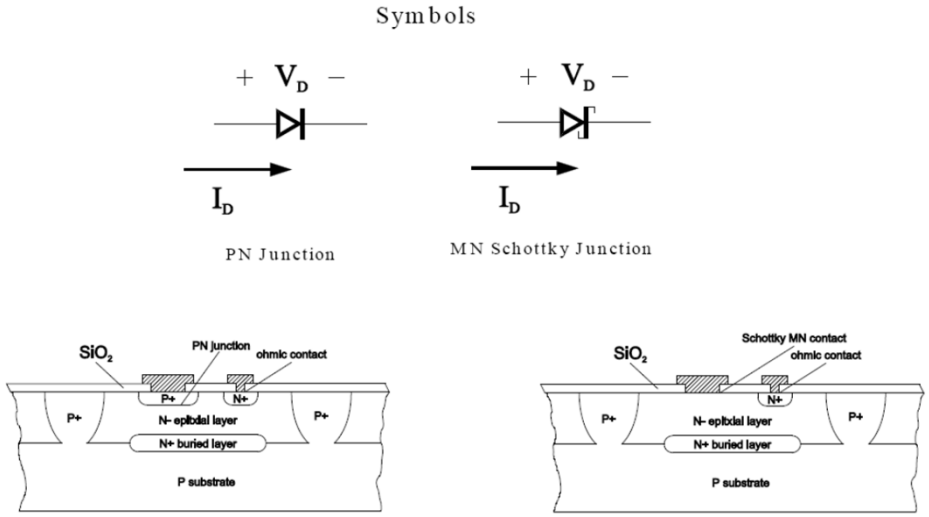
Power - Delay Product:

Speed-power product = (Average Power Diss) x (Propagation Delay)

$PD = P_{DISS(avg)} \times t_{P(avg)}$

Diode Digital Circuits

Diodes



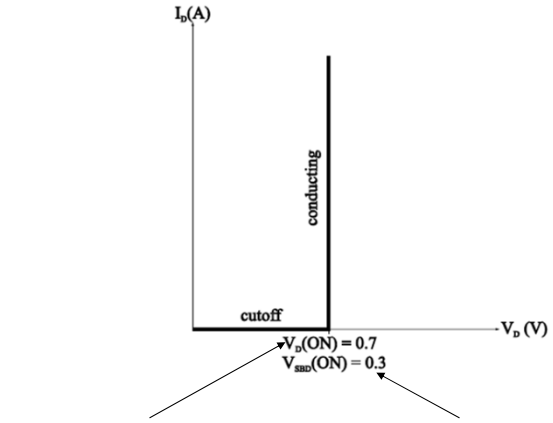
Shockleys Eq

$$I_D = I_S(e^{V_D/V_T} - 1) \quad \text{where } V_T = \frac{kT}{q}$$

for Forward Bias

$V_D \cong V_0 = 0.7$ V

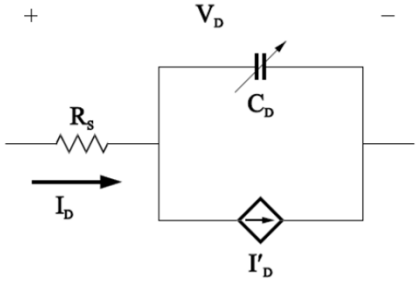
IV Characteristics



for PN Junction diodes

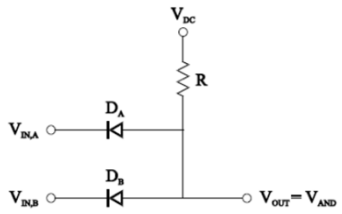
for MN Schottky diodes

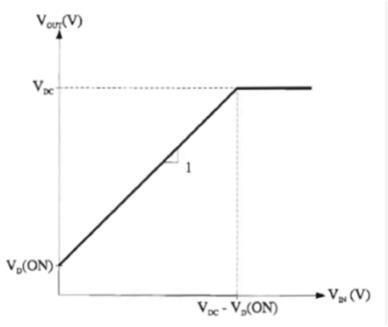
SPICE model



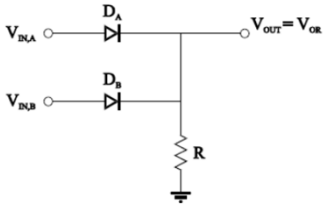
$$I'_D = I_S(e^{V_D/V_T} - 1)$$

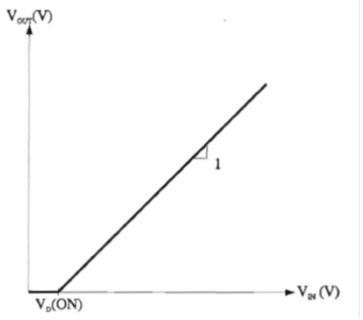
Basic Logic Gates: AND



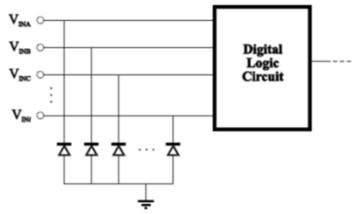


Basic Logic Gates: OR

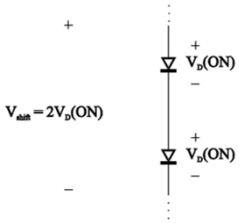




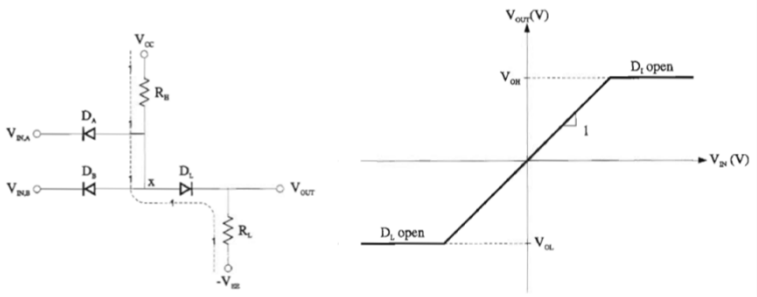
Clamping Diodes



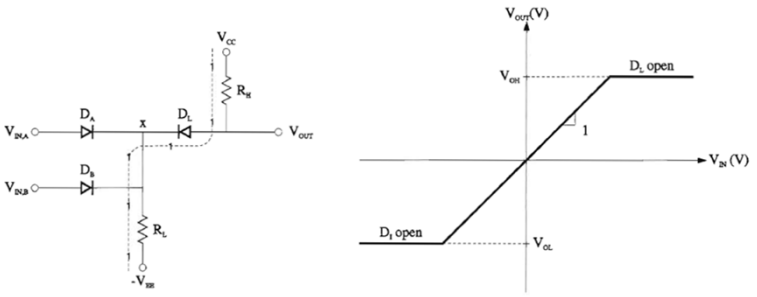
Level shifting diodes

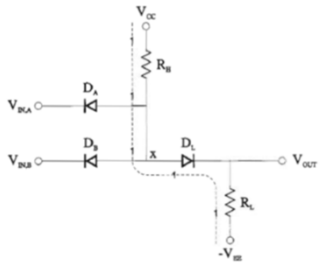


Level Shifting Diode AND Gate



Level Shifting Diode OR Gate





Ex. Find the output low and high voltages for the circuit shown above, where $V_{CC} = V_{EE} = 4V$, $V_{D(ON)} = 0.7V$, $R_H = 1k\Omega$, $R_L = 2k\Omega$.