

ELE 312
Digital Electronics

<http://www.ee.hacettepe.edu.tr/~usezen/ele312/>

Textbooks

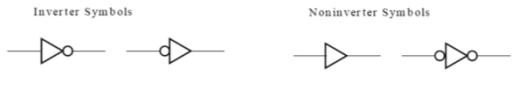
- DeMassa and Ciccone, *Digital Integrated Circuits*, John Wiley & Sons.
- Taub and Schilling, *Digital Integrated Electronics*, McGraw-Hill

Contents

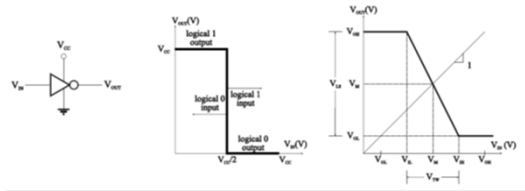
- Basic Properties of Digital Integrated Circuits
- Diode Digital Circuits
- BJT Digital Circuits
 - Ebers & Moll equations
 - Transistor modelling
 - State of transistor in a circuit
- Resistor-Transistor Logic (RTL)
- Diode-Transistor Logic (DTL)
- Transistor-Transistor Logic (TTL)
- Schottky Transistor – Transistor Logic (STTL)
- Different TTL Gates
- Emitter-Coupled Logic (ECL)
- MOS Digital Circuits
- NMOS Gates
- CMOS Gates

Properties of Digital Integrated Circuits

Most important elements: Inverter and Noninverter



Idealized Inverter and Voltage Transfer Characteristics (VTCs)



Noise Margins

High noise margin (for logical level 1) $V_{NMH} = V_{OH} - V_{IH}$

Low noise margin (for logical level 0) $V_{NML} = V_{IL} - V_{OL}$

Noise Sensitivities

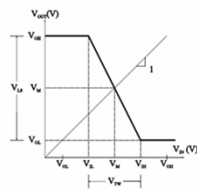
(For logical level 1) $V_{NSH} = V_{OH} - V_M$

(For logical level 0) $V_{NSL} = V_M - V_{OL}$

Noise Immunities

(For logical level 1) $V_{NIH} = \frac{V_{NSH}}{V_{LS}}$

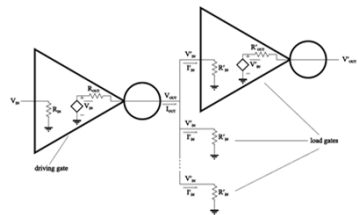
(For logical level 0) $V_{NIL} = \frac{V_{NSL}}{V_{LS}}$



FAN-IN and FAN-OUT

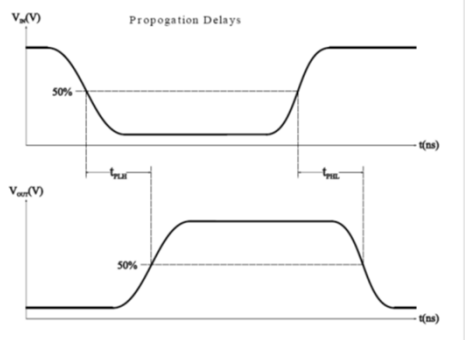
$$N_{high} = \left[\frac{I_{OUT(high)}}{I_{IN(high)}} \right]$$

$$N_{low} = \left[\frac{I_{OUT(low)}}{I_{IN(low)}} \right]$$

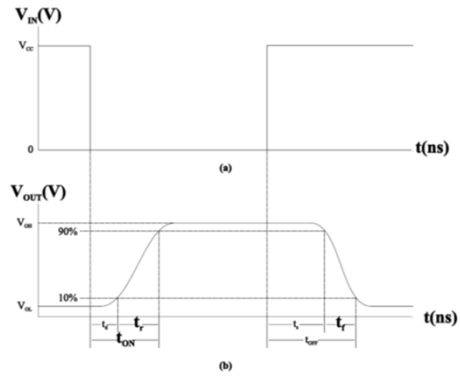


Maximum fan-out: $N_{max} = \min(N_{high(max)}, N_{low(max)})$

Propagation Delays

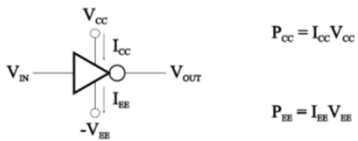


Rise and fall times and turn-on and turn-off times



Power dissipation

Average Power Dissipation = Average Power Supplied



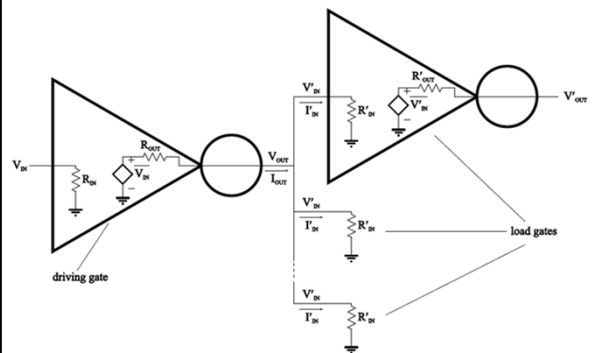
$$P_{CC} = I_{CC} V_{CC}$$

$$P_{EE} = I_{EE} V_{EE}$$

$$P_{CC(av)} = \frac{P_{CC(OH)} + P_{CC(OL)}}{2}$$

$$P_{CC(av)} = \frac{I_{CC(OH)} + I_{CC(OL)} V_{CC}}{2}$$

Logic Element Equivalent Circuit and Fan-out



Power - Delay Product:

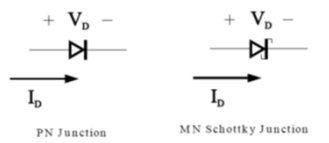
Speed-power product = (Average Power Diss) x (Propagation Delay)

$$PD = P_{DISS(avg)} \times t_{P(avg)}$$

Diode Digital Circuits

Diodes

Symbols



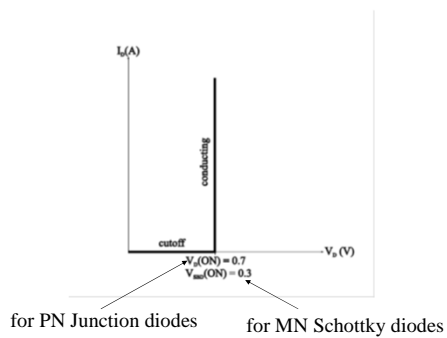
Shockleys Eq

$$I_D = I_S (e^{V_D/V_T} - 1) \quad \text{where } V_T = \frac{kT}{q}$$

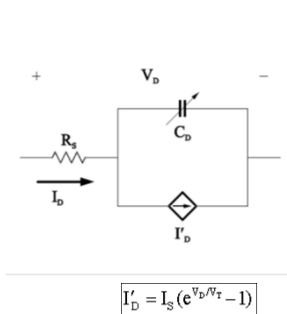
for Forward Bias

$$V_D \cong V_0 = 0.7 \text{ V}$$

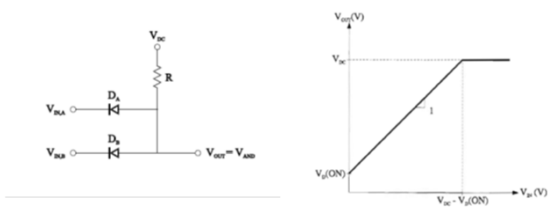
IV Characteristics



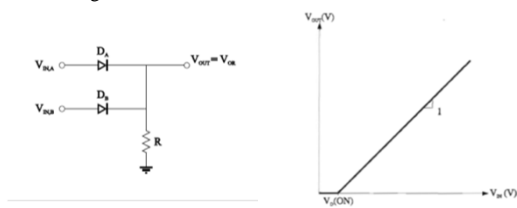
SPICE model



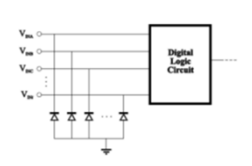
Basic Logic Gates: AND



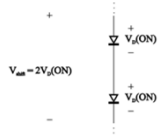
Basic Logic Gates: OR



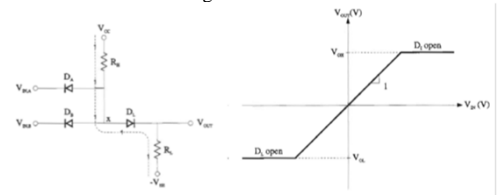
Clamping Diodes



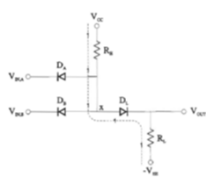
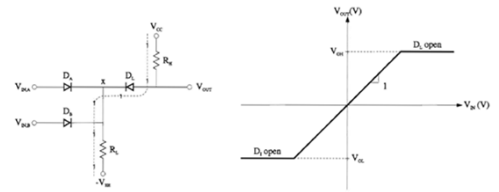
Level shifting diodes



Level Shifting Diode AND Gate



Level Shifting Diode OR Gate



Ex. Find the output low and high voltages for the circuit shown above, where $V_{CC} = V_{EE} = 4V$, $V_{D(ON)} = 0.7V$, $R_H = 1k\Omega$, $R_L = 2k\Omega$.

