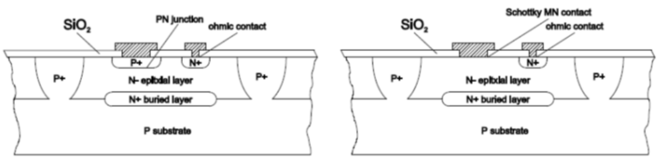
Contents

Diode Model

- Diodes are important elements in digital electronic circuits, as well as they are used to perform various logic operations, they are also used as variable capacitors, DC voltage level shifters and clamping diodes at logic circuit inputs.
- Symbols for PN junction diodes and MN junction diodes are shown in the figures left and right below, respectively.

- PN junction diodes are formed from the combination of P-type and N-type regions. Usually, PN junctions in integrated circuits (ICs) are usually formed by utilizing the two out of the three regions of a bipolar junction transistor, instead of a separate device structure. Turn-on voltage for a PN junction diode is $V_{D(ON)} = 0.7\,$V.
- MN junction (Schottky Barrier) diodes are formed from the combination of a metal and an N^--type semiconductor. Metal used in MN junction diodes is mostly platinum silicide (Pt_5Si_2). As there are no holes present, MN junction diodes are much faster than PN junction diodes. Turn-on voltage for a Schottky Barrier (MN junction) diode is $V_{SBD(ON)} = 0.3\,$V.

- Cross sections of some example PN and MN junction diodes as shown in the figures left and right below, respectively, in order to highlight some of the fabrication properties.

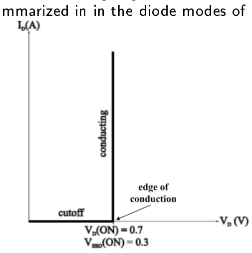


- Diode current-voltage (IV) characteristics are normally governed by the well-known Shockley's diode equation,

$$I_D = I_S \left(e^{V_D/\gamma} - 1 \right)$$

where I_S is the reverse saturation current (typically pA for PN junction diodes and μA for MN junction diodes) and $\gamma = \phi_T = kT/q$ is the thermal voltage (typically $\gamma = 26\,$mV at $300\,$K) with k representing the Boltzman constant, T representing the temperature in kelvins and q representing the elementary charge.

- In the analysis of digital circuits, we are going to use the **simplified diode model** as shown in the figure and summarized in in the diode modes of operation table below

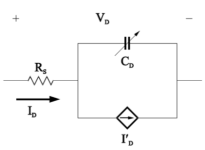


- The transition point from cutoff mode to conduction mode (i.e., when the current is not yet flowing) is called as **edge of conduction** (EOC).

Diode Modes of Operation

Junction Bias	Mode of Operation
Reverse	Cutoff (OFF)
Forward	Conducting (ON)

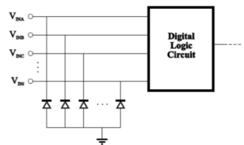
- The large signal diode model used in SPICE in shown in the figure below.



- PN Junction capacitance can be utilized in ICs by applying a negative bias to a diode. Diodes used for this purpose are referred to as **varactor** diodes and have the modified circuit symbol presented in the figure below.

Clamping and Level-Shifting Diodes

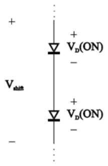
- When the input to a gate is switched from high-to-low, the input voltage sometimes swings well beyond $0\,$V. This is called as ringing and may cause physical damage to the gate.
- Connecting **clamping** diodes to each input of a gate, as shown in the figure below, eliminates this problem by preventing inputs from falling below $-0.7\,$V. The diodes will not affect the operation of the gate, as the diodes are open circuit for positive inputs.



- Clamping diodes can be also connected to the output(s) of a gate.
- Most TTL/STTL families employ clamping diodes at their inputs and sometimes also at their outputs.

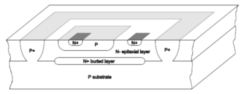
- It is often required to change the voltage level across particular portions of digital circuits, e.g., to level shift the output voltage.
- Another use of the diode forward voltage is to ensure that sub-circuits with complementary objectives are not conducting simultaneously. For example, TTL circuits employ two output drivers. Only one driver should be working for the output-low state, while only the other driver should be working for the output-high state. Placement of a voltage level-shifting device between the two drivers ensures the desired operation by allowing only one driver to be on at a time.

  Example 1: For the circuit below, determine the level-shifting voltage V_{shift}.

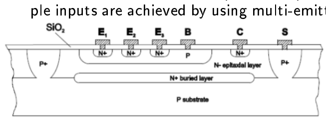


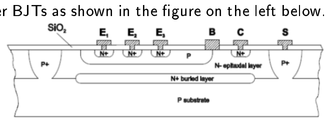
BJT Transistors

- Bipolar junction transistors (BJTs) are very important in digital circuits, e.g., TTL circuits are based on BJTs. Figure below shows a 3D cross-section (without metallization) of an NPN BJT fabricated with the junction isolated technology.



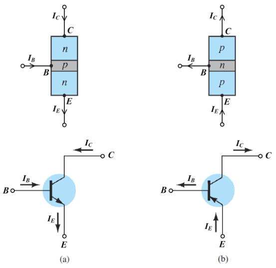
- In some BJT logic families (e.g., TTL), multiple inputs are achieved by using multi-emitter BJTs as shown in the figure on the left below.



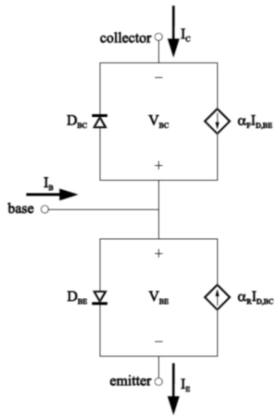


- A multi-emitter **Schottky-clamped BJT** (SBJT) is shown in the figure on the right above. The base contact is extended over the N collector region, thus placing a Schottky Barrier (MN) diode in parallel with the base-collector PN junction. This device operates much faster than a normal BJT, and an SBJT does not go into saturation mode.

- The most frequently used notation and symbols for BJT transistors are shown in the figure below for the NPN and PNP transistors.



Ebers-Moll BJT Model



$$I_{D,BE} = I_{ES}\left(e^{V_{BE}/\gamma} - 1\right)$$
$$I_{D,BC} = I_{CS}\left(e^{V_{BC}/\gamma} - 1\right)$$

I_{ES}: base-emitter reverse saturation current,
I_{CS}: base-collector reverse saturation current,
γ: thermal voltage ($kT/q = 26\,\text{mV}$ at $300\,\text{K}$).

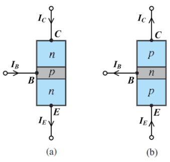
$$I_E = I_{D,BE} - \alpha_R I_{D,BC}$$
$$I_C = \alpha_F I_{D,BE} - I_{D,BC}$$
$$I_B = I_E - I_C$$

α_F and α_R are the common base **forward** and **reverse** amplification factors.
(typically $\alpha_F \approx 1$ and $0.2 \leq \alpha_R \leq 0.6$)

Reciprocity theorem:

$$I_S = \alpha_F I_{ES} = \alpha_R I_{CS}$$

I_S is known as the transport saturation current.



- A BJT transistor has two PN junctions: the base-emitter PN junction (BE junction) and the base-collector PN junction (BC junction), as depicted in the figure above. As either junction can be forward or reverse biased, there are four modes of operation (or four transistor states) as shown in the table below.

BJT Modes of Operation

BE Junction Bias	BC Junction Bias	Mode of Operation
Reverse	Reverse	Cutoff (OFF)
Forward	Reverse	Forward Active (FA)
Reverse	Forward	Reverse Active (RA)
Forward	Forward	Saturation (SAT)
		(Forward Saturation (FSAT) or Reverse Saturation (RSAT) in reality)

Cutoff (OFF)

- In the **cutoff** (OFF) mode, both PN junctions (BE and BC) of the BJT are reverse-biased. If we assume simplified diode model for the PN junctions in the Ebers-Moll model, both $I_{D,BE}$ and $I_{D,BC}$ are zero. Consequently,

$$I_{E(OFF)} = 0$$
$$I_{C(OFF)} = 0 \quad \text{and} \quad I_{B(OFF)} = 0$$

Forward Active (FA)

- In the **forward active** (FA) mode, the base-emitter PN junction (BE) is forward biased and the base-collector PN junction is reverse biased. In the Ebers-Moll model, $I_{D,BC}$ becomes zero. Consequently,

$$V_{BE(FA)} = 0.7\,\text{V}$$
$$I_{C(FA)} = \beta_F I_{B(FA)} \quad \text{or} \quad I_{C(FA)} = \alpha_F I_{E(FA)}$$

where β_F is the common-emitter current amplification factor given by

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F}$$

Similarly, α_F can also be expressed in terms of β_F as

$$\alpha_F = \frac{\beta_F}{\beta_F + 1}$$

Reverse Active (RA)

- In the **reverse active** (RA) mode, the base-emitter PN junction (BE) is reverse biased and the base-collector PN junction is forward biased. In the Ebers-Moll model, $I_{D,BE}$ becomes zero. Consequently,

$$V_{BC(RA)} = 0.7\,\text{V}$$
$$-I_{C(RA)} = (\beta_R + 1)\, I_{B(RA)} \qquad (I_{C(RA)} < 0)$$

or

$$I_{E(RA)} = \alpha_R I_{C(RA)} = -\beta_R I_{B(RA)} \qquad (I_{E(RA)} < 0)$$

where β_R is the reverse active current amplification factor (typically $0.1 \leq \beta_R \leq 2.0$) given by

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R}$$

Similarly, α_R can also be expressed in terms of β_R as

$$\alpha_R = \frac{\beta_R}{\beta_R + 1}$$

- Note that, negative values for currents mean that currents flow in the reverse directions. In other words, negative I_E and I_C mean that the current is flowing into the emitter and out of the collector for an NPN transistor, and into the collector and out of the emitter for a PNP transistor.

Saturation (SAT)

In the **saturation** (SAT) mode, both PN junctions (BE and BC) are forward biased. Normally, we only consider the case called **forward saturation** where base-emitter junction has a stronger bias (i.e., $V_{BE} \geq V_{BC}$ for NPNs). The opposite case ($V_{BC} > V_{BE}$ for NPNs) is called **reverse saturation** and rarely occurs in digital circuits.

- **Forward Saturation (FSAT)**: In this mode, base current is large and collector and emitter currents are saturated such that $I_C < \beta_F I_B$. Note that, in this mode I_C and I_E are **positive**.

$$I_{C(FSAT)} < \beta_F I_{B(FSAT)}$$
$$V_{BE(FSAT)} = 0.8\,\text{V}$$
$$V_{BC(FSAT)} = 0.6\,\text{V}$$
$$V_{CE(FSAT)} = 0.2\,\text{V}$$

A saturation parameter σ is defined to indicate the relationship between I_C and I_B as

$$\sigma = \frac{I_C}{\beta_F I_B}$$

where $\sigma \leq 1$. Note that σ is not constant, it changes according to the operating point, and $\sigma = 1$ denotes forward active operation and/or edge of saturation operation. If it is not given, you may assume $\sigma_{\textbf{max}} = 1$.

- **Reverse Saturation (RSAT)**: In this mode, base-collector junction has a stronger bias, i.e., $V_{BC} > V_{BE}$ for NPNs, and collector and emitter currents are saturated such that $-I_E < \beta_R I_B$. Note that, in this mode I_C and I_E are **negative**.

$$-I_{E(RSAT)} < \beta_R I_{B(RSAT)}$$
$$-I_{C(RSAT)} < (\beta_R + 1)\, I_{B(RSAT)}$$
$$V_{CE(RSAT)} < 0 \qquad \text{(for NPNs)}$$

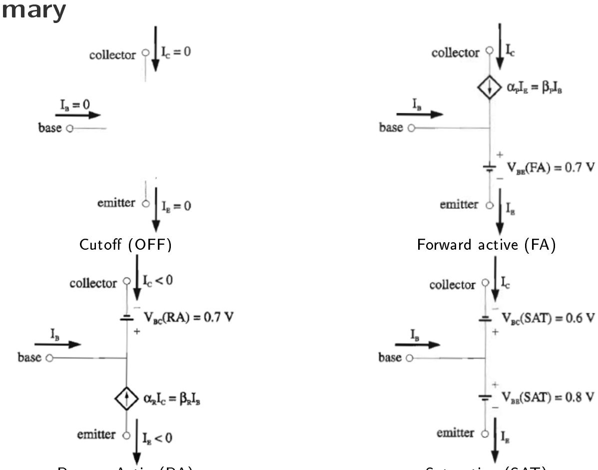
In this course, we are going to refer forward saturation (FSAT) mode as the only **saturation** (SAT) mode, i.e.,

$$SAT = FSAT.$$

In **all** operation modes (FSAT, RSAT etc.) the following must hold:

1. I_C and I_E always have the same sign, i.e., always in the same direction,
2. Base current is always nonnegative, i.e., $I_B \geq 0$,
3. KCL is satisfied, i.e., $I_E = I_C + I_B$,
4. KVL is satisfied, i.e., $V_{CE} = V_{BE} - V_{BC}$.

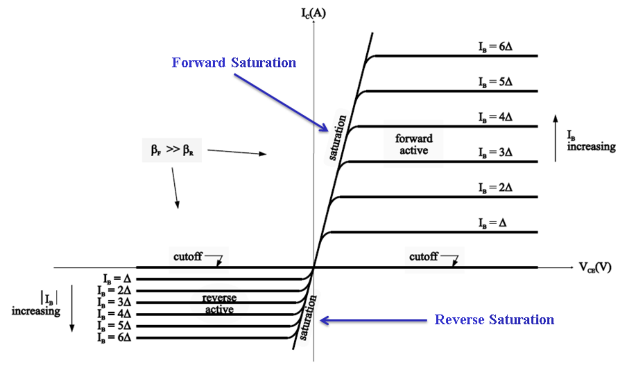
Summary



Cutoff (OFF) — Forward active (FA) — Reverse Active(RA) — Saturation (SAT)

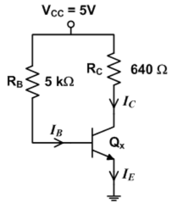
Simplified NPN BJT Model		
State	**Circuit Behaviour**	**Test Condition**
Cutoff (OFF)	$I_C = 0$, $I_E = 0$, $I_B = 0$	$V_{BE} < V_{BE(FA)}$, $V_{BC} < V_{BC(RA)}$
Forward Active (FA)	$V_{BE} = V_{BE(FA)}$, $I_C = \beta_F I_B$	$V_{BC} < V_{BC(RA)}$, $V_{CE} > V_{CE(FSAT)} > 0$
Reverse Active (RA)	$V_{BC} = V_{BC(RA)}$, $I_C = -(\beta_R + 1) I_B$	$V_{BE} < V_{BE(FA)}$, $V_{CE} < V_{CE(RSAT)} < 0$
Forward Saturation (FSAT) [Saturation (SAT)]	$V_{CE} = V_{CE(FSAT)}$, $V_{BE} = V_{BE(FSAT)}$ $V_{BC} = V_{BC(FSAT)}$	$I_C < \beta_F I_B$, $I_C > 0$, $I_E > 0$, $V_{CE} > 0$, $I_B > 0$.
Reverse Saturation (RSAT)	$V_{CE} = V_{CE(RSAT)}$, $V_{BE} = V_{BE(RSAT)}$ $V_{BC} = V_{BC(RSAT)}$	$-I_C < (\beta_R + 1) I_B$, $I_C < 0$, $I_E < 0$, $V_{CE} < 0$, $I_B > 0$.

IV Characteristics

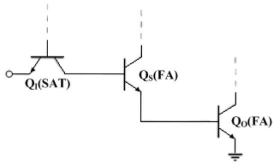


- Figure above shows a set of I_C versus V_{CE} characteristics for changes in I_B (of amount Δ). For equal increments in I_B, the curves in the active regions are approximately evenly spaced, although the curves in the reverse active region are much closer than those in the forward active region.

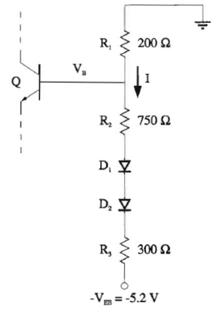
Example 2: For the circuit below, determine the state of the transistor and find currents I_B, I_C and I_E, given $\beta_F = 65$.



Example 3: For the circuit below, determine the voltages at the base and emitter of each BJT.

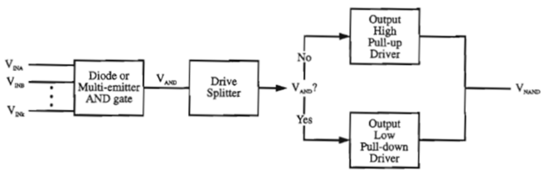


Example 4: For the circuit below, determine I and V_B. Assume the BJT base current is negligible.



BJT Sub-Circuits

- In order to provide a preview to succeeding chapters, this subsection introduces sub-circuits common to all TTL families summarized by the NAND block diagram in the figure below.



Input Section

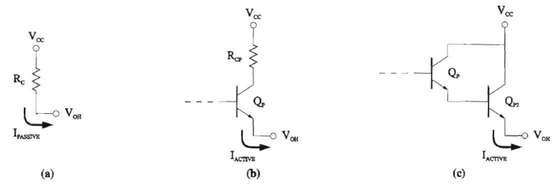
- For this NAND diagram, input section consists of ANDing of all inputs either with a parallel diode configuration or with a multi-emitter BJT.

Drive Splitter

- Depending on the result of ANDing, the **drive splitter** turns on one of the two output sections, namely output low and output high driver sections. A typical drive splitter is a BJT acting as a switch, when it is cutoff mode it activate the output-high driver and when it is in saturation mode it activates the output-low driver. Driver splitter section also provides an inversion operation.

Output-High Pull-Up Driver

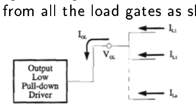
- As the output goes low-to-high, current is required to charge the equivalent input-capacitance of the load gates. Output-high pull-up driver provides the current for this charging. Some example pull-up driver sub-circuits are shown in the figure below.



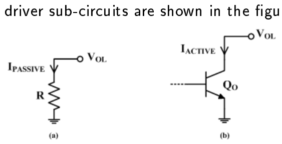
- A simple voltage driven resistor, also known as **passive pull-up**, would serve the purpose as shown in the figure (a) above.
- An emitter-follower shown in the figure (b) above is an **active** solution which provides a higher output current and hence provides faster switching time for the load gates. For even more sourcing current, a Darlington pair can be used as shown in the figure (c) above.
- Active pull-up circuitry also provides greater fan-out.

Output-Low Pull-Down Driver

- There are two purposes of output-low pull-down circuits: one is to discharge the capacitive load by providing a large sinking current, and another is to provide larger fan-out by sinking currents I_{IL} from all the load gates as shown in the figure below.



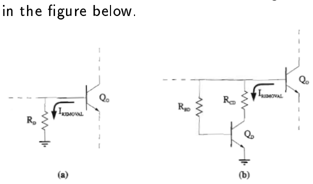
- Some example pull-down driver sub-circuits are shown in the figure below.



- A simple resistor connected to a negative power supply (or ground), also known as **passive pull-down**, would serve the purpose as shown in the figure (a) above.
- A BJT, as shown in the figure (b) above, will server as an **active pull-down** in **saturation** mode.
- Another advantage of active pull-down or pull-up circuits is that they can be activated and/or deactivated, apart from increasing fan-out.

Discharge Paths

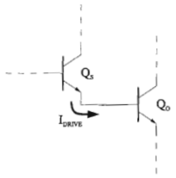
- In order to turn off a saturated BJT, all of the stored charges in the base region must be removed. A path must therefore be available for base discharge. Some example discharge sub-circuits are shown in the figure below.



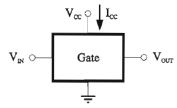
- Figure (a) above displays a circuit with an additional resistor R_D that provides passive charge removal.
- Figure (b) above shows an active configuration for stored charge removal, which provides a much faster discharge (i.e., higher discharge current) than R_D itself.

Base Driving Circuitry

- On the other hand, the turn-on time of a BJT is dependent on the time required to charge the base of the BJT. Active base driving current is often supplied to BJTs to ensure a shorter turn-on time.
- An emitter-follower BJT configuration, as shown in the figure below where Q_S drives base driving current to Q_O, usually supplies this driving current.



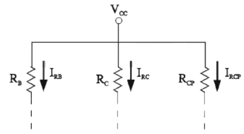
Power Dissipation of BJT Logic Circuits



- When BJT logic circuits have a single power supply, as shown in the figure above, the power dissipation for a particular gate in a particular state is taken as the power supplied given by

$$P_{CC} = I_{CC}V_{CC}$$

where I_{CC} is the current drawn from V_{CC} and is obtained by **summing all** the currents leaving the supply voltage source.



- For example, for the figure above, the current supplied by V_{CC} is

$$I_{CC} = I_{RB} + I_{RC} + I_{RCP}.$$

- Consequently, the average power dissipated in a logic circuit with two output states (output-low and output-high) is defined as

$$P_{CC(avg)} = \frac{I_{CC(OL)} + I_{CC(OH)}}{2} V_{CC}$$

Example 5: For the circuit below, calculate the average power dissipation for this gate, if $I_{RB(OH)} = 1.55\,$mA, $I_{RC(OH)} = 24.7\,\mu$A, $I_{RCP(OH)} = 1.21\,$mA, $I_{RB(OL)} = 1.14\,$mA, $I_{RC(OL)} = 4.48\,$mA and $I_{RCP(OL)} = 104\,\mu$A.