ELE315 Electronics II
Digital Circuits

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Dr. Umut Sezen & Dr. Dinçer Gökcen

Department of Electrical and Electronic Engineering
Hacettepe University

Digital Circuits

- Basic Properties of Digital Integrated Circuits
- Diode and BJT Digital Circuits (Ebers & Moll equations, transistor modelling, state of transistors in a circuit)
- Resistor-Transistor Logic (RTL)
- Diode-Transistor Logic (DTL)
- Transistor-Transistor Logic (TTL)
- Different TTL Gates
- NMOS Gates
- CMOS Gates

Digital Circuits Textbook

1. DeMassa and Ciccone, ***Digital Integrated Circuits***, John Wiley & Sons.

Contents

Properties of Digital Integrated Circuits

We are going to introduce the general properties and definitions common to all digital integrated circuit families. These properties and definitions include **voltage transfer characteristic (output voltage vs. input voltage)**, **Fan-in**, **Fan-out**, **power dissipation** and **propagation delay**.

Five basic logic operations, namely NOT, AND, OR, NAND and NOR, are used to investigate the properties of digital circuits, because any complex logical operation can be implemented by these five logic operations. The electronic circuit which performs one of these logic functions is called as a **gate**. The logic gates that perform one or more of the basic operations are called combinational gates.

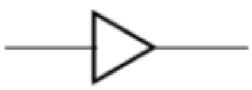
The voltages (or currents) in digital logic circuits have two possible states corresponding to two binary variables: **0** and **1**. We usually define the **LOW** voltage to correspond to a binary **0** and the **HIGH** voltage to correspond to a binary **1**.

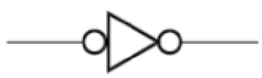
As we can obtain an **inverter** (or **non-inverter**) from NOR and NAND (or from OR and AND gates), we are going to analyze the properties of digital circuit families mostly by starting with the analysis of the inverter or non-inverter gate.

Inverter and Non-Inverter Gates

- Figures below show the circuit symbols for the **inverter** gate. The small circle denotes logical inversion (it makes no difference whether the inverting circle is at the input or output). That is, if the input voltage is **low**, the output voltage will be **high** and vice versa. This gate is also referred to as a NOT gate, since it performs the logical NOT operation.

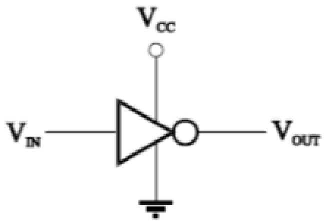
- Figures below show the circuit symbols for the **non-inverter** gate, or sometimes referred to as a **buffer**.





Ideal Inverter

Figure on the left below shows an ideal inverter gate operating with a single power supply, V_{CC}.



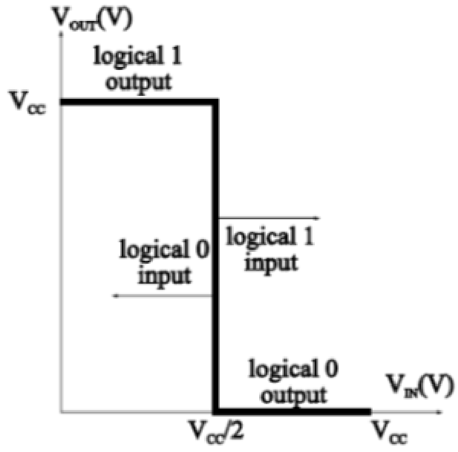
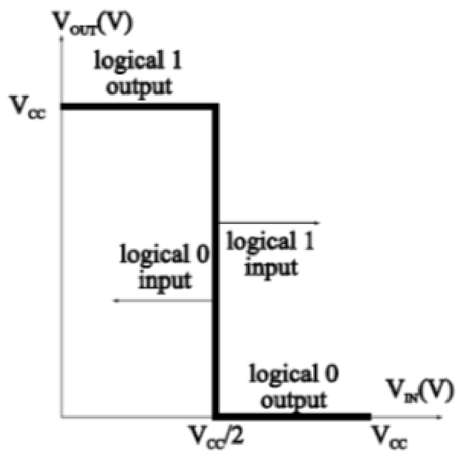


Figure on the right above shows the voltage transfer characteristic (VTC) of the ideal inverter gate, where the logical **1** is ideally at the power supply voltage V_{CC} and the logical **0** is ideally at ground ($0\,\text{V}$). Logic gates with output voltage transitions from ground to the power supply voltage are called to operate **rail-to-rail**.



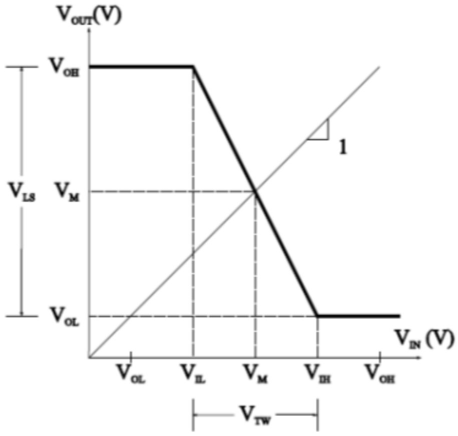
The transition between output logic states ideally occurs abruptly at an input value of $V_{CC}/2$. Thus, logical input **0** (or **input LOW**) is represented by the voltage range $0 \leq V_{IN} < V_{CC}/2$.

Similarly, logical input **1** (or **input HIGH**) is represented by the voltage range $V_{CC}/2 < V_{IN} \leq V_{CC}$.

The input voltage $V_{IN} = V_{CC}/2$ has an undefined output and will cause unpredictable results, and is therefore avoided.

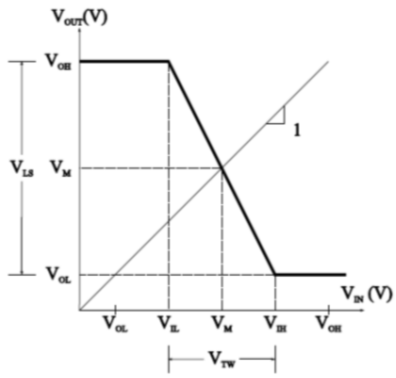
Inverter Voltage Transfer Characteristic

Figure below shows the linearized form of the voltage transfer characteristic (VTC) of an inverter.



- Indicated on the output axis are the voltages V_{OH} and V_{OL} which correspond to the **output high** and **output low** voltage levels, respectively.
- On the input axis, V_{IL} is the maximum input voltage that is considered as a LOW input (i.e., that provides a HIGH output), and V_{IH} is the minimum input voltage that is considered as a HIGH input (i.e., that provides a LOW output).

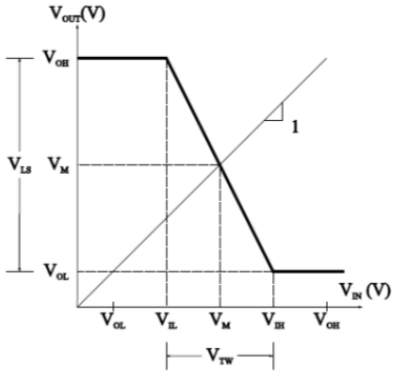
$$V_{IN} = \begin{cases} \textbf{LOW}, & \text{if } V_{IN} \leq V_{IL} \\ \textbf{HIGH}, & \text{if } V_{IN} \geq V_{IH} \\ \text{undefined}, & \text{if } V_{IL} < V_{IN} < V_{IH} \end{cases}$$



- Note that, output voltages V_{OL} and V_{OH} for the current inverter will be the **inputs** for the **next inverter**. If we want these outputs V_{OL} and V_{OH} to be considered LOW and HIGH, respectively, for the next inverter, then we must always have

$$V_{OL} < V_{IL}$$
$$V_{OH} > V_{IH}.$$

- One of the critical points labelled on the VTC graph is the midpoint voltage, V_M, which is defined as the point on the transfer characteristic where $V_{OUT} = V_{IN}$ and ideally should appear at the center of the transition region. V_M can be found graphically by drawing the $V_{OUT} = V_{IN}$ line (the unity slope line) on the VTC and finding its intersection with the VTC.



- Logic swing, V_{LS}, is defined as the magnitude of the voltage difference between the output high and low voltage levels, i.e.,

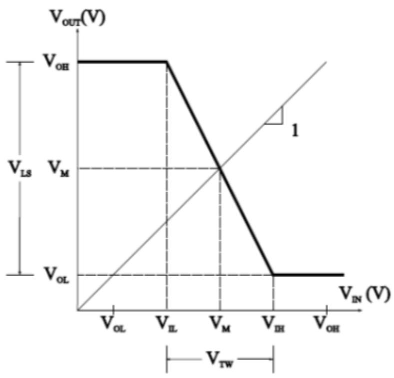
$$V_{LS} = V_{OH} - V_{OL}$$

- Transition width, V_{TW}, is defined as the magnitude of the voltage difference between V_{IH} and V_{IL} voltage levels, i.e.,

$$V_{TW} = V_{IH} - V_{IL}$$

- The low and high voltage **noise margins**, V_{NML} and V_{NMH}, represent a safety margin for low and high voltage levels, respectively.

$$V_{NML} = V_{IL} - V_{OL}$$
$$V_{NMH} = V_{OH} - V_{IH}$$



- The effects of input variations are also quantified in terms of the **noise sensitivities**. The low and high noise sensitivities are defined as the difference between the input and midpoint voltage for V_{IN} at V_{OL} and V_{OH}, respectively, i.e.,

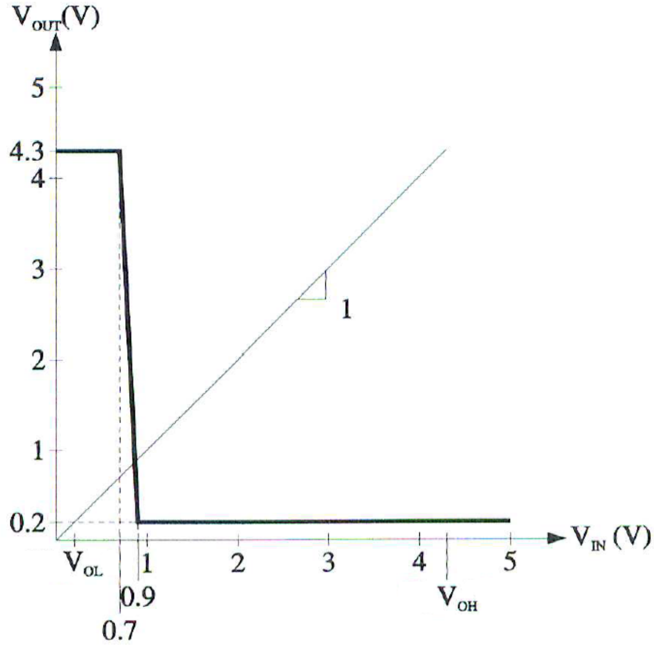
$$V_{NSL} = V_M - V_{OL}$$
$$V_{NSH} = V_{OH} - V_M$$

- The quantity **noise immunity** is the ability of a gate to reject noise, and defined as the ratio of noise sensitivities and the logical swing, i.e.,

$$V_{NIL} = \frac{V_{NSL}}{V_{LS}}$$
$$V_{NIH} = \frac{V_{NSH}}{V_{LS}}$$

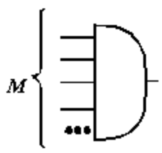
VTC Example

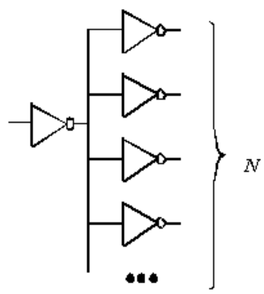
Example 1: For the circuit below, determine V_{OL}, V_{OH}, V_{IL}, V_{IH}, V_M, V_{TW}, V_{LS}, V_{NML}, V_{NMH}, V_{NSL}, V_{NSH}, V_{NIL} and V_{NIH}.



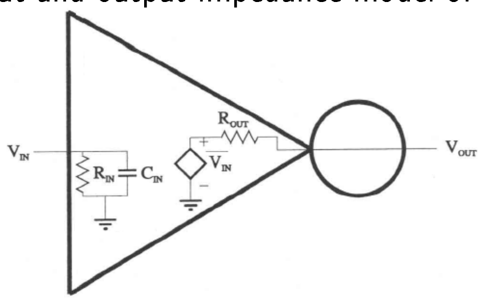
Fan-In and Fan-Out

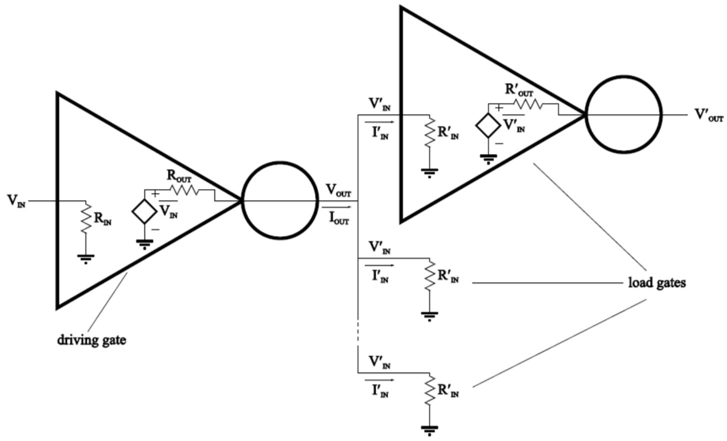
- A general logic gate has multiple inputs and multiple outputs. By multiple outputs, we mean the output of a given gate is connected to (i.e., driving) the inputs of several load gates.
- The term **fan-in** is used to describe the number of inputs of a gate, as shown in the figure on the left below. Similarly, the term **fan-out** is used to describe the number of outputs of a gate, as shown in the figure on the right below.





- Figure below shows the input and output impedance model of an inverter.





- **Maximum fan-out** of a digital logic circuit is the maximum number of load gates that can be connected to the output of a gate in parallel as shown in the figure above. From the static behaviour point of view, it is restricted by its input and output currents,

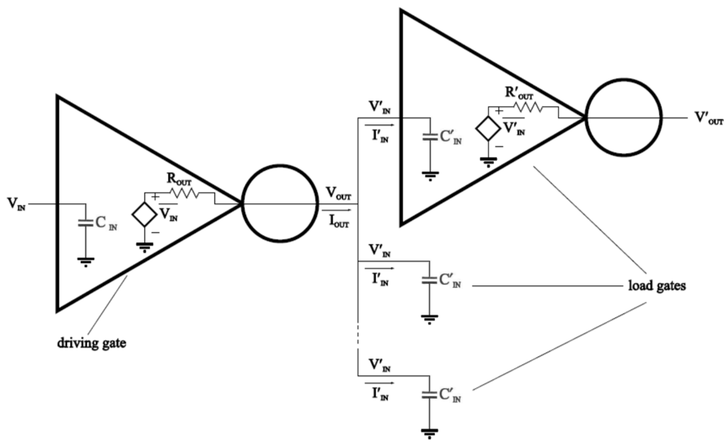
$$N_{\mathsf{max}} = \min\left(N_{OL(\mathsf{max})}, N_{OH(\mathsf{max})}\right)$$

where

$$N_{OL(\mathsf{max})} = \left\lfloor \frac{I_{OL(\mathsf{max})}}{I'_{IL}} \right\rfloor$$

$$N_{OH(\mathsf{max})} = \left\lfloor \frac{I_{OH(\mathsf{max})}}{I'_{IH}} \right\rfloor$$

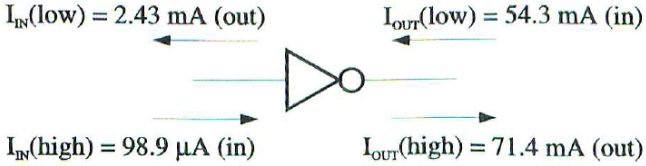
and $\lfloor \cdot \rfloor$ denotes the floor function.



- As input current of MOSFET's is the infinitesimal gate current, this might suggest that logic circuits with MOSFETs will have an infinite fan-out. However, this is not the case. Fan-out of MOSFET digital circuits is limited by the input capacitance of the gate which is the gate oxide capacitance due to dynamic behaviour. As you see in the figure above, equivalent load capacitance will be higher (parallel capacitances are added together) limiting the maximum operating frequency. In other words, maximum required operating frequency will limit the maximum number of load gates.

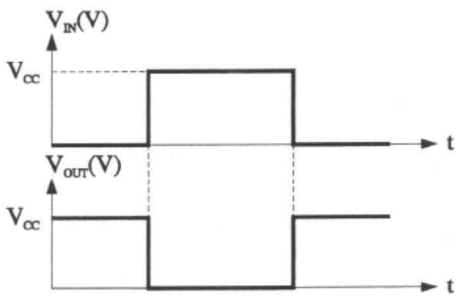
Fan-Out Example

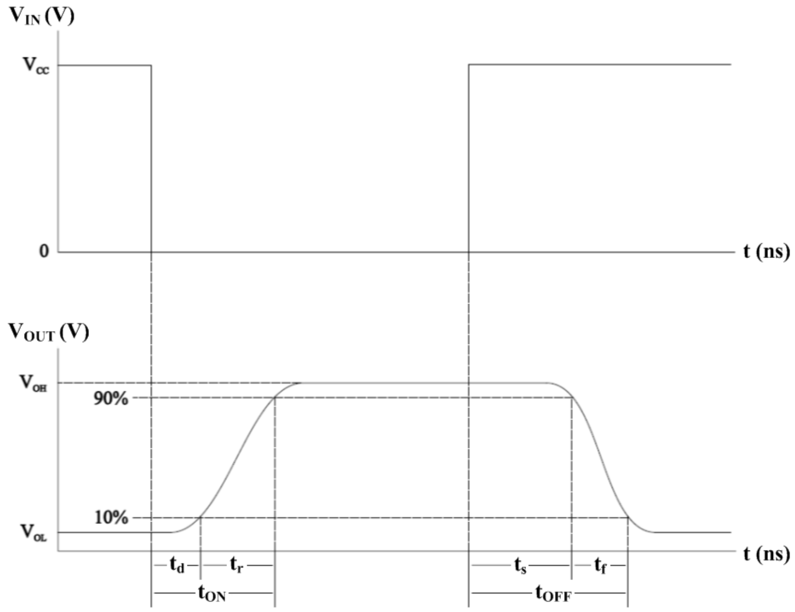
Example 2: For the circuit below, calculate the maximum fan-out.



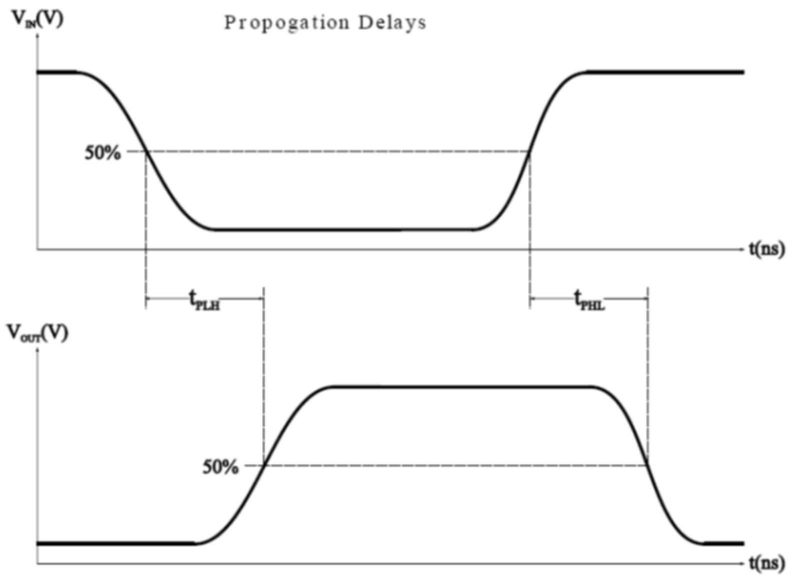
Transient Characteristics

- Digital circuits have finite **switching speeds**, i.e., switching a voltage from high to low (or low to high) requires a finite amount of time called **turn-on** t_{ON} and **turn-off** t_{OFF} time.
- Additionally, when the input voltage changes from one level to another, the output voltage is delayed in time, which is referred to as **propagation delay**.
- For digital circuits employing BJTs, these time limitations are caused by the time required to store and remove charge from the base region.
- Similarly, transient characteristics of digital circuits employing MOSFETs are limited by the gate oxide capacitance.
- Ideally, turn-on, turn-off and propagation delay times are zero, as shown in the ideal transient response of the inverter below.





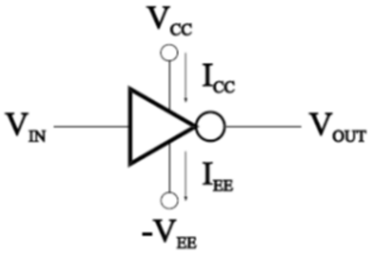
- The figure above shows an input pulse and output response of an inverter. Here, t_d is the delay time, t_r is the rise time, t_s is the storage time, t_f is the fall time, $t_{ON} = t_d + t_r$ is the turn-on time and $t_{OFF} = t_s + t_f$ is the turn-off time.
- The $10\% \, V_{OH}$ and $90\% \, V_{OH}$ points are marked on both the rising and falling edges of the output voltage. The rise time t_r and fall time t_f are the times associates with charging and discharging load capacitances.
- The delay time t_d and storage time t_s are associated with the storage charge of PN junctions.



- The figure above shows an input waveform and output response of an inverter. Here, t_{PLH} is the low-to-high propagation delay time and t_{PHL} is the high-to-low propagation delay time.
- The 50% points are labelled on the rising and falling edges of both the input and output waveforms.
- The overall propagation delay time $t_{p(avg)}$ is defined as the average of t_{PLH} and t_{PHL}, i.e.,

$$t_{p(avg)} = \frac{t_{PLH} + t_{PHL}}{2}.$$

Average Power Dissipation



$P_{CC} = I_{CC}V_{CC}$

$P_{EE} = I_{EE}V_{EE}$

A logic circuit with two power supplies is shown in the figure above. As the power dissipated in this gate for the output high and output low states are different, the **average power dissipation** $P_{D(avg)}$ for this gate with two possible states are given as

$$\begin{aligned} P_{D(avg)} &= P_{CC(avg)} + P_{EE(avg)} \\ &= \frac{P_{CC(OH)} + P_{CC(OL)}}{2} + \frac{P_{EE(OH)} + P_{EE(OL)}}{2} \\ &= \frac{I_{CC(OH)} + I_{CC(OL)}}{2} V_{CC} + \frac{I_{EE(OH)} + I_{EE(OL)}}{2} V_{EE} \end{aligned}$$

- As we will see later, static power dissipation will be zero in CMOS circuits. Hence, we have to consider the dynamic power dissipation as given below

$$P_{D(dynamic)} = C_L f\, V_{LS}^2.$$

where C_L is the load capacitance, f is the frequency of switching and V_{LS} is the voltage swing over the load. In CMOS circuits operate rail-to-rail, so $V_{LS} = V_{DD}$, where V_{DD} is value of the DC power supply.

Power-Delay Product

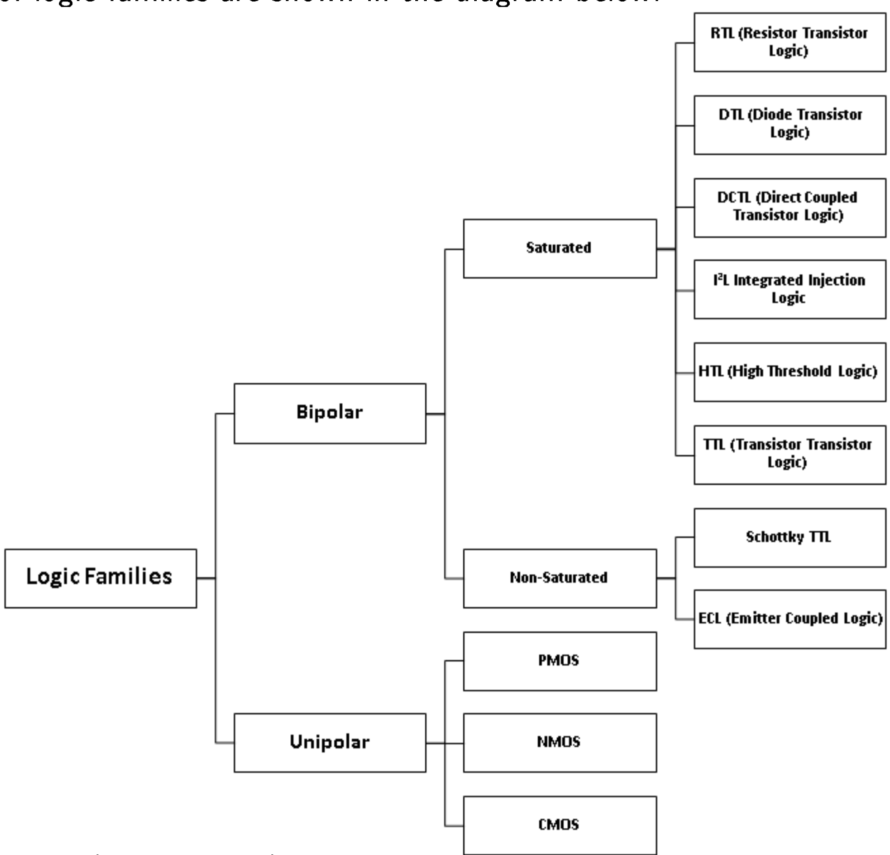
- Low power dissipation and short propagation delay times are both desirable for digital logic circuits. However, faster propagation times are achieved at the cost of increased power dissipation. Conversely, lower power dissipation results in longer propagation delays
- A practical figure of merit used for digital logic gates is the **power-delay product** or speed-power product given by

$$PD = P_{D(avg)} \times t_{p(avg)}$$

- The unit of power-delay product is in terms of joules and the lower the value of the power-delay product the better.
- For a logic family, this power-delay product can be considered as constant. In other words, if you want to decrease power dissipation by increasing resistor values, the propagation delay will increase accordingly. You can change the power-delay product by redesigning the whole digital circuit (using different design and/or different components).

Logic Families

A summary of logic families are shown in the diagram below.



All logic families have different properties. For example, CMOS logic circuits have very low power dissipations.

For another example, propagation delay and power dissipation characteristics for TTL and STTL families are given in the table below.

Family	**Power**	**Prop. Delay**
TTL	10 mW	9 ns
STTL	20 mW	3 ns
LSTTL	2 mW	9 ns
ASTTL	10 mW	2 ns
ALSTTL	1 mW	4 ns
FAST	4 mW	2 ns