ELE 315 Electronics II

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1. These lecture notes are not complete and regularly updated at the address below: http://www.ee.hacettepe.edu.tr/∼usezen/ele315/.

2. These lecture notes use material from several other sources like Prof. Selçuk Geçim's lecture notes, "Electronic Devices and Circuit Theory, 8th ed." by Boylestad and Nashelsky and and its instructor materials, "Integrated Electronics: Analog and Digital Circuits and Systems" by Millman and Halkias, and "Digital Integrated Circuits" by DeMassa and Ciccone.

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Chapter 1

Analogue Electronics

1.1 Feedback and Feedback Amplifiers

Before continuing further, we are going to classify the amplifiers according to their input and output signals. Determining the amplifier type is very important for feedback design and analysis.

1.1.1 Amplifier Models

Let us first classify the amplifier models according to their input and output signal types.

1. Voltage-Gain Amplifier
    - voltage input (i.e., voltage source at input)
    - voltage output (i.e., voltage-controlled voltage source at output)
2. Transresistance Amplifier
    - current input (i.e., current source at input)
    - voltage output (i.e., current-controlled voltage source at output)
3. Transconductance Amplifier
    - voltage input (i.e., voltage source at input)
    - current output (i.e., voltage-controlled current source at output)
4. Current-Gain Amplifier
    - current input (i.e., current source at input)
    - current output (i.e., current-controlled current source at output)

1.1.1.1 Voltage-Gain Amplifier

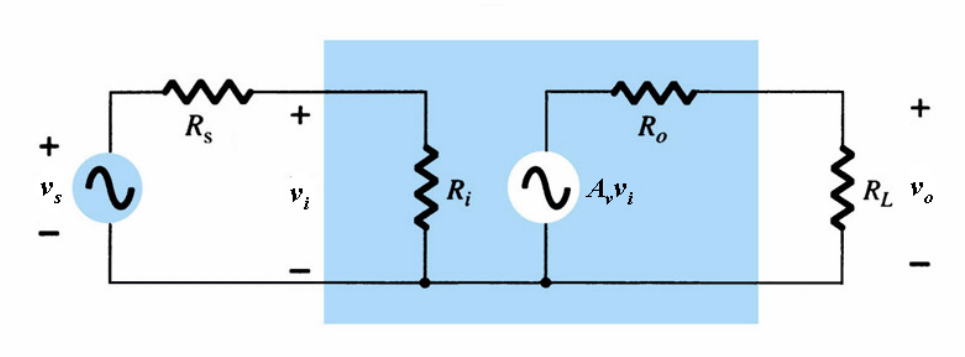


Figure 1.1.1: Voltage-gain amplifier

Here, v_s and R_s are the voltage source and internal resistance of the voltage source; R_i, A_v and R_o are the input resistance, no-load gain and output resistance of the amplifier; and R_L is the load resistance.

- As, no-load voltage gain, A_v is defined as

$$\boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty}} \tag{1.1.1}$$

- Voltage gain with load, A_V will be given as

$$\boxed{A_V = \frac{v_o}{v_i} = A_v \frac{R_L}{R_o + R_L}} \tag{1.1.2}$$

- No-load overall voltage gain, A_{vs} will be given as

$$\boxed{A_{vs} = \left.\frac{v_o}{v_s}\right|_{R_L=\infty} = \frac{R_i}{R_s + R_i} A_v} \tag{1.1.3}$$

- Overall voltage gain, A_{Vs} will be given as

$$\boxed{A_{Vs} = \frac{v_o}{v_s} = \frac{R_i}{R_s + R_i} A_v \frac{R_L}{R_o + R_L}} \tag{1.1.4}$$

- Ideally we want overall voltage gain A_{Vs} should be equal to the no-load voltage gain A_v. Thus, ideal input resistance R_i and ideal output resistance R_o of a voltage-gain amplifier should be infinity and zero, respectively.

$$\boxed{A_{Vs} \to A_v \quad \Rightarrow \quad \begin{cases} R_i \to \infty \\ R_o \to 0 \end{cases}}$$

- Thus, for a good voltage-gain amplifier R_i should be **large** (i.e., $R_i \gg R_s$) and R_o should be **small** (i.e., $R_o \ll R_L$).

1.1.1.2 Transresistance Amplifier

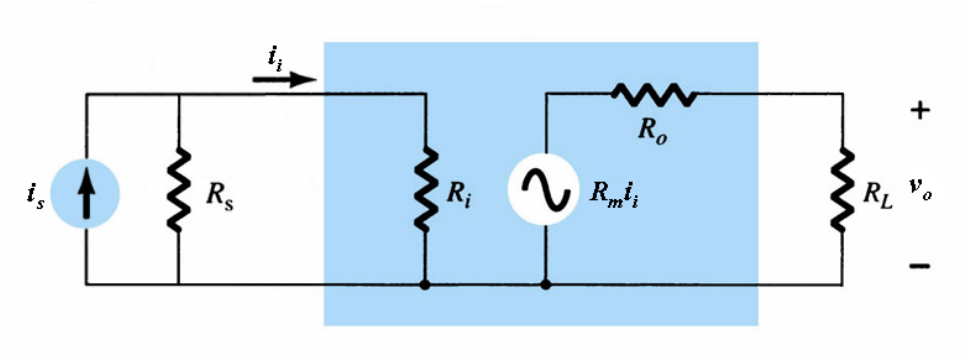


Figure 1.1.2: Transresistance amplifier

Here, i_s and R_s are the current source and internal resistance of the current source; R_i, R_m and R_o are the input resistance, no-load gain and output resistance of the amplifier; and R_L is the load resistance.

- As, no-load transresistance gain, R_m is defined as

$$\boxed{R_m = \left.\frac{v_o}{i_i}\right|_{R_L=\infty}} \tag{1.1.5}$$

- Transresistance gain with load, R_M will be given as

$$\boxed{R_M = \frac{v_o}{i_i} = R_m \frac{R_L}{R_o + R_L}} \tag{1.1.6}$$

- No-load overall gain, R_{ms} will be given as

$$\boxed{R_{ms} = \left.\frac{v_o}{i_s}\right|_{R_L=\infty} = \frac{R_s}{R_s + R_i} R_m} \tag{1.1.7}$$

- Overall transresistance gain, R_{Ms} will be given as

$$\boxed{R_{Ms} = \frac{v_o}{i_s} = \frac{R_s}{R_s + R_i} R_m \frac{R_L}{R_o + R_L}} \tag{1.1.8}$$

- Ideally we want overall transresistance gain R_{Ms} should be equal to the no-load transresistance gain R_m. Thus, ideal input resistance R_i and ideal output resistance R_o of a transresistance amplifier should be both zero.

$$\boxed{R_{Ms} \to R_m \quad \Rightarrow \quad \begin{cases} R_i \to 0 \\ R_o \to 0 \end{cases}}$$

- Thus, for a good transresistance amplifier R_i should be **small** (i.e., $R_i \ll R_s$) and R_o should be **small** also (i.e., $R_o \ll R_L$).

1.1.1.3 Transconductance Amplifier

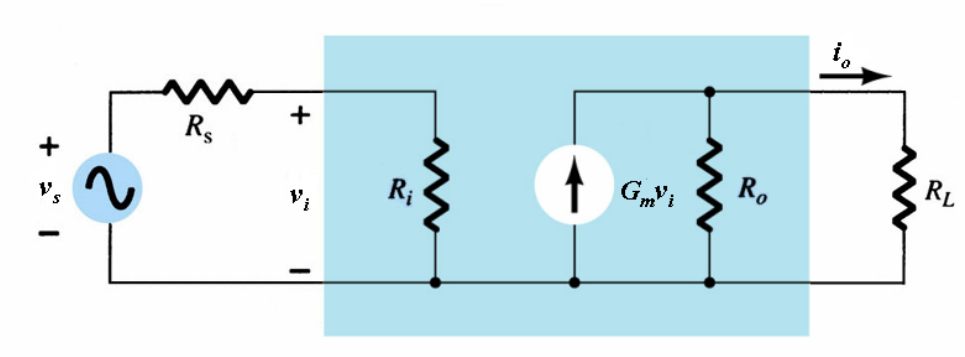


Figure 1.1.3: Transconductance amplifier

Here, v_s and R_s are the voltage source and internal resistance of the voltage source; R_i, G_m and R_o are the input resistance, no-load gain and output resistance of the amplifier; and R_L is the load resistance.

- As, no-load transconductance gain, G_m is defined as

$$\boxed{G_m = \left.\frac{i_o}{v_i}\right|_{R_L=0}} \tag{1.1.9}$$

- Transconductance gain with load, G_M will be given as

$$\boxed{G_M = \frac{i_o}{v_i} = G_m \frac{R_o}{R_o + R_L}} \tag{1.1.10}$$

- No-load overall transconductance gain, G_{ms} will be given as

$$\boxed{G_{ms} = \left.\frac{i_o}{v_s}\right|_{R_L=0} = \frac{R_i}{R_s + R_i} G_m} \tag{1.1.11}$$

- Overall transconductance gain, G_{Ms} will be given as

$$\boxed{G_{Ms} = \frac{i_o}{v_s} = \frac{R_i}{R_s + R_i} G_m \frac{R_o}{R_o + R_L}} \tag{1.1.12}$$

- Ideally we want overall transconductance gain G_{Ms} should be equal to the no-load transconductance gain G_m. Thus, ideal input resistance R_i and ideal output resistance R_o of a transconductance amplifier should be both infinity.

$$\boxed{G_{Ms} \to G_m \quad \Rightarrow \quad \begin{cases} R_i \to \infty \\ R_o \to \infty \end{cases}}$$

- Thus, for a good transconductance amplifier R_i should be **large** (i.e., $R_i \gg R_s$) and R_o should be **large** also (i.e., $R_o \gg R_L$).

1.1.1.4 Current-Gain Amplifier

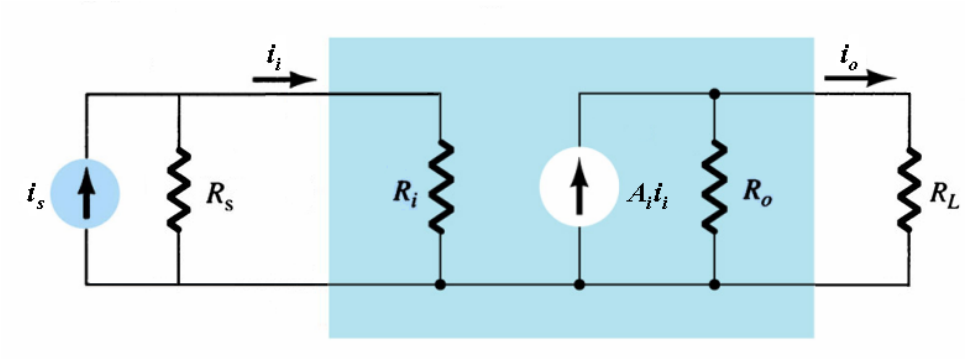


Figure 1.1.4: Current-gain amplifier

Here, i_s and R_s are the current source and internal resistance of the current source; R_i, A_i and R_o are the input resistance, no-load gain and output resistance of the amplifier; and R_L is the load resistance.

- As, no-load current gain, A_i is defined as

$$\boxed{A_i = \left.\frac{i_o}{i_i}\right|_{R_L=0}} \tag{1.1.13}$$

- Current gain with load, A_I will be given as

$$\boxed{A_I = \frac{i_o}{i_i} = A_i \frac{R_o}{R_o + R_L}} \tag{1.1.14}$$

- No-load overall current gain, A_{is} will be given as

$$\boxed{A_{is} = \left.\frac{i_o}{i_s}\right|_{R_L=0} = \frac{R_s}{R_s + R_i} A_i} \tag{1.1.15}$$

- Overall current gain, A_{Is} will be given as

$$\boxed{A_{Is} = \frac{i_o}{i_s} = \frac{R_s}{R_s + R_i} A_i \frac{R_o}{R_o + R_L}} \tag{1.1.16}$$

- Ideally we want overall current gain A_{Is} should be equal to the no-load current gain A_i. Thus, ideal input resistance R_i and ideal output resistance R_o of a current-gain amplifier should be zero and infinity, respectively.

$$\boxed{A_{Is} \to A_i \quad \Rightarrow \quad \begin{cases} R_i \to 0 \\ R_o \to \infty \end{cases}}$$

- Thus, for a good current-gain amplifier R_i should be **small** (i.e., $R_i \ll R_s$) and R_o should be **large** (i.e., $R_o \gg R_L$).

1.1.2 Negative Feedback Concepts

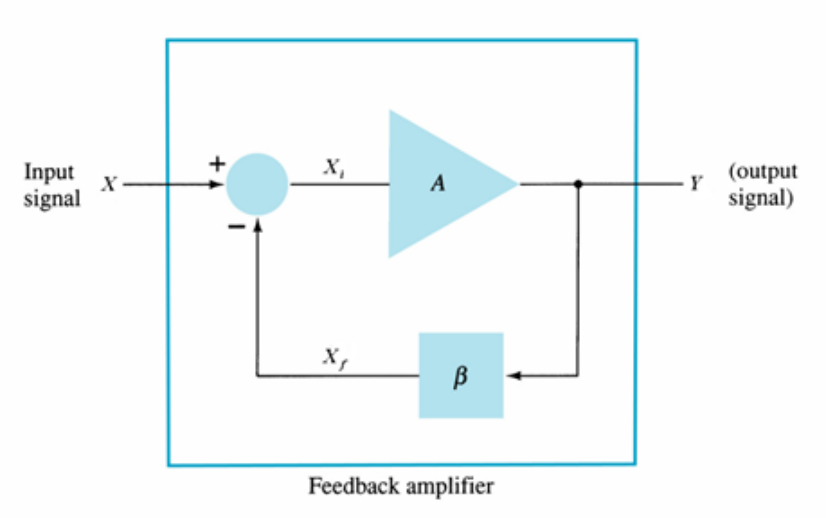


Figure 1.1.5: Negative feedback block diagram

This block diagram is called **negative feedback**, because the feedback signal X_f subtracted from the input signal X as seen in the figure above. Here, A is the open-loop gain (i.e., gain without feedback), X, Y and X_f represents the input, output and feedback signals respectively, and X_i is the feedback reduced input signal.

The effects of the negative feedback on an amplifier can be summarized as follows.

Disadvantages:

- Lower gain

Advantages:

- More stable gain
- Reduced distortion
- Improved frequency response
- Improved input impedance
- Improved output impedance
- More linear operation

1.1.2.1 Closed-loop Gain, A_f

From the Figure 1.1.5 we can calculate the **closed-loop gain** (i.e., gain with feedback), $A_f = \dfrac{Y}{X}$ as follows

$$Y = AX_i \tag{1.1.17}$$
$$X_f = \beta Y \tag{1.1.18}$$
$$X_i = X - X_f \tag{1.1.19}$$

From the three equations above, we can on obtain the gain with feedback A_f as follows

$$\boxed{A_f = \frac{Y}{X} = \frac{A}{1+\beta A}} \tag{1.1.20}$$

If $\beta A \gg 1$ then, above equation reduces to

$$\boxed{A_f \approx \frac{1}{\beta}.} \tag{1.1.21}$$

So, in order to have $A_f > 1$, $\beta < 1$ is required.

1.1.2.2 Negative Feedback Improvements

We are going to investigate and prove the following three improvements of the negative feedback

1. Improved Gain Stability
2. Reduced Distortion
3. Increased Bandwidth

Improved Gain Stability

We need to find the closed-loop gain stability (relative change of the gain), i.e., the ratio $\frac{\Delta A_f}{A_f}$. In order to derive this quantity, we need to first find the derivative $\frac{dA_f}{dA}$.

$$\frac{dA_f}{dA} = \frac{d\left(\frac{A}{1+\beta A}\right)}{dA} \tag{1.1.22}$$

$$= \frac{1}{(1+\beta A)^2} \qquad \ldots \text{using the chain rule of derivatives} \tag{1.1.23}$$

$$= \frac{A}{1+\beta A}\frac{1}{A(1+\beta A)} \qquad \ldots \text{multiplying the numerator and denominator by } A \tag{1.1.24}$$

$$= \frac{A_f}{A}\frac{1}{1+\beta A} \tag{1.1.25}$$

From the result above, we can obtain the following expression for the closed-loop gain stability in terms of the open-loop gain stability

$$\boxed{\frac{dA_f}{A_f} = \frac{1}{1+\beta A}\frac{dA}{A}} \tag{1.1.26}$$

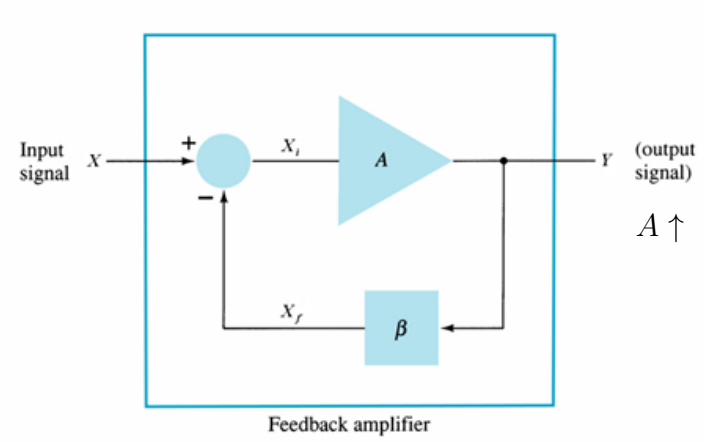
Thus, the closed-loop gain stability is improved by a factor of $(1+\beta A)$ compared to the open-loop gain stability.

Example 1.1: Assume a system where open-loop gain equals $A = 1000$ and changes by 20% due to a temperature change. Consider a negative feedback closed-loop system with $\beta = 0.1$ and calculate the change for the closed-loop gain A_f for the same conditions.

Solution: We can find $\dfrac{\Delta A_f}{A_f}$ from the equation derived previously. Thus,

$$\begin{aligned}\frac{\Delta A_f}{A_f} &= \frac{1}{1+\beta A}\frac{\Delta A}{A} \\ &= \frac{1}{1+0.1\times 1000}\,20\% \\ &= 0.2\%.\end{aligned}$$

Thus, the closed-loop gain (although smaller) is much more stable than the open-loop gain.



$$A\uparrow \;\Rightarrow\; Y\uparrow \;\Rightarrow\; X_f\uparrow \;\Rightarrow\; X_i\downarrow \;\Rightarrow\; Y\downarrow$$

Above figure explains the reason for the stability improvement. If open-loop gain A increases, then output Y increases. If output Y increases, then feedback signal X_f increases. If feedback signal X_f increases, then internal input signal X_i decreases. If internal input signal X_i decreases the eventually the output signal Y decreases. Hence, this process provides stability.

Reduced Distortion

Here we are going to assume that we have some additive distortion D in the open-loop system, i.e.,

$$Y = AX + D \tag{1.1.27}$$

We need to investigate the same problem when we employ a negative feedback for this system. Let us start with writing the closed-loop equations from the Figure 1.1.5

$$Y = AX_i + D \tag{1.1.28}$$

$$X_f = \beta Y \tag{1.1.29}$$

$$X_i = X - X_f \tag{1.1.30}$$

From the three equations above, we can on obtain the output Y as follows

$$\boxed{Y = \frac{A}{1+\beta A}X + \frac{D}{1+\beta A}} \tag{1.1.31}$$

Thus, distortion in the closed-loop system is reduced by a factor of $(1 + \beta A)$.

Increased Bandwidth

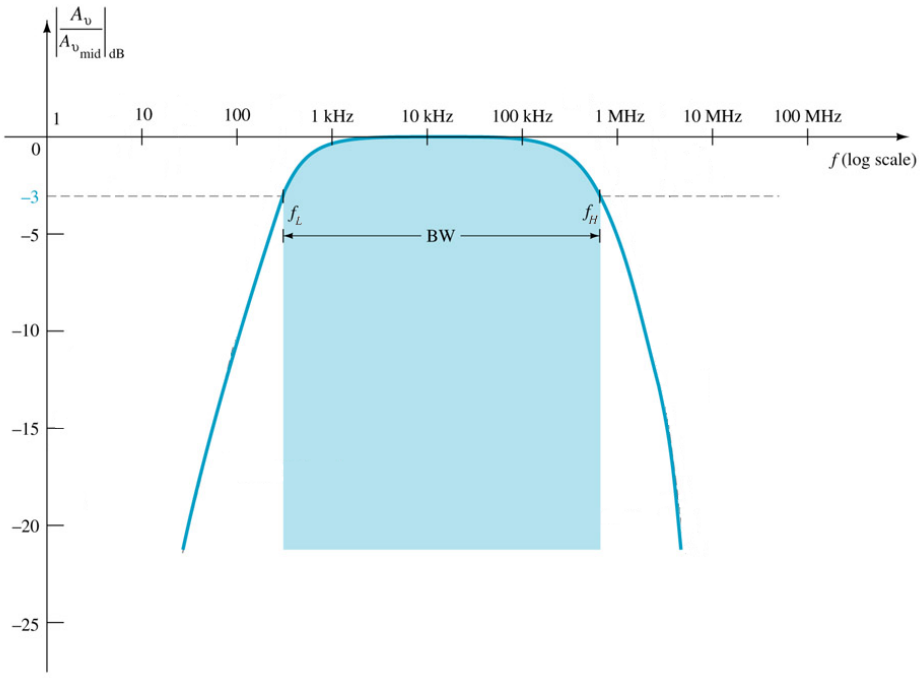


Figure 1.1.6: Amplifier bandwidth example

Bandwidth BW is the difference between the higher cut-off frequency f_H and the lower cut-off frequency f_L of the amplifier, i.e.,

$$BW = f_H - f_L. \tag{1.1.32}$$

So, if f_H gets higher and/or f_L gets lower, then the bandwidth increases.

We can consider both ends of the amplitude response in Figure 1.1.6 separately (as $f_H \gg f_L$). The lower end of the amplitude response is a high-pass filter, and the higher end of the amplitude response is a low-pass filter.

Let us first consider the lower-end high-pass system like a simple RC-filter and write down the open-loop frequency response $A_H(f)$ accordingly (f is the frequency of the input signal)

$$A_H(f) = \frac{A_m}{1 - j\frac{f_L}{f}} \tag{1.1.33}$$

where A_m and f_L are the midband gain and lower cut-off frequency of the open-loop system, respectively. We know that the closed-loop gain $A_{Hf}(f)$ is given by

$$A_{Hf}(f) = \frac{A_H(f)}{1 + \beta A_H(f)}. \tag{1.1.34}$$

By inserting $A_H(f)$ into the equation and rearranging it, we arrive at

$$A_{Hf}(f) = \frac{A_{mf}}{1 - j\frac{f_{Lf}}{f}} \tag{1.1.35}$$

where A_{mf} and f_{Lf} are the midband gain and lower cut-off frequency of the closed-loop system, and given by

$$\boxed{A_{mf} = \frac{A_m}{1 + \beta A_m}} \tag{1.1.36}$$

and

$$\boxed{f_{Lf} = \frac{f_L}{1 + \beta A_m}} \tag{1.1.37}$$

respectively. Thus, low-frequency f_{Lf} of the closed-loop system is reduced by a factor of $(1 + \beta A_m)$.

Let us now consider the upper-end low-pass system like a simple RC-filter and write down the open-loop frequency response $A_L(f)$ accordingly (f is the frequency of the input signal)

$$A_L(f) = \frac{A_m}{1 + j\dfrac{f}{f_H}} \tag{1.1.38}$$

where A_m and f_H are the midband gain and higher cut-off frequency of the open-loop system, respectively. We know that the closed-loop gain $A_{Lf}(f)$ is given by

$$A_{Lf}(f) = \frac{A_L(f)}{1 + \beta A_L(f)}. \tag{1.1.39}$$

Similarly, by inserting $A_L(f)$ into the equation and rearranging it, we arrive at

$$A_{Lf}(f) = \frac{A_{mf}}{1 + j\dfrac{f}{f_{Hf}}} \tag{1.1.40}$$

where A_{mf} and f_{Hf} are the midband gain and higher cut-off frequency of the closed-loop system, and given by

$$\boxed{A_{mf} = \frac{A_m}{1 + \beta A_m}} \tag{1.1.41}$$

and

$$\boxed{f_{Hf} = (1 + \beta A_m)\, f_H} \tag{1.1.42}$$

respectively. Thus, high-frequency f_{Hf} of the closed-loop system is increased by a factor of $(1 + \beta A_m)$. Consequently, we have showed that negative feedback increases the bandwidth.

NOTE: The **gain-bandwidth product** stays (nearly) **constant**

$$A_f \times BW_f \cong A \times BW = \text{constant} \tag{1.1.43}$$

as $BW_f \approx f_{Hf}$ and $BW \approx f_H$.

1.1.2.3 Sampling and Mixing

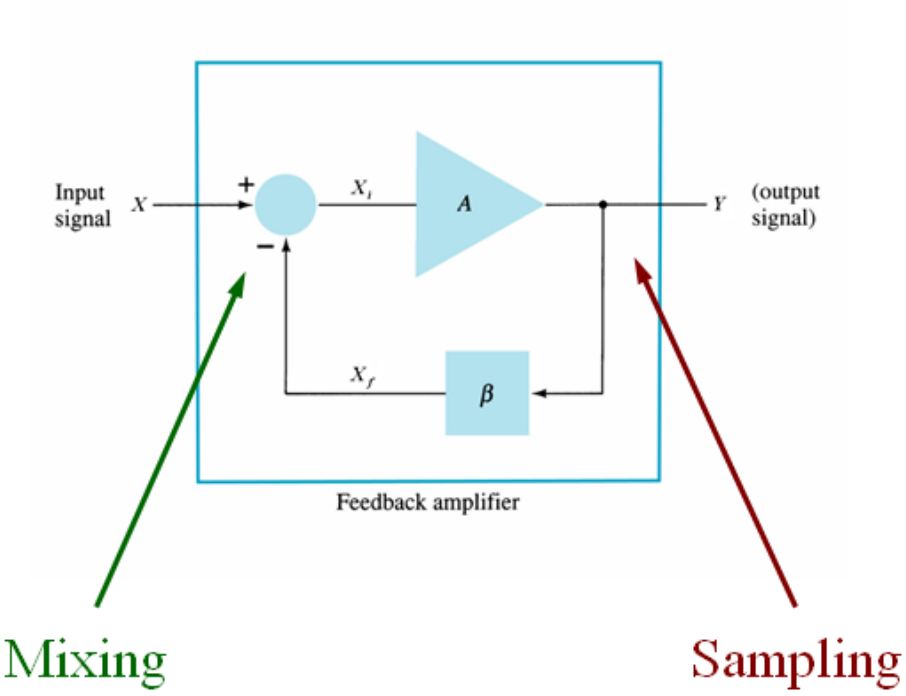


Figure 1.1.7: Sampling and mixing diagram in a negative feedback system

The output signal is **sampled** and fed back to the system and **mixed** with the input signal. Here, we are going to analyze the possible sampling and mixing types.

1.1.2.4 Sampling Types

As there two types of electrical signals, i.e., voltage and current, there are two types of sampling. In order to sample **output voltage** we need to connect the feedback network in parallel (i.e., shunt connection) with the output (like a voltmeter). Similarly, in order to sample **output current** we need to connect the feedback network in series with the output (like an ammeter).

1. **Voltage-sampling** (Shunt-sampling or parallel-sampling)
2. **Current-sampling** (Series-sampling)

Voltage-Sampling Example

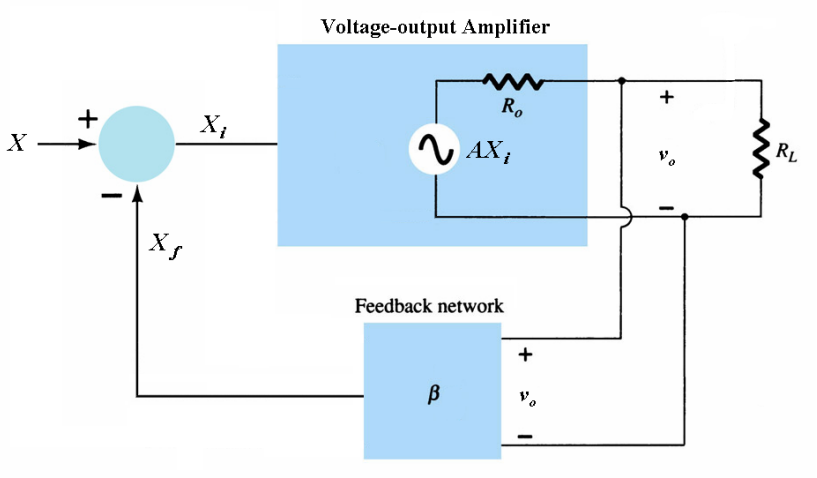


Figure 1.1.8: Voltage-sampling example

Current-Sampling Example

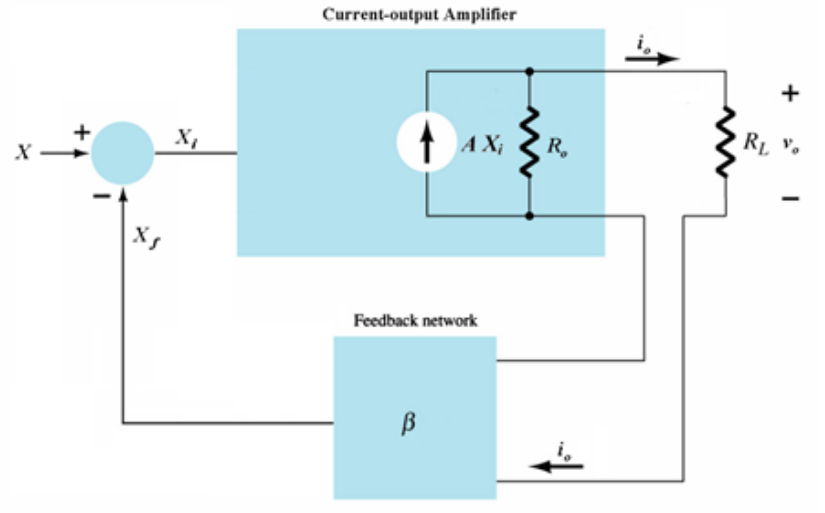


Figure 1.1.9: Current-sampling example

1.1.2.5 Mixing Types

We can mix (i.e., connect) the feedback network output to the input in parallel or in series. In order to mix voltage feedback signal we need to connect the feedback network in **series** to the input (remember KVL). Similarly, in order to mix current feedback signal we need to connect the feedback network in parallel (i.e., **shunt** connection) to the input (remember KCL).

1. **Series-mixing** (voltage-mixing)
2. **Shunt-mixing** (parallel-mixing or current-mixing)

Series-Mixing Example

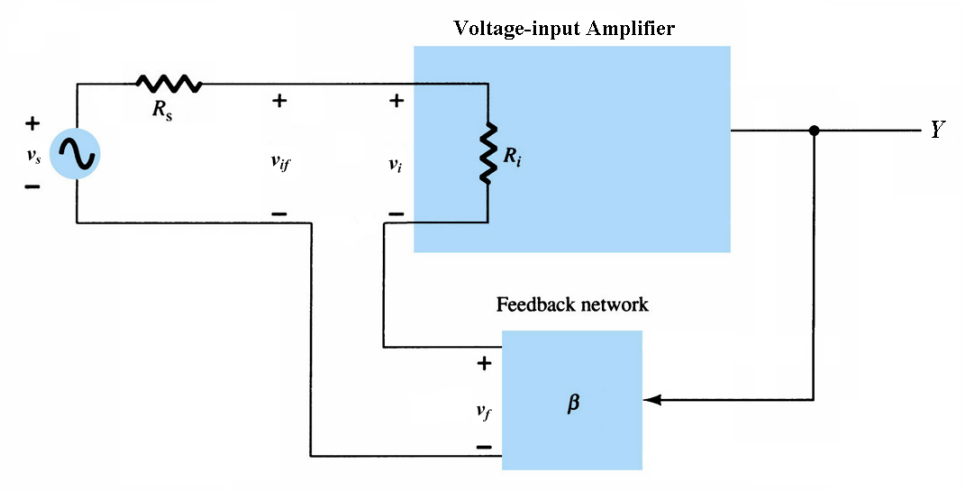


Figure 1.1.10: Series-mixing example

Shunt-Mixing Example

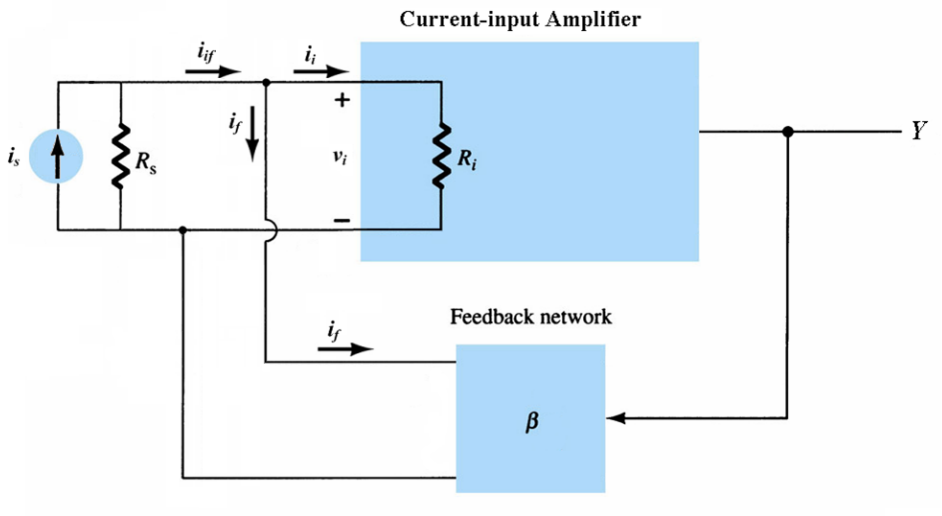


Figure 1.1.11: Shunt-mixing example

1.1.2.6 Negative Feedback Types

Negative feedback types are classified according to the **Sampling-Mixing** type pairs. As there are two types of sampling and two types mixing, there four types feedback types.

1. **Voltage-Series Feedback**
2. **Voltage-Shunt Feedback** (voltage-parallel feedback)
3. **Current-Series Feedback**
4. **Current-Shunt Feedback** (current-parallel feedback)

1.1.3 Voltage-Series Feedback

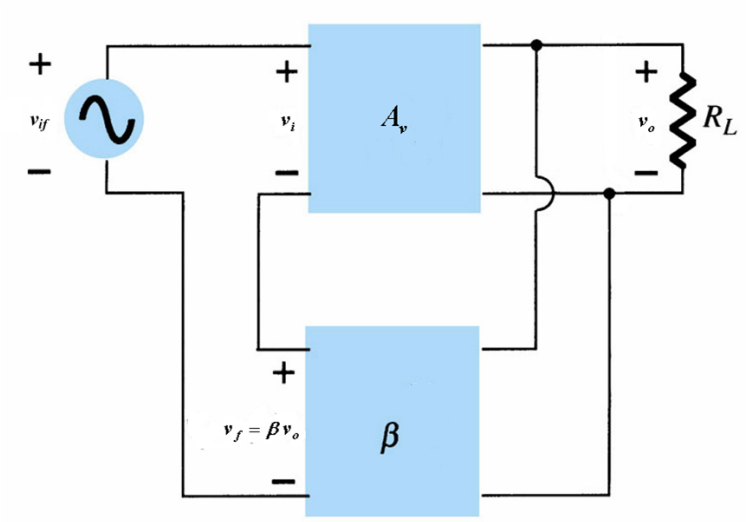


Figure 1.1.12: Voltage-series feedback: Block diagram

Voltage-series feedback amplifier is actually a closed-loop voltage-gain amplifier as shown below. We are going to find the derive the no-load gain A_{vf}, input resistance R_{if} and output resistance R_{of} of this closed-loop system.

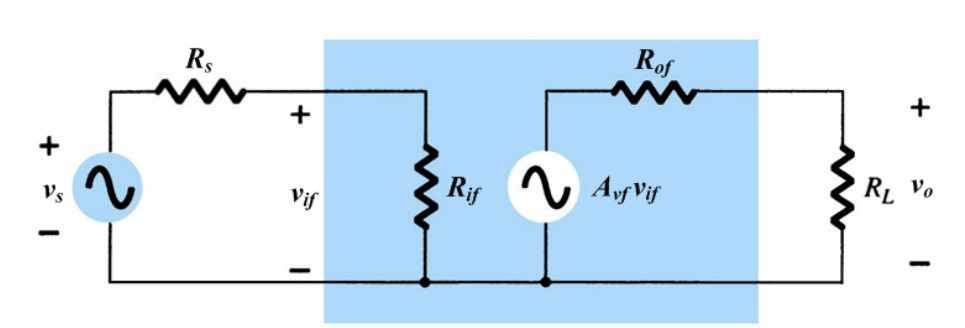


Figure 1.1.13: Voltage-series feedback amplifier model (i.e., closed-loop voltage-gain amplifier)

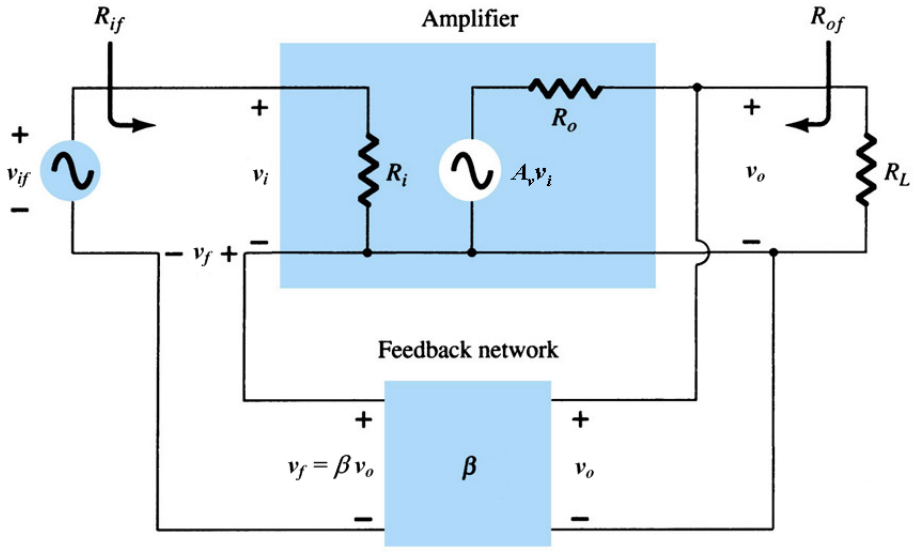


Figure 1.1.14: Voltage-series feedback: Block diagram with open-loop amplifier parameters

Let us derive no-load gain A_{vf}, input resistance R_{if} and output resistance R_{of} of the voltage-series feedback system in terms of the open-loop amplifier parameters A_v, R_i and R_o.

$\boxed{A_{vf} = ?}$ $\boxed{R_{if} = ?}$ $\boxed{R_{of} = ?}$

1.1.3.1 No-load Gain

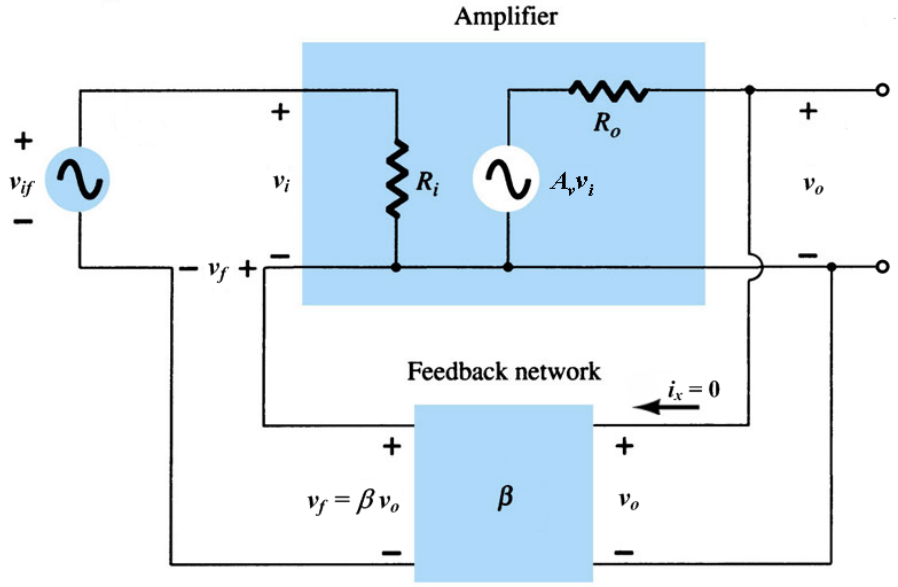


Figure 1.1.15: Voltage-series feedback: No-load gain calculation diagram

From the above figure, we can quickly derive the closed-loop no-load gain A_{vf} where

$$A_{vf} = \left.\frac{v_o}{v_{if}}\right|_{R_L=\infty} = \frac{v_o}{v_i + v_f} = \frac{A_v v_i}{(1 + \beta A_v) v_i}$$

as

$$\boxed{A_{vf} = \frac{A_v}{1 + \beta A_v}} \tag{1.1.44}$$

1.1.3.2 Input Resistance

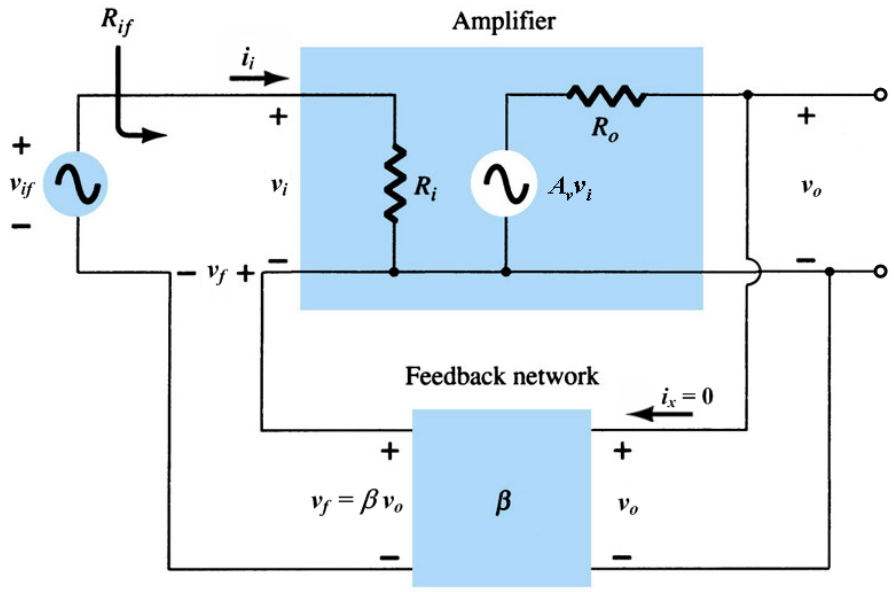


Figure 1.1.16: Voltage-series feedback: Input resistance calculation diagram

From the above figure, we can quickly derive the closed-loop input resistance R_{if}

$$R_{if} = \left.\frac{v_{if}}{i_i}\right|_{R_L=\infty} = \frac{v_i + v_f}{i_i} = \frac{(1 + \beta A_v) v_i}{i_i} = (1 + \beta A_v)\frac{v_i}{i_i}$$

as

$$\boxed{R_{if} = (1 + \beta A_v) R_i} \tag{1.1.45}$$

Loading Effect of Negative Feedback

- If a load R_L is connected, then the gain will drop due to the voltage divider configuration between R_o and R_L. Hence, closed-loop input resistance will be affected due to the feedback.

  Consequently, closed-loop input resistance R_{if} will be given by

$$\boxed{R_{if} = (1 + \beta A_V) R_i} \tag{1.1.46}$$

  where

$$\boxed{A_V = A_v \frac{R_L}{R_L + R_o}} \tag{1.1.47}$$

1.1.3.3 Output Resistance

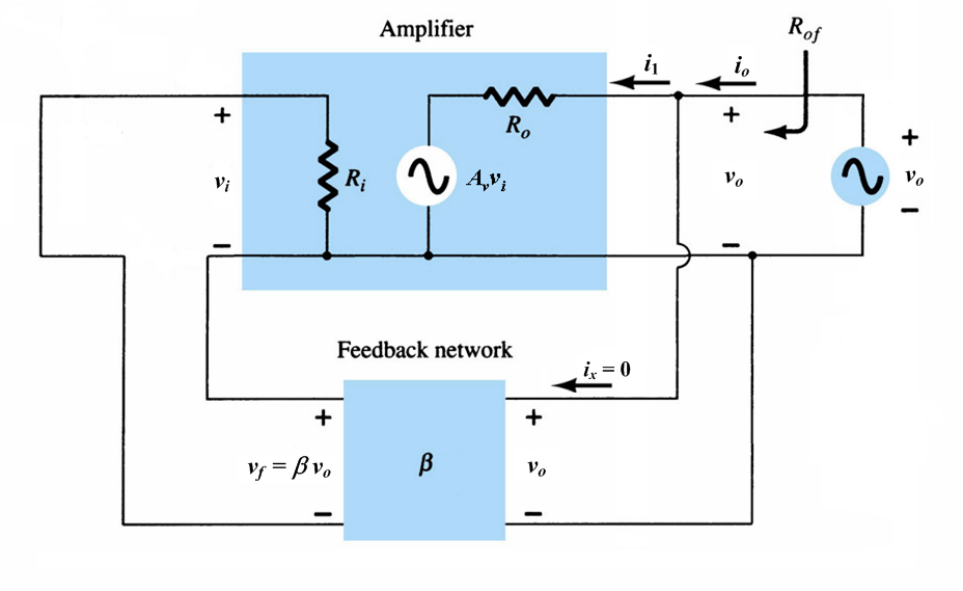


Figure 1.1.17: Voltage-series feedback: Output resistance calculation diagram

We can calculate the closed-loop output resistance (i.e., as a Thévenin equivalent resistance) by using the test voltage method as shown in the figure above. Note that as the feedback network is ideal, internal resistance of the feedback network is infinity. So, $i_x = 0$ and $i_o = i_1 + i_x = i_1$. Also as $v_{if} = 0$, $v_i = -v_f = -\beta v_o$. Hence, output resistance R_{of}

$$R_{of} = \left.\frac{v_o}{i_o}\right|_{R_L=v_o, v_{if}=0} = \frac{v_o}{i_1} = \frac{v_o}{\frac{v_o - A_v v_i}{R_o}} = \frac{R_o v_o}{v_o - A_v(-\beta v_o)} = \frac{R_o v_o}{(1+\beta A_v)v_o}$$

is derived as

$$\boxed{R_{of} = \frac{R_o}{1+\beta A_v}} \tag{1.1.48}$$

Effect of Source Resistance under Negative Feedback

- If a voltage source v_s with an internal resistance R_s is connected at the input, then the gain will drop due to the voltage divider configuration between R_i and R_s. Hence, closed-loop output resistance will be affected due to the feedback.

  Consequently, closed-loop output resistance R_{of} will be given by

$$\boxed{R_{of} = \frac{R_o}{1+\beta A_{vs}}} \tag{1.1.49}$$

  where

$$\boxed{A_{vs} = \frac{R_i}{R_s + R_i} A_v} \tag{1.1.50}$$

1.1.4 Voltage-Shunt Feedback

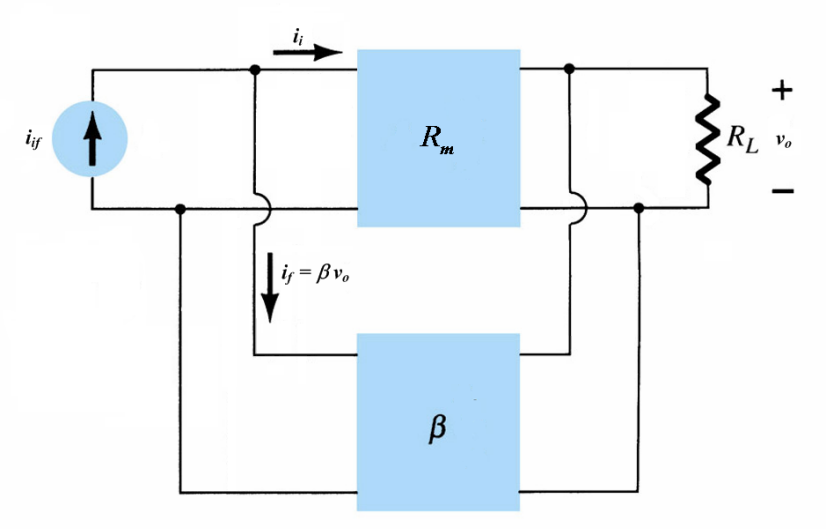


Figure 1.1.18: Voltage-shunt feedback: Block diagram

Voltage-shunt feedback amplifier is actually a closed-loop transresistance amplifier as shown below. We are going to find the derive the no-load gain R_{mf}, input resistance R_{if} and output resistance R_{of} of this closed-loop system.

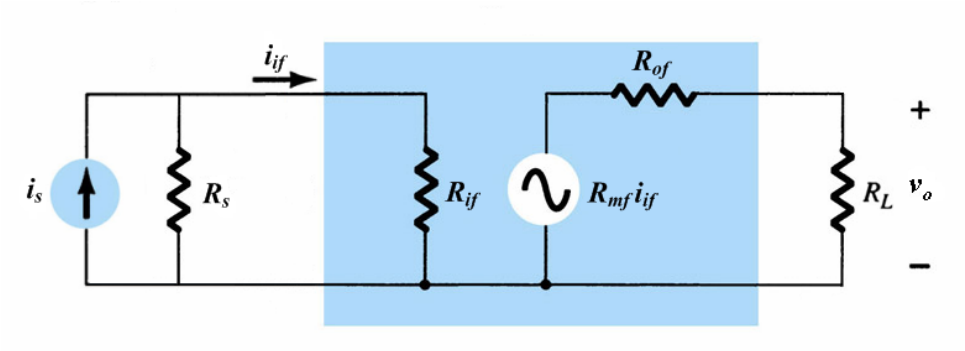


Figure 1.1.19: Voltage-shunt feedback amplifier model (i.e., closed-loop transresistance amplifier)

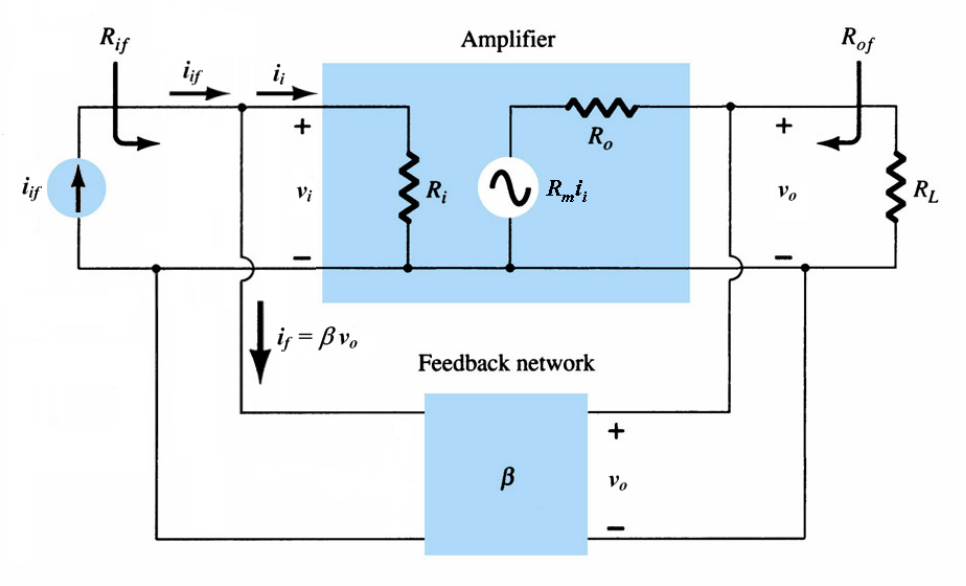


Figure 1.1.20: Voltage-shunt feedback: Block diagram with open-loop amplifier parameters

Let us derive no-load gain R_{mf}, input resistance R_{if} and output resistance R_{of} of the voltage-shunt feedback system in terms of the open-loop amplifier parameters R_m, R_i and R_o.

$\boxed{R_{mf} = ?}$ $\boxed{R_{if} = ?}$ $\boxed{R_{of} = ?}$

1.1.4.1 No-load Gain

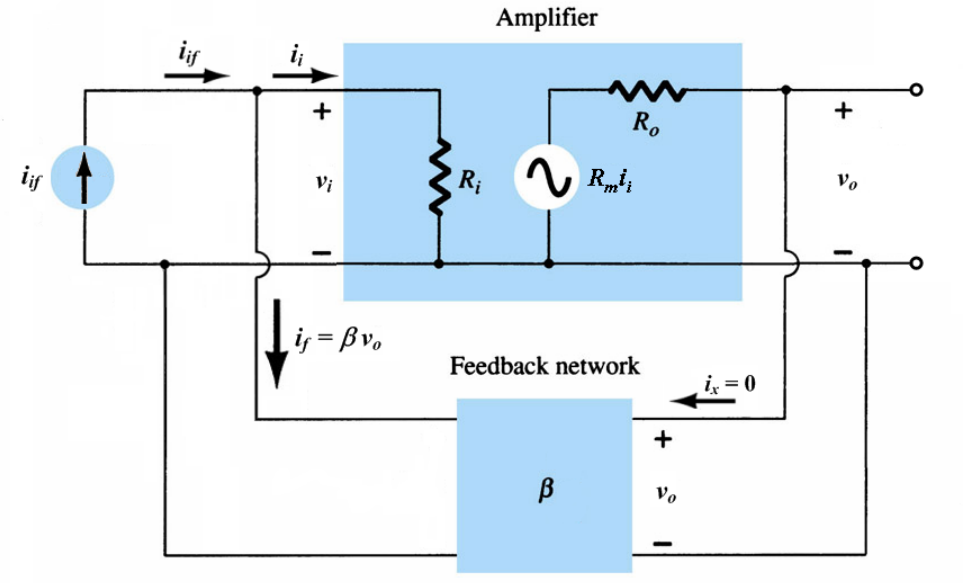


Figure 1.1.21: Voltage-shunt feedback: No-load gain calculation diagram

From the above figure, we can quickly derive the closed-loop no-load gain R_{mf} where

$$R_{mf} = \left.\frac{v_o}{i_{if}}\right|_{R_L=\infty} = \frac{v_o}{i_i + i_f} = \frac{R_m i_i}{(1+\beta R_m) i_i}$$

as

$$\boxed{R_{mf} = \frac{R_m}{1 + \beta R_m}} \tag{1.1.51}$$

1.1.4.2 Input Resistance

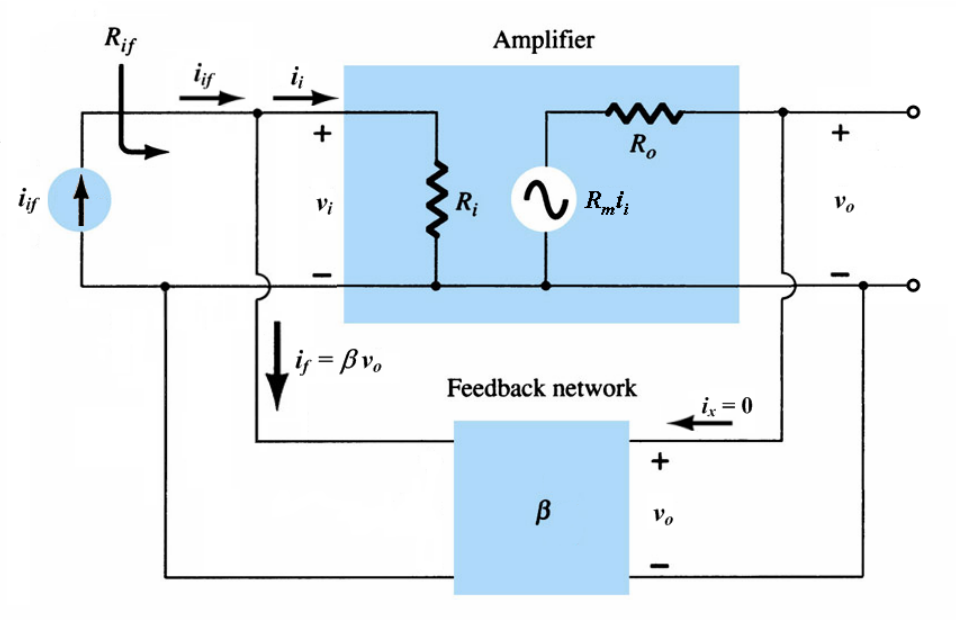


Figure 1.1.22: Voltage-shunt feedback: Input resistance calculation diagram

From the above figure, we can quickly derive the closed-loop input resistance R_{if}

$$R_{if} = \left.\frac{v_i}{i_{if}}\right|_{R_L=\infty} = \frac{v_i}{i_i + i_f} = \frac{v_i}{(1 + \beta R_m) i_i}$$

as

$$\boxed{R_{if} = \frac{R_i}{1 + \beta R_m}} \tag{1.1.52}$$

Loading Effect of Negative Feedback

- If a load R_L is connected, then the gain will drop due to the voltage divider configuration between R_o and R_L. Hence, closed-loop input resistance will be affected due to the feedback.

  Consequently, closed-loop input resistance R_{if} will be given by

$$\boxed{R_{if} = \frac{R_i}{1 + \beta R_M}} \tag{1.1.53}$$

  where

$$\boxed{R_M = R_m \frac{R_L}{R_L + R_o}} \tag{1.1.54}$$

1.1.4.3 Output Resistance

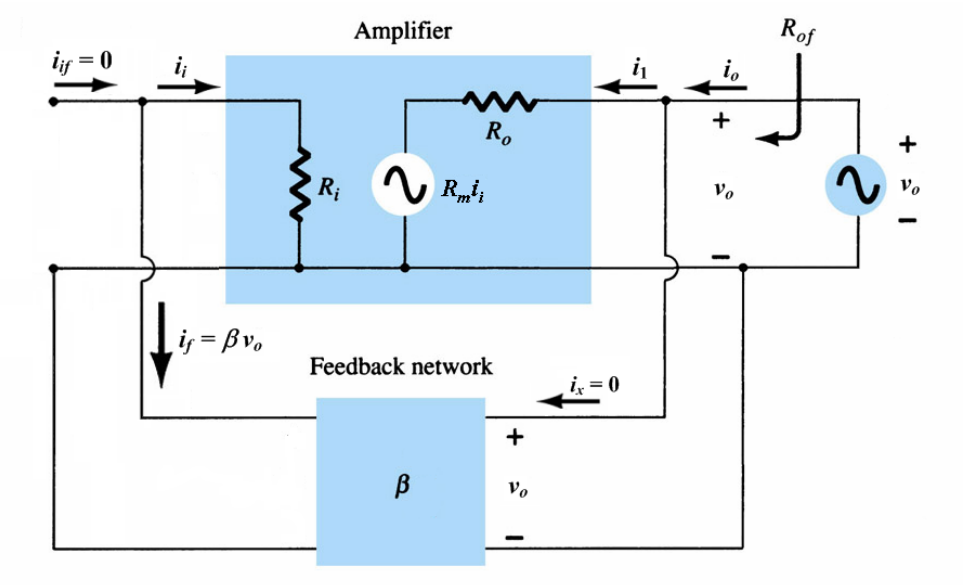


Figure 1.1.23: Voltage-shunt feedback: Output resistance calculation diagram

We can calculate the closed-loop output resistance (i.e., as a Thévenin equivalent resistance) by using the test voltage method as shown in the figure above. Note that as the feedback network is ideal, internal resistance of the feedback network is infinity. So, $i_x = 0$ and $i_o = i_1 + i_x = i_1$. Also as $i_{if} = 0$, $i_i = -i_f = -\beta v_o$. Hence, output resistance R_{of}

$$R_{of} = \left.\frac{v_o}{i_o}\right|_{R_L = v_o, i_{if} = 0} = \frac{v_o}{i_1} = \frac{v_o}{\frac{v_o - R_m i_i}{R_o}} = \frac{R_o v_o}{v_o - R_m(-\beta v_o)} = \frac{R_o v_o}{(1 + \beta R_m) v_o}$$

is derived as

$$\boxed{R_{of} = \frac{R_o}{1 + \beta R_m}} \tag{1.1.55}$$

Effect of Source Resistance under Negative Feedback

- If a current source i_s with an internal resistance R_s is connected at the input, then the gain will drop due to the current divider configuration between R_i and R_s. Hence, closed-loop output resistance will be affected due to the feedback.

  Consequently, closed-loop output resistance R_{of} will be given by

$$\boxed{R_{of} = \frac{R_o}{1 + \beta R_{ms}}} \tag{1.1.56}$$

  where

$$\boxed{R_{ms} = \frac{R_s}{R_s + R_i} R_m} \tag{1.1.57}$$

1.1.5 Current-Series Feedback

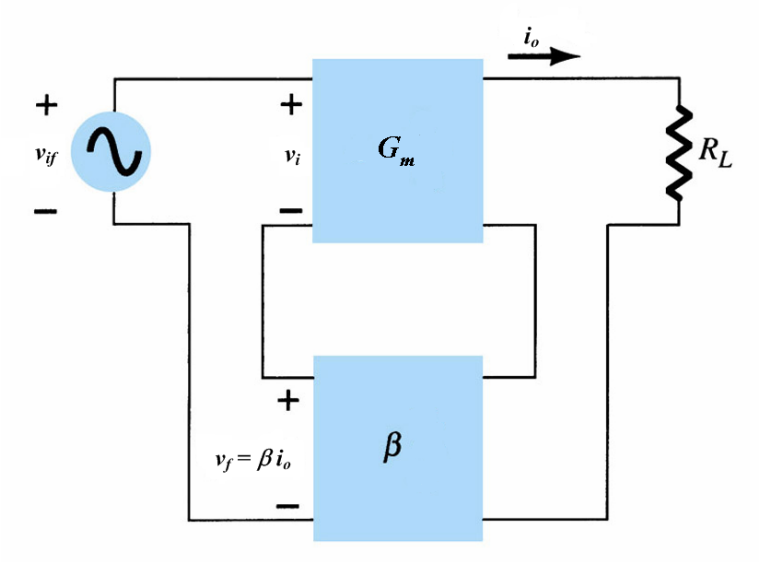


Figure 1.1.24: Current-series feedback: Block diagram

Current-series feedback amplifier is actually a closed-loop transconductance amplifier as shown below. We are going to find the derive the no-load gain G_{mf}, input resistance R_{if} and output resistance R_{of} of this closed-loop system.

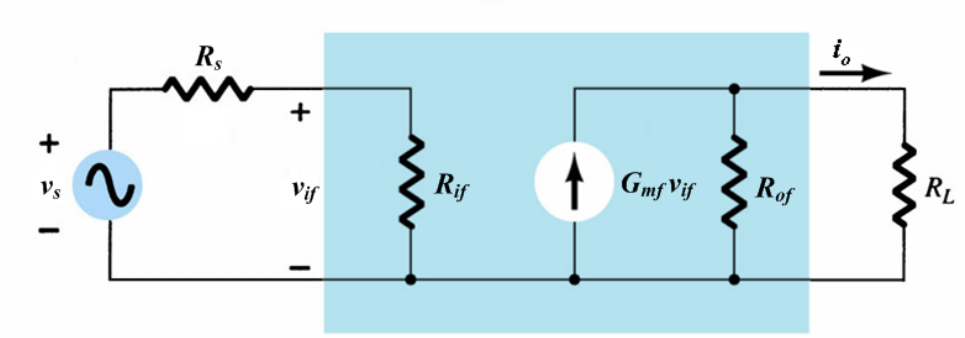


Figure 1.1.25: Current-series feedback amplifier model (i.e., closed-loop transconductance amplifier)

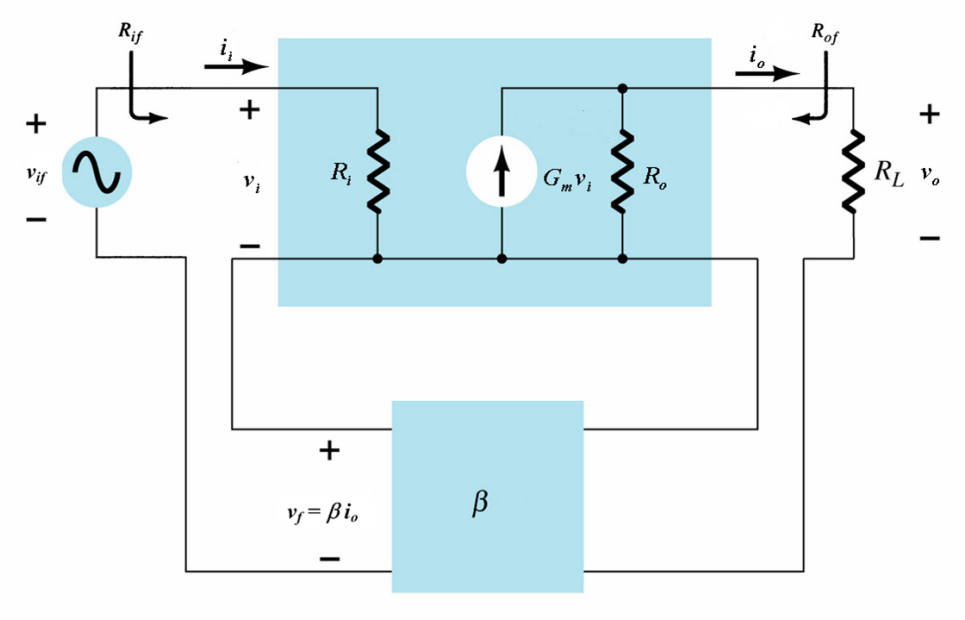


Figure 1.1.26: Current-series feedback: Block diagram with open-loop amplifier parameters

Let us derive no-load gain G_{mf}, input resistance R_{if} and output resistance R_{of} of the current-series feedback system in terms of the open-loop amplifier parameters G_m, R_i and R_o.

$\boxed{G_{mf} =?}$ $\boxed{R_{if} =?}$ $\boxed{R_{of} =?}$

1.1.5.1 No-load Gain

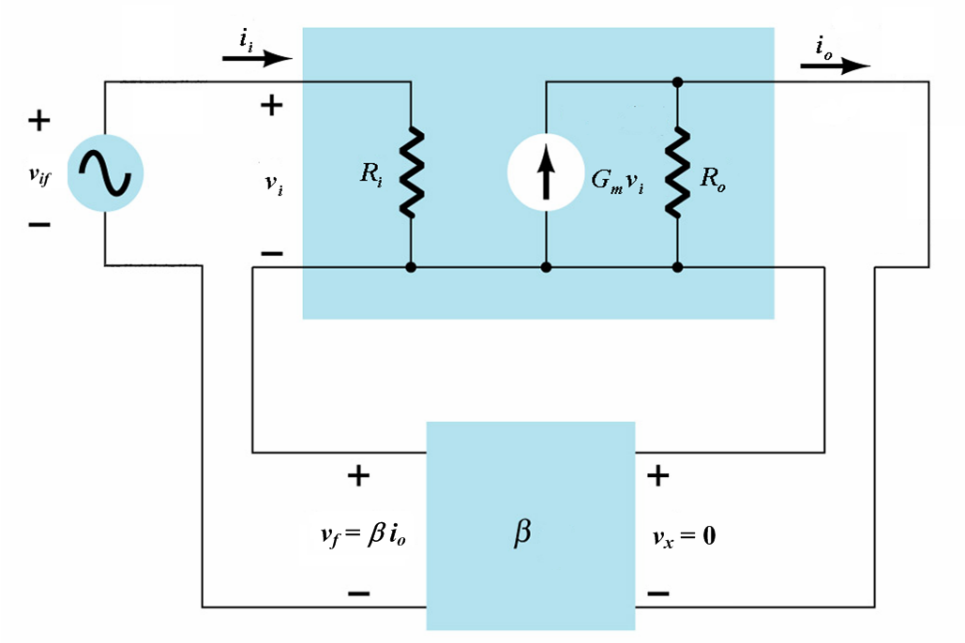


Figure 1.1.27: Current-series feedback: No-load gain calculation diagram

From the above figure, we can quickly derive the closed-loop no-load gain G_{mf} where

$$G_{mf} = \left.\frac{i_o}{v_{if}}\right|_{R_L=0} = \frac{i_o}{v_i + v_f} = \frac{G_m v_i}{(1+\beta G_m) v_i}$$

as

$$\boxed{G_{mf} = \frac{G_m}{1+\beta G_m}} \tag{1.1.58}$$

1.1.5.2 Input Resistance

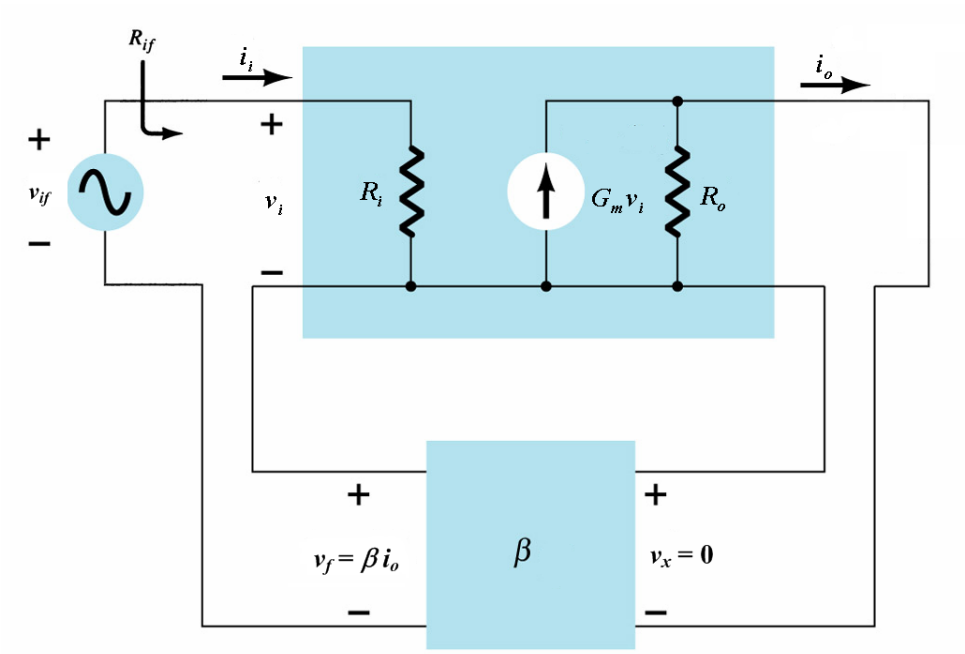


Figure 1.1.28: Current-series feedback: Input resistance calculation diagram

From the above figure, we can quickly derive the closed-loop input resistance R_{if}

$$R_{if} = \left.\frac{v_{if}}{i_i}\right|_{R_L=0} = \frac{v_i + v_f}{i_i} = \frac{(1+\beta G_m) v_i}{i_i} = (1+\beta G_m)\frac{v_i}{i_i}$$

as

$$\boxed{R_{if} = (1+\beta G_m) R_i} \tag{1.1.59}$$

Loading Effect of Negative Feedback

- If a load R_L is connected, then the gain will drop due to the current divider configuration between R_o and R_L. Hence, closed-loop input resistance will be affected due to the feedback.

  Consequently, closed-loop input resistance R_{if} will be given by

$$\boxed{R_{if} = (1 + \beta G_M)\, R_i} \tag{1.1.60}$$

where

$$\boxed{G_M = G_m \frac{R_o}{R_L + R_o}} \tag{1.1.61}$$

1.1.5.3 Output Resistance

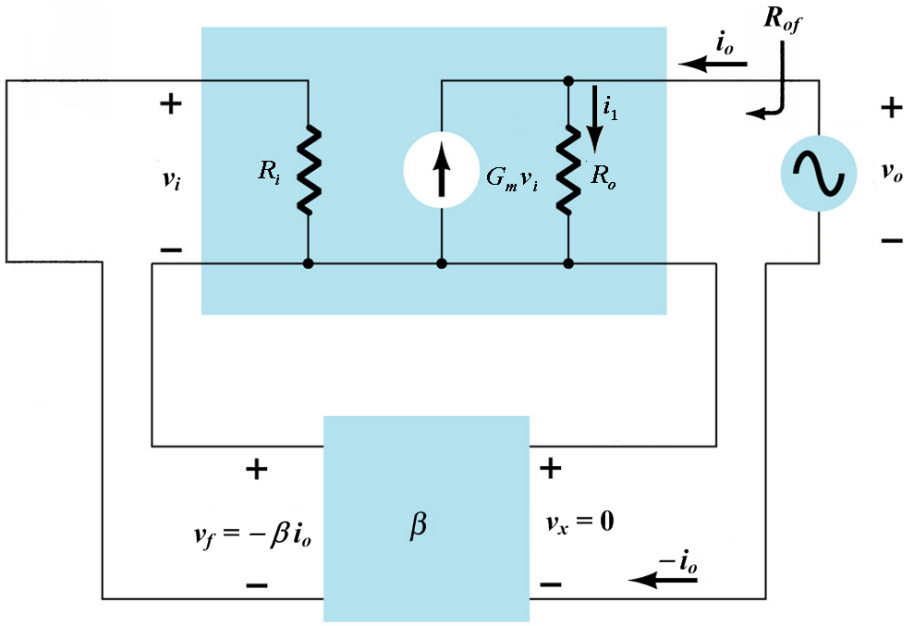


Figure 1.1.29: Current-series feedback: Output resistance calculation diagram

We can calculate the closed-loop output resistance (i.e., as a Thévenin equivalent resistance) by using the test voltage method as shown in the figure above. Note that as the feedback network is ideal, internal resistance of the feedback network is zero. So, $v_x = 0$ and $v_o = i_1 R_o + v_x = i_1 R_o$. Also as $v_{if} = 0$, $v_i = -v_f = \beta i_o$. Hence, output resistance R_{of}

$$R_{of} = \left.\frac{v_o}{i_o}\right|_{R_L = v_o, v_{if} = 0} = \frac{i_1 R_o}{i_o} = \frac{(i_o + G_m v_i) R_o}{i_o} = \frac{(i_o + G_m \beta i_o) R_o}{i_o}$$

is derived as

$$\boxed{R_{of} = (1 + \beta G_m)\, R_o} \tag{1.1.62}$$

Effect of Source Resistance under Negative Feedback

- If a voltage source v_s with an internal resistance R_s is connected at the input, then the gain will drop due to the voltage divider configuration between R_i and R_s. Hence, closed-loop output resistance will be affected due to the feedback.

Consequently, closed-loop output resistance R_{of} will be given by

$$\boxed{R_{of} = (1 + \beta G_{ms})\, R_o} \tag{1.1.63}$$

where

$$\boxed{G_{ms} = \frac{R_i}{R_s + R_i}\, G_m} \tag{1.1.64}$$

1.1.6 Current-Shunt Feedback

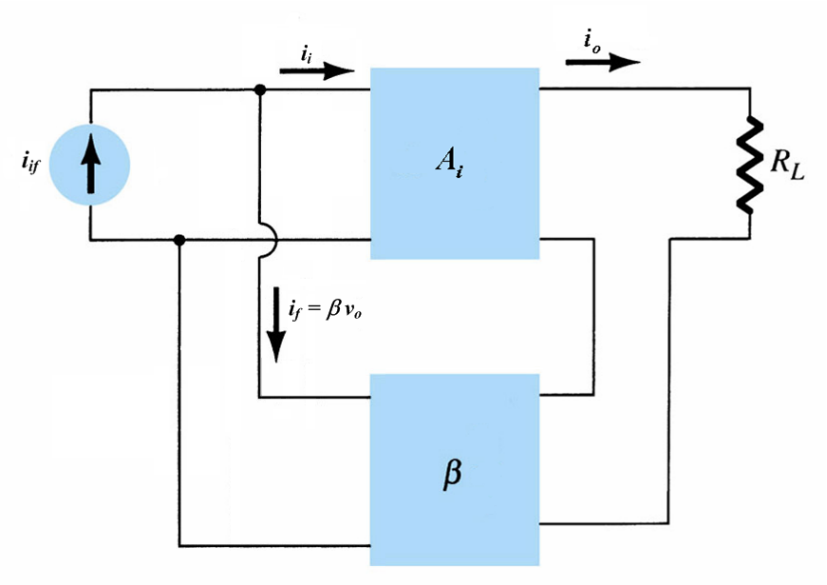


Figure 1.1.30: Current-shunt feedback: Block diagram

Current-shunt feedback amplifier is actually a closed-loop current-gain amplifier as shown below. We are going to find the derive the no-load gain A_{if}, input resistance R_{if} and output resistance R_{of} of this closed-loop system.

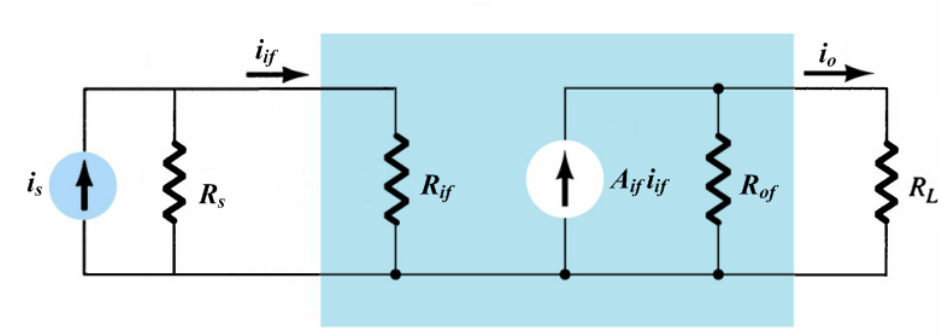


Figure 1.1.31: Current-shunt feedback amplifier model (i.e., closed-loop current-gain amplifier)

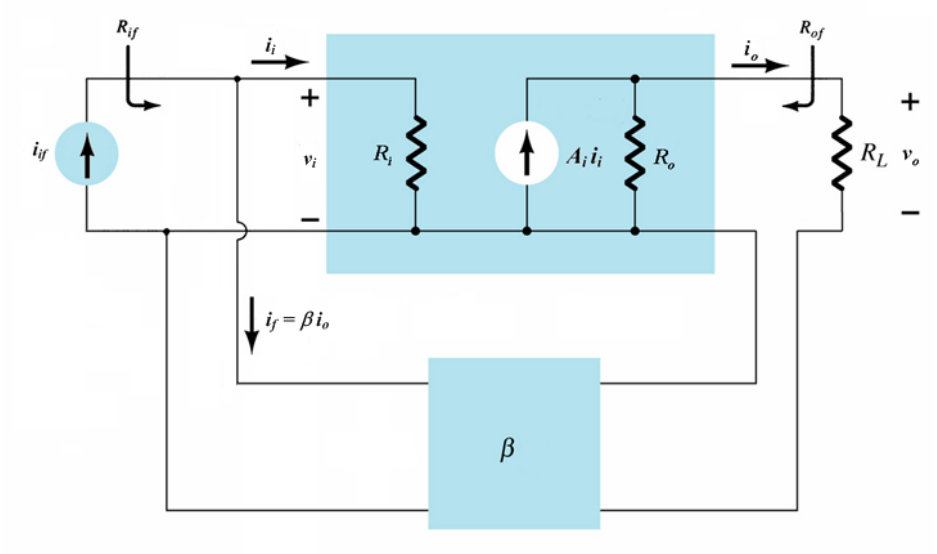


Figure 1.1.32: Current-shunt feedback: Block diagram with open-loop amplifier parameters

Let us derive no-load gain A_{if}, input resistance R_{if} and output resistance R_{of} of the current-shunt feedback system in terms of the open-loop amplifier parameters A_i, R_i and R_o.

$$\boxed{A_{if} = ?} \quad \boxed{R_{if} = ?} \quad \boxed{R_{of} = ?}$$

1.1.6.1 No-load Gain

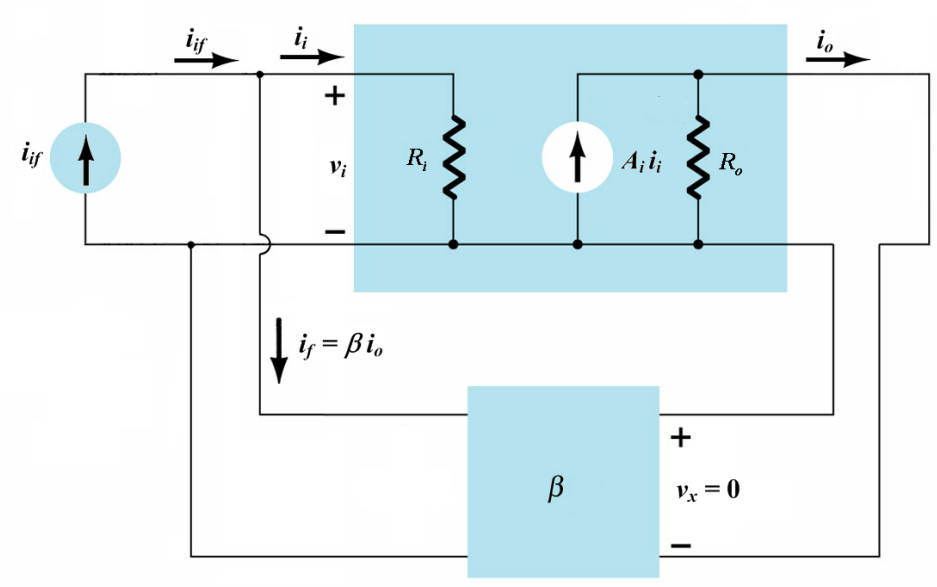


Figure 1.1.33: Current-shunt feedback: No-load gain calculation diagram

From the above figure, we can quickly derive the closed-loop no-load gain A_{if} where

$$A_{if} = \left.\frac{i_o}{i_{if}}\right|_{R_L=0} = \frac{i_o}{i_i + i_f} = \frac{A_i i_i}{(1 + \beta A_i) i_i}$$

as

$$\boxed{A_{if} = \frac{A_i}{1 + \beta A_i}} \tag{1.1.65}$$

1.1.6.2 Input Resistance

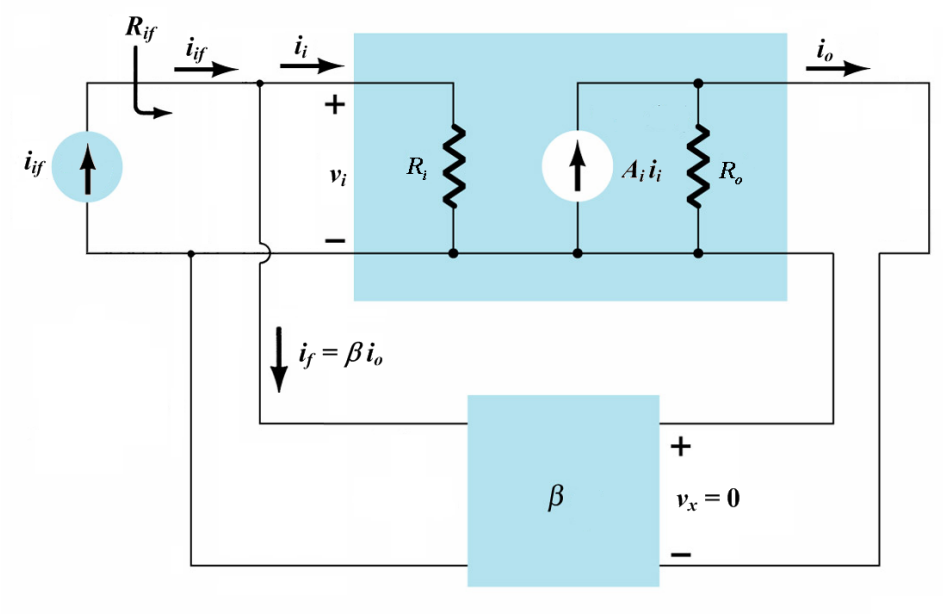


Figure 1.1.34: Current-shunt feedback: Input resistance calculation diagram

From the above figure, we can quickly derive the closed-loop input resistance R_{if}

$$R_{if} = \left.\frac{v_i}{i_{if}}\right|_{R_L=0} = \frac{v_i}{i_i + i_f} = \frac{v_i}{(1 + \beta A_i) i_i}$$

as

$$\boxed{R_{if} = \frac{R_i}{1 + \beta A_i}} \tag{1.1.66}$$

Loading Effect of Negative Feedback

- If a load R_L is connected, then the gain will drop due to the current divider configuration between R_o and R_L. Hence, closed-loop input resistance will be affected due to the feedback.

  Consequently, closed-loop input resistance R_{if} will be given by

$$\boxed{R_{if} = \frac{R_i}{1 + \beta A_I}} \tag{1.1.67}$$

  where

$$\boxed{A_I = A_i \frac{R_o}{R_L + R_o}} \tag{1.1.68}$$

1.1.6.3 Output Resistance

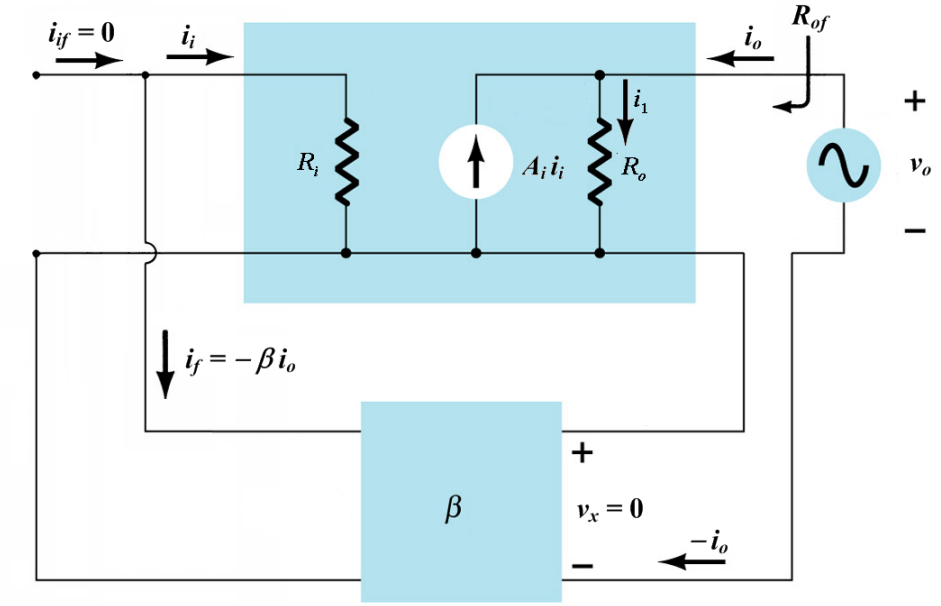


Figure 1.1.35: Current-shunt feedback: Output resistance calculation diagram

We can calculate the closed-loop output resistance (i.e., as a Thévenin equivalent resistance) by using the test voltage method as shown in the figure above. Note that as the feedback network is ideal, internal resistance of the feedback network is zero. So, $v_x = 0$ and $v_o = i_1 R_o + v_x = i_1 R_o$. Also as $i_{if} = 0$, $i_i = -i_f = \beta i_o$. Hence, output resistance R_{of}

$$R_{of} = \left.\frac{v_o}{i_o}\right|_{R_L = v_o, i_{if} = 0} = \frac{i_1 R_o}{i_o} = \frac{(i_o + A_i i_i) R_o}{i_o} = \frac{(i_o + A_i \beta i_o) R_o}{i_o}$$

is derived as

$$\boxed{R_{of} = (1 + \beta A_i)\, R_o} \tag{1.1.69}$$

Effect of Source Resistance under Negative Feedback

- If a current source i_s with an internal resistance R_s is connected at the input, then the gain will drop due to the current divider configuration between R_i and R_s. Hence, closed-loop output resistance will be affected due to the feedback.

  Consequently, closed-loop output resistance R_{of} will be given by

$$\boxed{R_{of} = (1 + \beta A_{is})\, R_o} \tag{1.1.70}$$

  where

$$\boxed{A_{is} = \frac{R_s}{R_s + R_i} A_i} \tag{1.1.71}$$

1.1.7 Summary of Closed-loop Input and Output Resistances

Table below summarizes the closed-loop input and output resistances for each type of feedback.

TABLE 17.2 Effect of Feedback Connection on Input and Output Impedance

	Voltage-Series	*Voltage-Shunt*	*Current-Series*	*Current-Shunt*
R_{if}	$(1+\beta A_V)\,R_i$	$\dfrac{R_i}{1+\beta R_M}$	$(1+\beta G_M)\,R_i$	$\dfrac{R_i}{1+\beta A_I}$
R_{of}	$\dfrac{R_o}{1+\beta A_{vs}}$	$\dfrac{R_o}{1+\beta R_{ms}}$	$(1+\beta G_{ms})\,R_o$	$(1+\beta A_{is})\,R_o$

Figure 1.1.36: Summary table for closed-loop input and output resistance expressions

1.1.8 Analysis of Negative Feedback

The following steps needs to be taken during the analysis of negative feedback.

1. Recognize the type of feedback
2. Derive open-loop circuit (i.e., circuit without feedback)
3. Ensure suitability of the input signal source
4. Obtain open-loop small-signal equivalent circuit
5. Find feedback gain $\beta = X_f/Y$
6. Calculate open-loop parameters A, R_i and R_o
7. Calculate closed-loop parameters A_f, R_{if} and R_{of}

1.1.8.1 Recognize the type of feedback

a) Identify the common circuit elements (i.e., feedback network) in between the input and output loops.

b) Determine input-mixing type (i.e., type of feedback signal X_f)

- *Series-mixing* (feedback signal is voltage, v_f)
  - If the input voltage source v_s is connected to the output with an element in series
    - e.g., when a circuit element, like R_E or R_S, present in the emitter/source terminal of the first transistor when the input is from the base/gate terminal.
- *Shunt-mixing* (feedback signal is current, i_f)

– If the output-circuit is wired to the input circuit allowing the feedback current i_f to flow
  - e.g., collector-feedback configuration or drain-feedback configuration

c) Determine output-sampling type

– *Voltage-sampling* (shunt-connection)
  ⋆ If $X_f = 0$ when $v_o = 0\,\text{V}$ (i.e., $R_L = 0\,\Omega$)
– *Current-sampling* (series-connection)
  ⋆ If $X_f = 0$ when $i_o = 0\,\text{A}$ (i.e., $R_L = \infty\,\Omega$)

NOTE 1: If both tests hold, then select the one where feedback gain β does not contain the load (or effective load) in its expression.

NOTE 2: If the feedback network is connected in **parallel** to the output, then it is **voltage-sampling**. Similarly, if the feedback network is connected in **series** to the output, then it is **current-sampling**

1.1.8.2 Derive open-loop circuit

a) Obtain the open-loop input circuitry

◦ *Voltage-sampling*

– Make $X_f = 0$ by making $v_o = 0$, i.e., short-circuit the output connection.

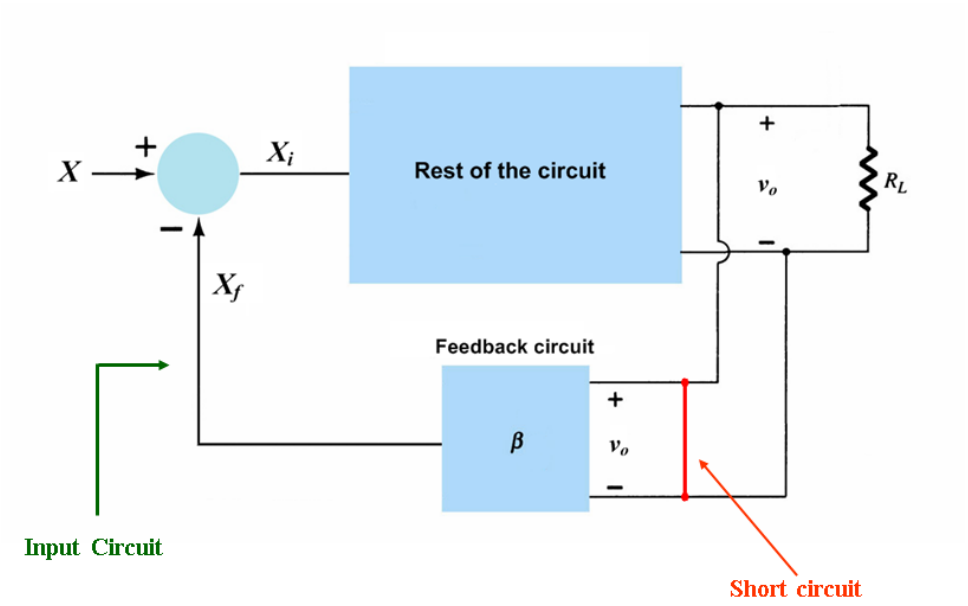


Figure 1.1.37: Obtaining the open-loop input circuitry under voltage-sampling

◦ *Current-sampling*

– Make $X_f = 0$ by making $i_o = 0$, i.e., open-circuit the output connection.

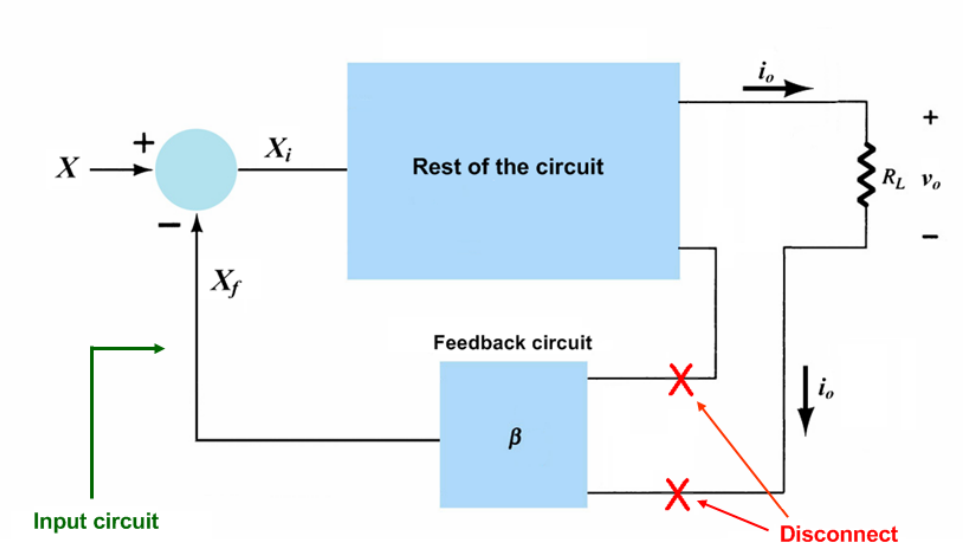


Figure 1.1.38: Obtaining the open-loop input circuitry under current-sampling

b) Obtain the open-loop output circuitry

- *Series-mixing*
  - Make the reverse feedback signal $Y_f = 0$ by making $i_i = 0$ where $Y_f = \beta_r i_i$ and β_r is the reverse feedback gain, i.e., open-circuit the input connection.

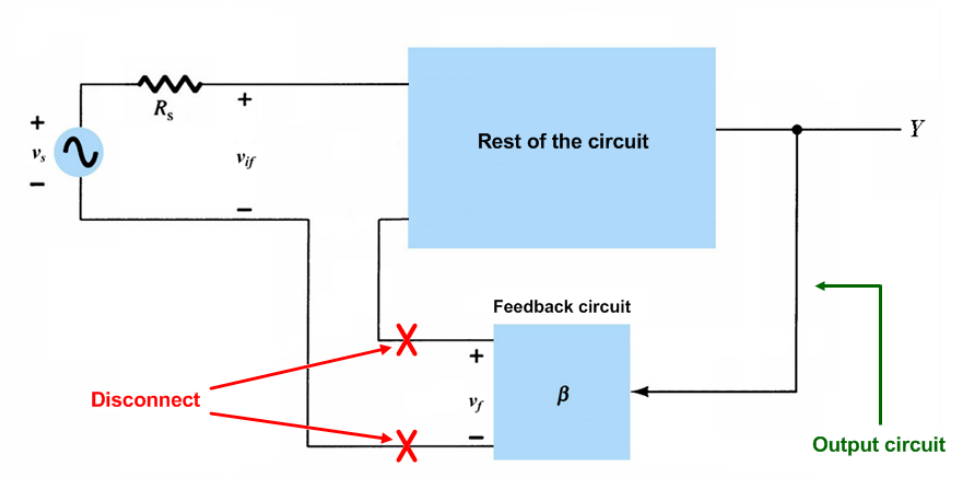


Figure 1.1.39: Obtaining the open-loop output circuitry under series-mixing

- *Shunt-mixing*
  - Make the reverse feedback signal $Y_f = 0$ by making $v_i = 0$ where $Y_f = \beta_r v_i$ and β_r is the reverse feedback gain, i.e., short-circuit the input connection.

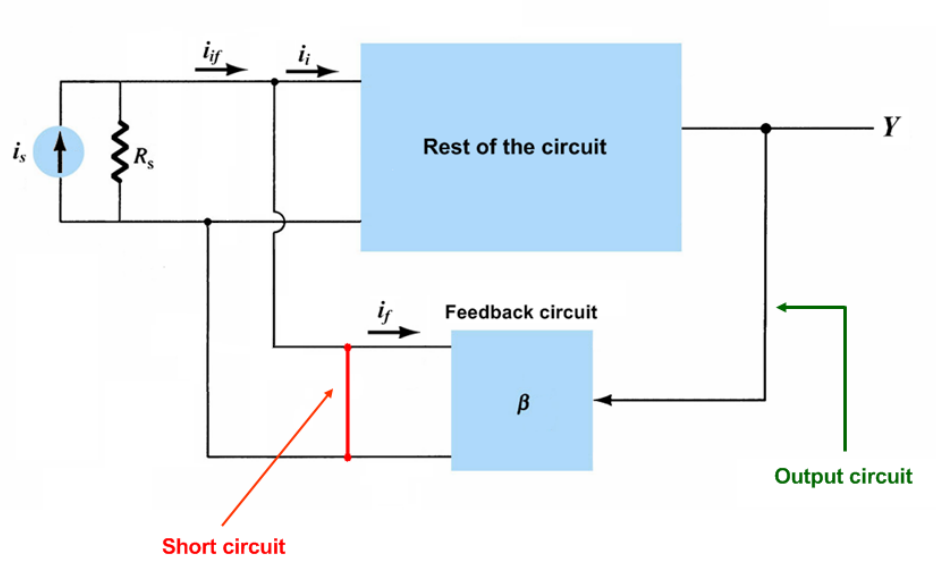


Figure 1.1.40: Obtaining the open-loop output circuitry under shunt-mixing

NOTE: According to the connection type, always **short-circuit** a **shunt-connection** (or parallel-connection) and always **open-circuit** a **series-connection** in order to eliminate the effect of the observable. This is true **for both output and input connections** of the feedback network.

c) Then draw the open-loop circuit by putting the input circuitry and output circuitry together

i. Open-loop circuit diagram for **voltage-series** feedback

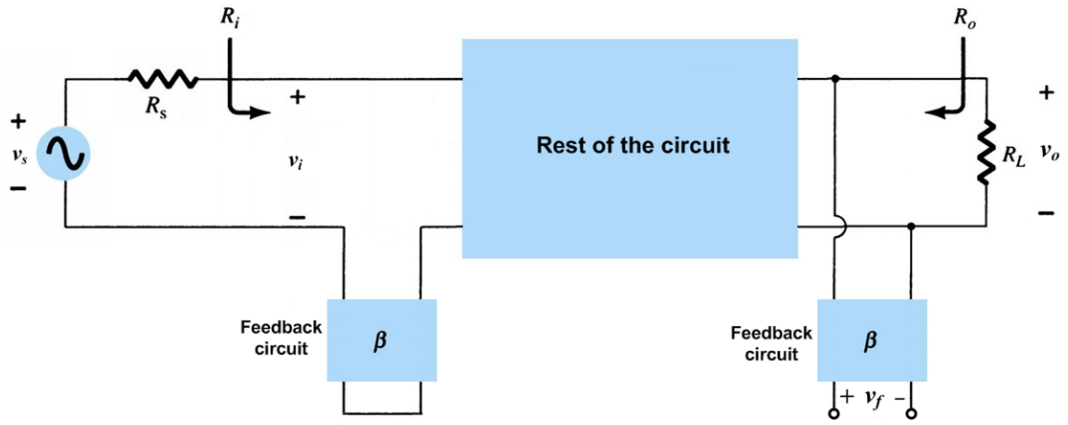


Figure 1.1.41: Open-loop circuit diagram for voltage-series feedback

ii. Open-loop circuit diagram for **voltage-shunt** feedback

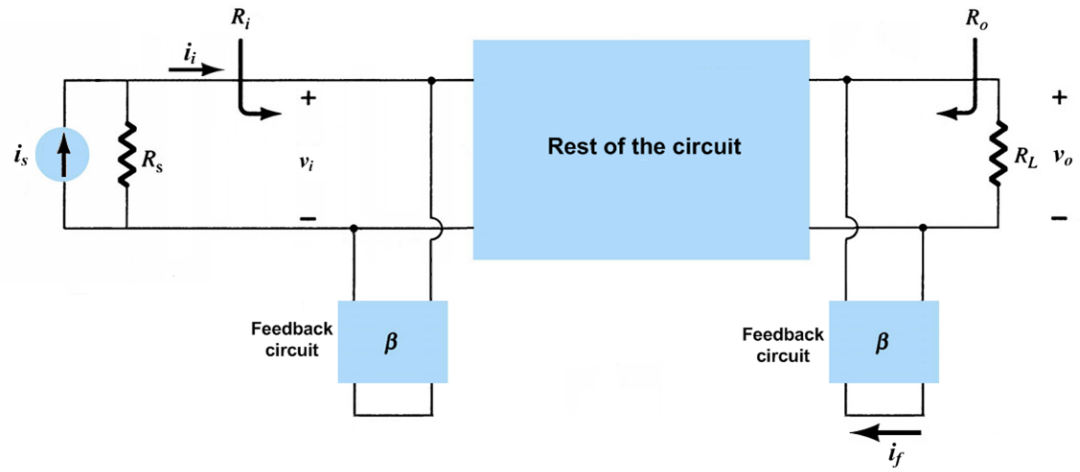


Figure 1.1.42: Open-loop circuit diagram for voltage-shunt feedback

iii. Open-loop circuit diagram for **current-series** feedback

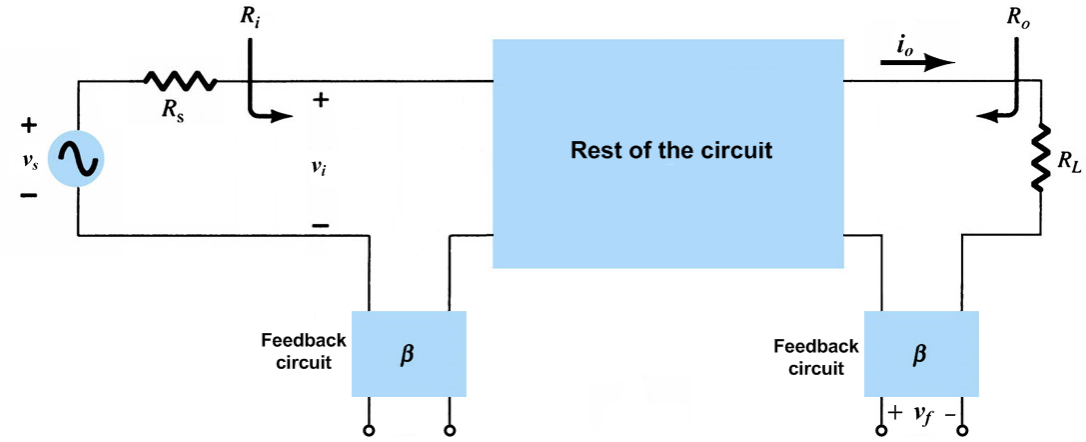


Figure 1.1.43: Open-loop circuit diagram for current-series feedback

iv. Open-loop circuit diagram for **current-shunt** feedback

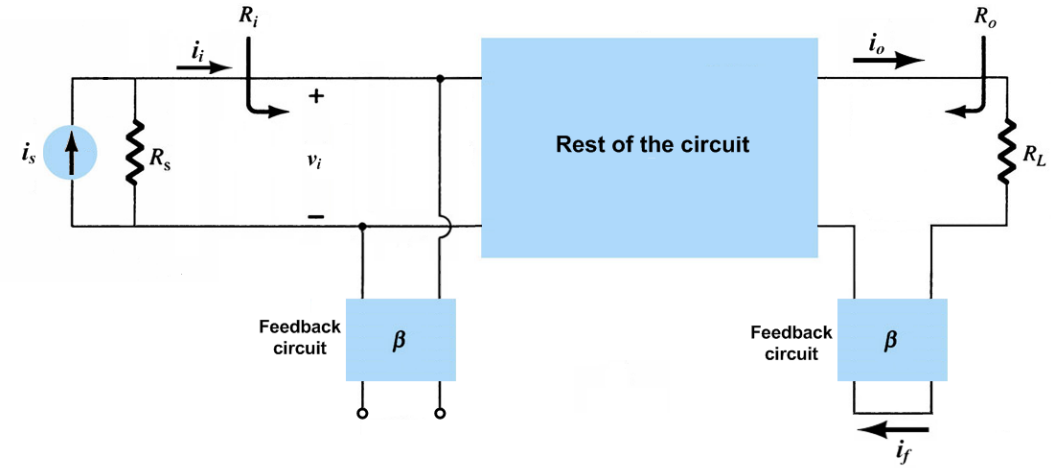


Figure 1.1.44: Open-loop circuit diagram for current-shunt feedback

1.1.8.3 Ensure suitability of the input signal source

If feedback signal X_f is a

- *Voltage signal* (in the case of series-mixing)
  - Use a Thévenin voltage source,
- *Current signal* (in the case of shunt-mixing)
  - Use a Norton current source.

NOTE: If necessary, perform source transformation (voltage source $\leftrightarrow$ current source).

1.1.8.4 Obtain open-loop small-signal equivalent circuit

Replace each active device (e.g. BJT, JFET, MOSFET etc.) in the open-loop circuit by their appropriate small-signal model and draw the open-loop small signal equivalent circuit.

1.1.8.5 Find feedback gain β

- Obtain feedback gain $\beta = \dfrac{X_f}{Y}$
  - Feedback circuit cannot include either the source resistance R_s or the load resistance R_L.
    - i.e., $\beta \neq \beta(R_s, R_L)$, in other words, β cannot be a function of R_s or R_L.

NOTE: Any external circuit element (or equivalent element) via which we obtain the output voltage v_o and output current i_o will be the **effective load** in the circuit, even though it was not labelled explicitly as R_L.

1.1.8.6 Summary of feedback amplifier analysis

The table below shows the summary of the feedback amplifier analysis

Characteristic \ Topology	(1) Voltage series	(2) Current series	(3) Current shunt	(4) Voltage shunt
Feedback signal X_f	Voltage	Voltage	Current	Current
Sampled signal X_o	Voltage	Current	Current	Voltage
To find input loop, set†	$V_o = 0$	$I_o = 0$	$I_o = 0$	$V_o = 0$
To find output loop, set†	$I_i = 0$	$I_i = 0$	$V_i = 0$	$V_i = 0$
Signal source	Thévenin	Thévenin	Norton	Norton
$\beta = X_f/X_o$	V_f/V_o	V_f/I_o	I_f/I_o	I_f/V_o
$A = X_o/X_i$	$A_V = V_o/V_i$	$G_M = I_o/V_i$	$A_I = I_o/I_i$	$R_M = V_o/I_i$
$D = 1 + \beta A$	$1 + \beta A_V$	$1 + \beta G_M$	$1 + \beta A_I$	$1 + \beta R_M$
A_f	A_V/D	G_M/D	A_I/D	R_M/D
R_{if}	R_iD	R_iD	R_i/D	R_i/D
R_{of}	$\dfrac{R_o}{1 + \beta A_v}$	$R_o(1 + \beta G_m)$	$R_o(1 + \beta A_i)$	$\dfrac{R_o}{1 + \beta R_m}$

†This procedure gives the basic amplifier circuit without feedback but taking the loading of β, R_L and R_s into account.

Figure 1.1.45: Summary table for negative feedback amplifier analysis

1.1.9 Examples

Example 1.2: Determine the feedback type and derive the open-loop and closed-loop amplifier parameters (i.e., input resistance, output resistance and gain) for the source follower circuit below.

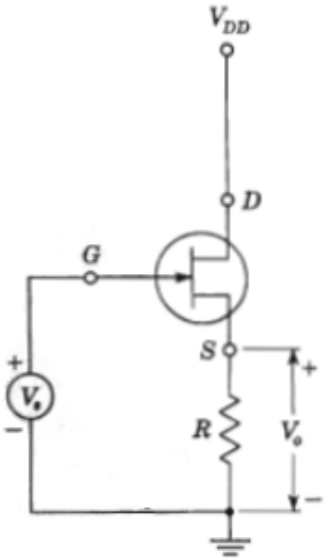


Figure 1.1.46: A source follower circuit (a voltage-series feedback example).

Solution: Output and input networks have one common element R which provides feedback in this circuit. It is connected in series to the input circuitry. The feedback signal v_f is the voltage across resistor R. Output signal sampled is output voltage v_o (because if output current was sampled, then the feedback gain β will be equal to the value of resistor R, but R is the effective load in this circuit and feedback network cannot include the load). So, this circuit has **voltage-series feedback**.

Feedback network's input connection is between the JFET source terminal and the ground. Similarly, feedback network's output connection is also between the JFET source terminal and the ground terminal. In order to obtain the open-loop input circuitry we short circuit the output connection terminals of the feedback network. Then, to obtain the open-loop output circuitry we disconnect the input connection terminals of the feedback network (so, resistor R becomes part of the open-loop output circuitry). Then, as shown in Figure 1.1.41 e put the open-loop input and output circuitries together and we obtain the initial open-loop circuit (i.e., circuit without feedback) below. Note that, we have to indicate the feedback signal v_f at the output circuitry of the open-loop circuit with the correct polarity.

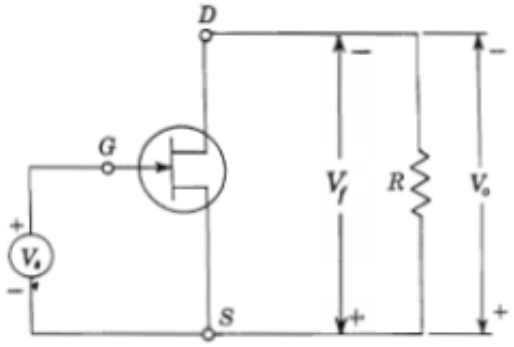


Figure 1.1.47: Initial open-loop circuit of the circuit given in Figure 1.1.46.

Now, let us replace the JFET transistor with its small-signal equivalent model and obtain the open-loop small-signal equivalent circuit below

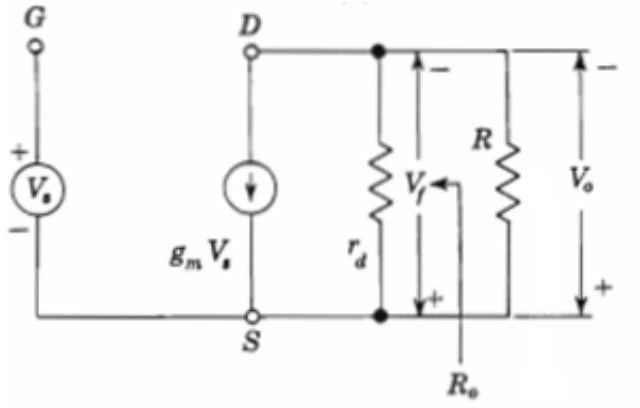


Figure 1.1.48: Open-loop small-signal equivalent circuit of Figure 1.1.46.

Now, the feedback gain β is given by $\boxed{\beta = \dfrac{v_f}{v_o} = 1}$.

Note that, as output current flows through and output voltage is across R, R is the effective load, i.e., $\boxed{R_L \equiv R}$.

From the figure above let us calculate the open-loop amplifier parameters R_i, R_o and A_v.

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = \infty} \qquad \boxed{R_o = \left.\frac{v_o}{i_o}\right|_{R_L=v_o, v_s=0} = r_{ds}} \qquad \boxed{A_v = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = g_m r_{ds}}$$

Now, let us calculate the closed-loop amplifier parameters R_{if}, R_{of} and A_{vf} using the voltage-series feedback formulas derived before.

$$\boxed{R_{if} = (1 + \beta A_V)\, R_i = [1 + g_m\,(r_{ds}||R)] \cdot \infty = \infty}$$

$$\boxed{R_{of} = \frac{R_o}{1 + \beta A_{vs}} = \frac{r_{ds}}{1 + g_m r_{ds}} \approx \frac{1}{g_m}}$$

$$\boxed{A_{vf} = \frac{A_v}{1 + \beta A_v} = \frac{g_m r_{ds}}{1 + g_m r_{ds}} \approx 1}$$

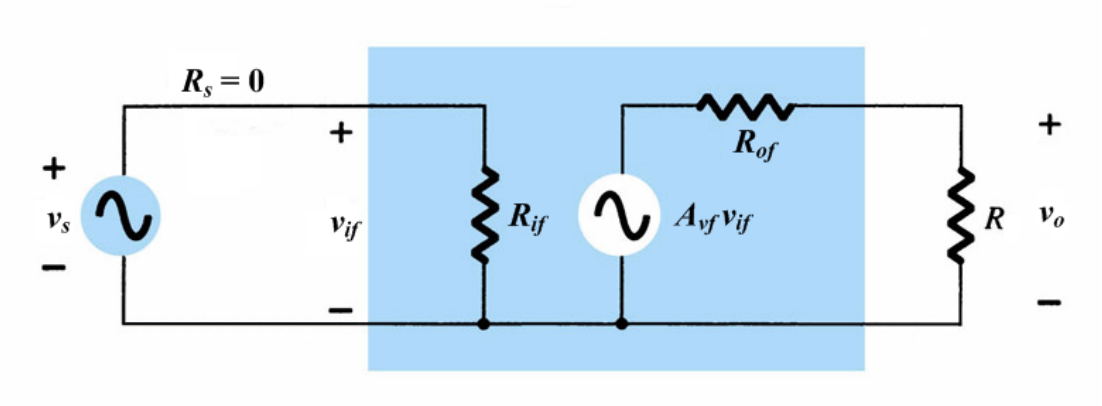


Figure 1.1.49: Equivalent closed-loop amplifier block diagram of the circuit given in Figure 1.1.46.

From the closed-loop amplifier diagram above, we can also find the overall closed-loop voltage gain A_{Vsf}, as

$$\boxed{\begin{aligned} A_{Vsf} &= \frac{R_{if}}{R_s + R_{if}}\, A_{vf}\, \frac{R_L}{R_{of} + R_L} \\ &= A_{vf}\, \frac{R}{R_{of} + R} \end{aligned}}$$

Example 1.3: Determine the feedback type, derive the open-loop circuit and find feedback gain β for the feedback amplifier shown below.

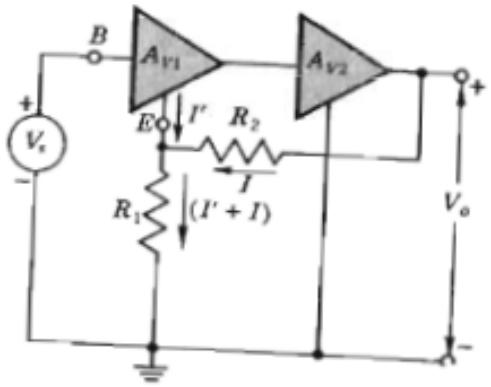


Figure 1.1.50: A multistage amplifier system (a voltage-series feedback example).

Solution: Feedback type is voltage-series feedback and feedback network, consisting of resistors R_1 and R_2, connects the output and input networks to each other. Consequently, open-loop circuit is derived as shown below

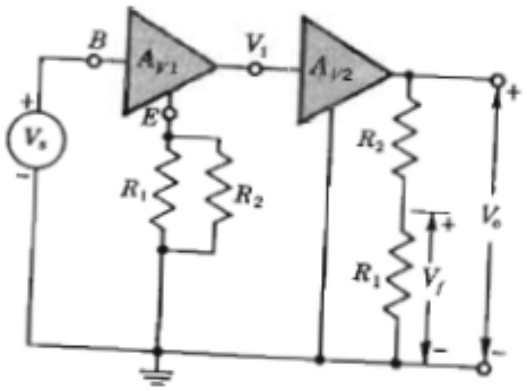


Figure 1.1.51: Open-loop circuit of the circuit given in Figure 1.1.50.

Thus, feedback gain β is found as $\boxed{\beta = \dfrac{v_f}{v_o} = \dfrac{R_1}{R_1 + R_2}}$.

Example 1.4: Determine the feedback type and derive the open-loop and closed-loop amplifier parameters (i.e., input resistance, output resistance and gain) for the collector feedback circuit below.

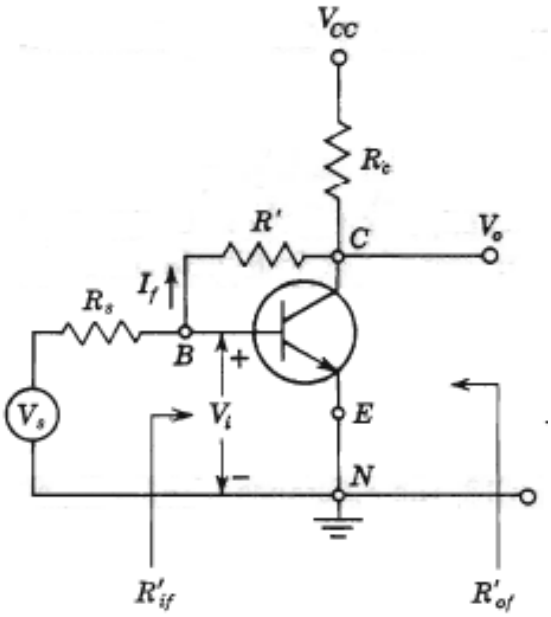


Figure 1.1.52: A collector feedback circuit (a voltage-shunt feedback example)

Solution: Output and input network have one common element R' which provides feedback in this circuit. It is connected in parallel (i.e., shunt connection) to the input circuitry. The feedback signal i_f is the current through resistor R'. Output signal sampled is output voltage v_o. So, this circuit has **voltage-shunt feedback**.

Feedback network's input connection is between the BJT base terminal and the ground. Similarly, feedback network's output connection is between the BJT collector terminal and the ground. In order to obtain the open-loop input circuitry, we short circuit the output connection terminals of the feedback network. Then, to obtain the open-loop output circuitry we short circuit the input connection terminals of the feedback network. Then, as shown in Figure 1.1.42 e put the open-loop input and output circuitries together and we obtain the initial open-loop circuit (i.e., circuit without feedback) below. Note that, we have transformed the input voltage source to a current source as feedback signal is a current signal and also indicated the feedback signal i_f at the output circuitry of the open-loop circuit with the correct direction.

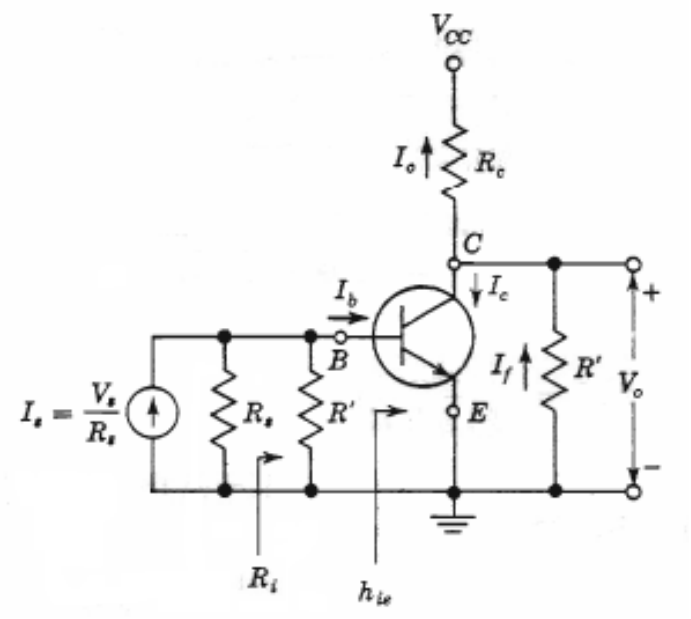


Figure 1.1.53: Initial open-loop circuit of the circuit given in Figure 1.1.52.

Now, the feedback gain β is given by $\boxed{\beta = \frac{i_f}{v_o} = \frac{i_f}{-i_f R'} = -\frac{1}{R'}}$.

Note that, as output current flows through and output voltage is across R_C, R_C is the effective load, i.e., $\boxed{R_L \equiv R_C}$.

From the figure above let us calculate the open-loop amplifier parameters R_i, R_o and R_m.

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=\infty} = R' || h_{ie}} \qquad \boxed{R_o = \left.\frac{v_o}{i_o}\right|_{R_L=v_o, i_s=0} = R' || \frac{1}{h_{oe}}}$$

$$\boxed{R_m = \left.\frac{v_o}{i_i}\right|_{R_L=\infty} = -h_{fe}\left(R' || \frac{1}{h_{oe}}\right)\frac{R'}{R' + h_{ie}}}$$

Now, let us calculate the closed-loop amplifier parameters R_{if}, R_{of} and R_{mf} using the voltage-shunt feedback formulas derived before.

$$R_{if} = \frac{R_i}{1+\beta R_M} = \frac{R'||h_{ie}}{1+(R'||1/h_{oe})\dfrac{h_{fe}}{R'+h_{ie}}\dfrac{R_C}{(R'||1/h_{oe})+R_C}} \approx \frac{h_{ie}}{1+h_{fe}\dfrac{R_C}{R'}}$$

$$R_{of} = \frac{R_o}{1+\beta R_{ms}} = \frac{R'||1/h_{oe}}{1+\dfrac{R_s}{R_s+R_i}(R'||1/h_{oe})\dfrac{h_{fe}}{R'+h_{ie}}} \approx \left(1+\frac{R_i}{R_s}\right)\frac{R'}{h_{fe}}$$

$$R_{mf} = \frac{R_m}{1+\beta R_m} = \frac{-(R'||1/h_{oe})\dfrac{h_{fe}R'}{R'+h_{ie}}}{1+(R'||1/h_{oe})\dfrac{h_{fe}}{R'+h_{ie}}} \approx -R'$$

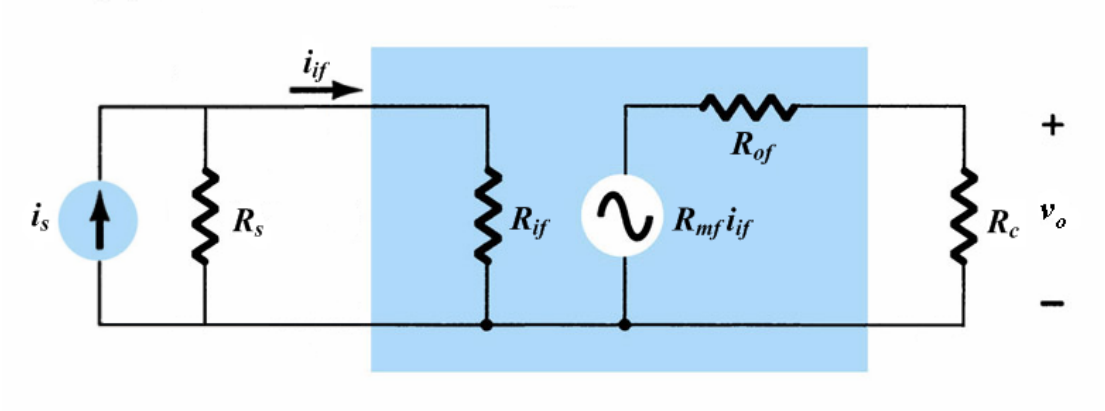


Figure 1.1.54: Equivalent closed-loop amplifier block diagram of the circuit given in Figure 1.1.52.

From the closed-loop amplifier diagram above, we can also find the overall closed-loop transresistance gain R_{Msf}, as

$$R_{Msf} = \frac{v_o}{i_s} = \frac{R_s}{R_s+R_{if}} R_{mf} \frac{R_C}{R_{of}+R_C}$$

where $i_s = \dfrac{v_s}{R_s}$

Thus, overall closed-loop voltage gain A_{Vsf} will be given by

$$A_{Vsf} = \frac{v_o}{v_s} = \frac{v_o}{i_s R_s} = \frac{1}{R_s} R_{Msf}$$

Example 1.5: Determine the feedback type and derive the open-loop and closed-loop amplifier parameters (i.e., input resistance, output resistance and gain) for the common emitter circuit below.

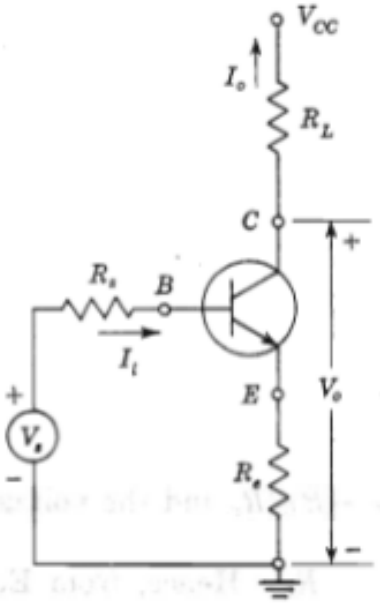


Figure 1.1.55: A common emitter circuit (a current-series feedback example).

Solution: Output and input networks have one common element R_E which provides feedback in this circuit. It is connected in series to the input circuitry. The feedback signal v_f is the voltage across resistor R_E. Output signal sampled is output current i_o. So, this circuit has **current-series feedback**.

Feedback network's input connection is between the BJT emitter terminal and the ground. Similarly, feedback network's output connection is also between the BJT emitter terminal and the ground. In order to obtain the open-loop input circuitry, we disconnect the output connection terminals of the feedback network. Then, to obtain the open-loop output circuitry we also disconnect the input connection terminals of the feedback network. Then, as shown in Figure 1.1.43 e put the open-loop input and output circuitries together and we obtain the initial open-loop circuit (i.e., circuit without feedback) below. Note that, have to indicate the feedback signal v_f at the output circuitry of the open-loop circuit with the correct polarity.

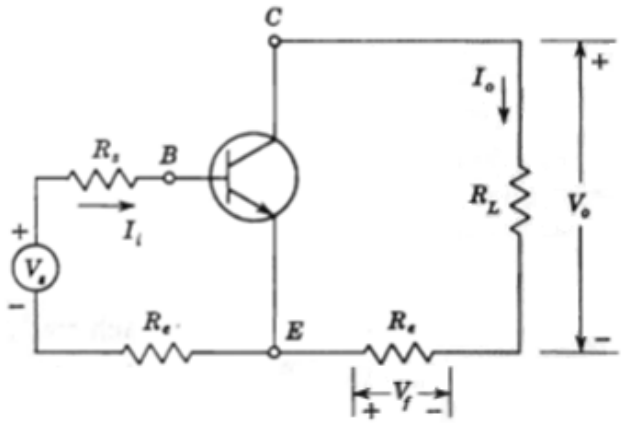


Figure 1.1.56: Initial open-loop circuit of the circuit given in Figure 1.1.55.

Now, let us replace the BJT transistor with its small-signal equivalent model and obtain the open-loop small-signal equivalent circuit below

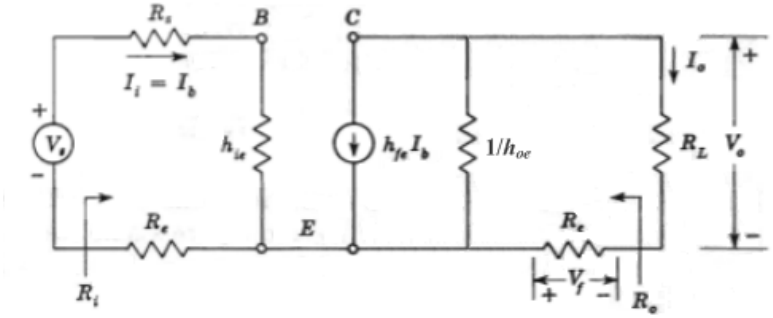


Figure 1.1.57: Open-loop small-signal equivalent circuit of Figure 1.1.55.

Now, the feedback gain β is given by $\boxed{\beta = \dfrac{v_f}{i_o} = \dfrac{-R_E i_o}{i_o} = -R_E}$.

Note that, as output current flows through and output voltage is across R_L, R_L is the effective load.

From the figure above let us calculate the open-loop amplifier parameters R_i, R_o and G_m.

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=0} = R_E + h_{ie}} \qquad \boxed{R_o = \left.\frac{v_o}{i_o}\right|_{R_L=v_o,v_s=0} = 1/h_{oe} + R_E}$$

$$\boxed{\begin{aligned} G_m = \left.\frac{i_o}{v_i}\right|_{R_L=0} &= -\frac{1/h_{oe}}{1/h_{oe} + R_E}\frac{h_{fe}}{R_E + h_{ie}} \\ &\approx \frac{-h_{fe}}{R_E + h_{ie}} \end{aligned}}$$

Now, let us calculate the closed-loop amplifier parameters R_{if}, R_{of} and G_{mf} using the current-series feedback formulas derived before.

$$\boxed{\begin{aligned} R_{if} = (1 + \beta G_M)\, R_i &= \left(1 + \frac{h_{fe}R_E}{R_E + h_{ie}}\,\frac{1/h_{oe} + R_E}{1/h_{oe} + R_E + R_L}\right)(R_E + h_{ie}) \\ &\approx (h_{fe} + 1)\, R_E + h_{ie} \end{aligned}}$$

$$\boxed{R_{of} = (1 + \beta G_{ms})\, R_o = \left(1 + \frac{R_E + h_{ie}}{R_s + R_E + h_{ie}}\,\frac{h_{fe}R_E}{R_E + h_{ie}}\right)(1/h_{oe} + R_E) \approx \infty}$$

$$\boxed{G_{mf} = \frac{G_m}{1 + \beta G_m} = \frac{\dfrac{-h_{fe}}{R_E + h_{ie}}}{1 + \dfrac{h_{fe}R_E}{R_E + h_{ie}}} \approx -\frac{1}{R_E}}$$

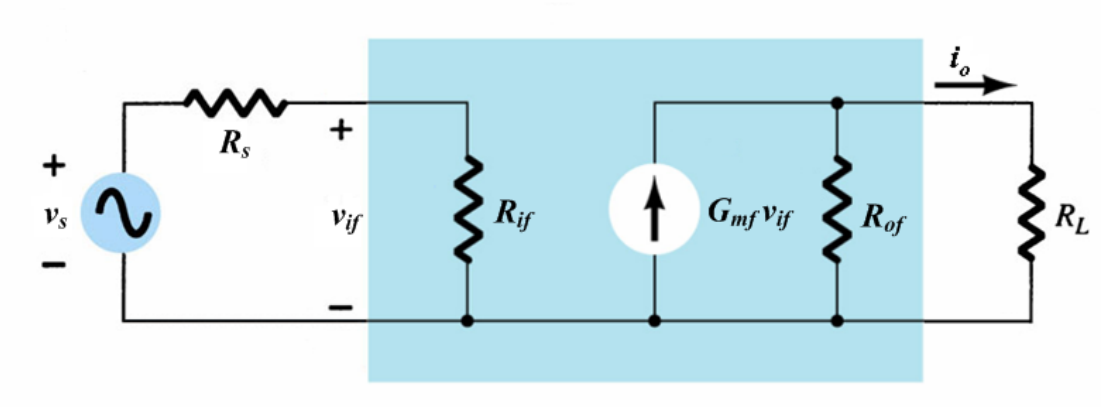


Figure 1.1.58: Equivalent closed-loop amplifier block diagram of the circuit given in Figure 1.1.55.

From the closed-loop amplifier diagram above, we can also find the overall closed-loop transconductance gain G_{Msf}, as

$$\boxed{G_{Msf} = \frac{i_o}{v_s} = \frac{R_{if}}{R_s + R_{if}} G_{mf} \frac{R_{of}}{R_{of} + R_L}}$$

Thus, overall closed-loop voltage gain A_{Vsf} will be given by

$$\boxed{A_{Vsf} = \frac{v_o}{v_s} = \frac{i_o R_L}{v_s} = G_{Msf} R_L}$$

Example 1.6: Determine the feedback type and derive the open-loop and closed-loop amplifier parameters (i.e., input resistance, output resistance and gain) for the multistage BJT circuit below.

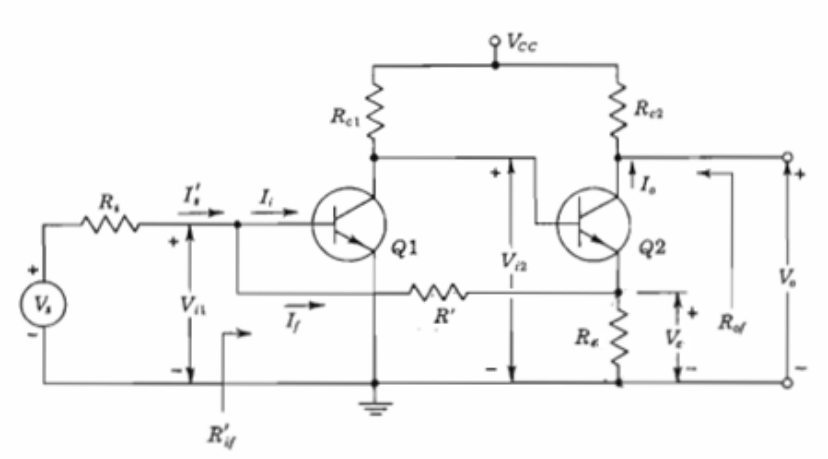


Figure 1.1.59: A multistage BJT circuit (a current-shunt feedback example).

Solution: Output and input networks have two common elements R' and R_E which provide feedback in this circuit. It is connected in parallel (i.e., shunt connection) to the input circuitry. The feedback signal i_f is the voltage through resistor R'. Output signal sampled is output current i_o. So, this circuit has **current-shunt feedback**.

Feedback network's input connection is between the base terminal of Q_1 and the ground. Similarly, feedback network's output connection is between the emitter terminal of Q_2 and the ground. In order to obtain the open-loop input circuitry, we disconnect the output connection terminals of the feedback network. Then, to obtain the open-loop output circuitry we short circuit the input connection terminals of the feedback network. Then, as shown in Figure 1.1.44 e put the open-loop input and output circuitries together and we obtain the initial open-loop circuit (i.e., circuit without feedback) below. Note that, have to indicate the feedback signal i_f at the output circuitry of the open-loop circuit with the correct direction.

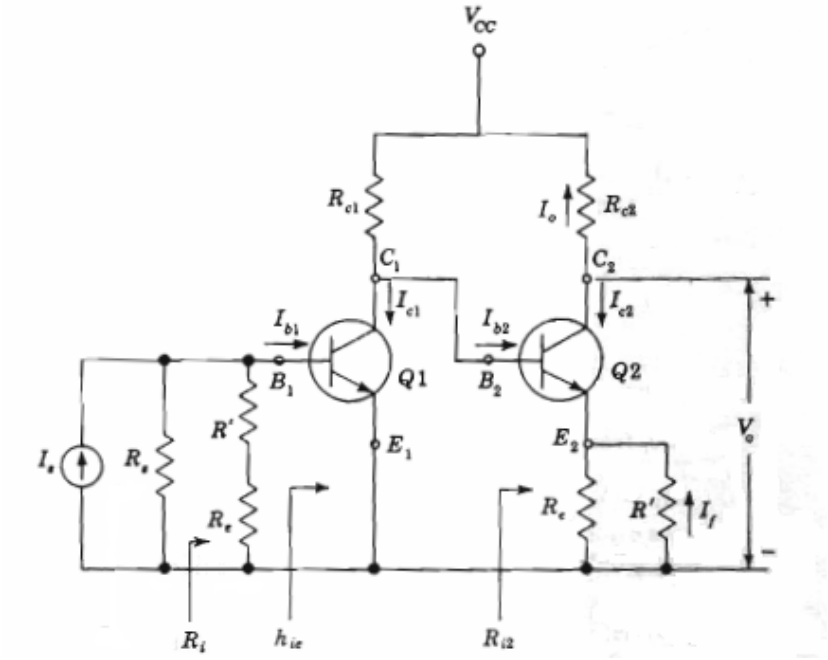


Figure 1.1.60: Initial open-loop circuit of the closed-loop circuit given in Figure 1.1.59.

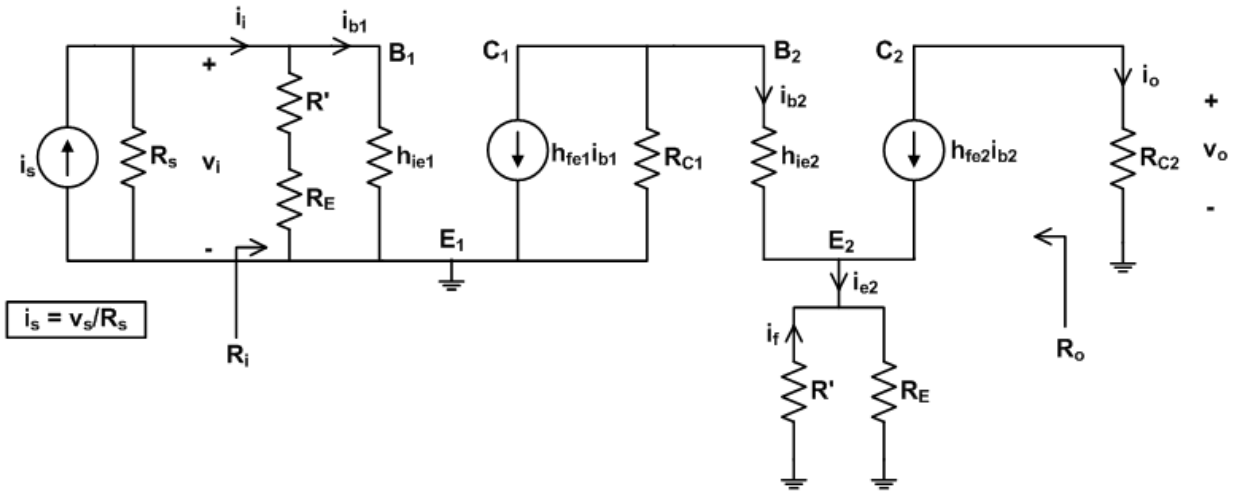


Figure 1.1.61: Small-signal open-loop circuit of the closed-loop circuit given in Figure 1.1.59.

Now, the feedback gain β is given by $\boxed{\beta = \dfrac{i_f}{i_o} = \dfrac{R_E}{R' + R_E}}$.

Note that, as output current flows through and output voltage is across R_{C2}, R_{C2} is the effective load, i.e., $\boxed{R_L \equiv R_{C2}}$.

From the figure above let us calculate the open-loop amplifier parameters R_i, R_o and A_i. Note that, for simplicity we take $h_{oe_1} = h_{oe_2} = 0$.

$$\boxed{R_i = \left.\frac{v_i}{i_i}\right|_{R_L=0} = (R' + R_E)||h_{ie_1}} \qquad \boxed{R_o = \left.\frac{v_o}{i_o}\right|_{R_L=v_o, i_s=0} = \infty}$$

Before calculating the total gain A_i, let us first calculate no-load gain of the second stage A_{i_2} and loaded gain of the first stage A_{I_1} as follows

$$A_{i_2} = \left.\frac{i_o}{i_{i_2}}\right|_{R_L=0} = \frac{i_o}{i_{b_2}} = -h_{fe_2}$$

Note that $i_{o_1} = i_{i_2} = i_{b_2}$.

$$A_{I_1} = \frac{i_{o_1}}{i_i} = \frac{i_{b_2}}{i_i} = -\frac{R_E + R'}{R_E + R' + h_{ie_1}} h_{fe_1} \frac{R_{C1}}{R_{C1} + R_{i_2}}$$

where R_{i_2} is the input resistance of the second stage and given by

$$R_{i_2} = h_{ie_2} + (h_{fe_2+1})\,(R'||R_E)$$

Thus, open-loop no-load current gain A_i is given by

$$\boxed{A_i = \left.\frac{i_o}{i_i}\right|_{R_L=0} = A_{I_1} \cdot A_{i_2} = \frac{R_E + R'}{R_E + R' + h_{ie_1}} \frac{h_{fe_1} h_{fe_2} R_{C1}}{R_{C1} + R_{i_2}}}$$

Now, let us calculate the closed-loop amplifier parameters R_{if}, R_{of} and A_{if} using the current-series feedback formulas derived before.

$$\boxed{R_{if} = \frac{R_i}{1 + \beta A_I} = \frac{(R' + R_E)||h_{ie_1}}{1 + \dfrac{R_E}{R_E + R' + h_{ie_1}} \dfrac{h_{fe_1} h_{fe_2} R_{C1}}{R_{C1} + R_{i_2}}}}$$

$$\boxed{R_{of} = (1 + \beta A_{is})\, R_o = \left(1 + \frac{R_s}{R_s + R_i} \frac{R_E}{R' + R_E} A_i\right) \infty = \infty}$$

$$\boxed{A_{if} = \frac{A_i}{1 + \beta A_i} = \frac{\dfrac{R_E + R'}{R_E + R' + h_{ie_1}} \dfrac{h_{fe_1} h_{fe_2} R_{C1}}{R_{C1} + R_{i_2}}}{1 + \dfrac{R_E}{R_E + R' + h_{ie_1}} \dfrac{h_{fe_1} h_{fe_2} R_{C1}}{R_{C1} + R_{i_2}}} \approx 1 + \frac{R'}{R_E}}$$

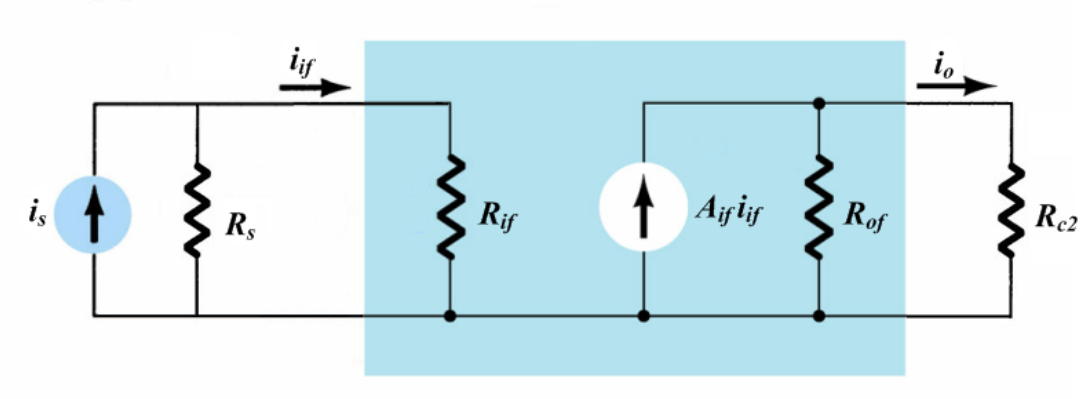


Figure 1.1.62: Equivalent closed-loop amplifier block diagram of the circuit given in Figure 1.1.59.

From the closed-loop amplifier diagram above, we can also find the overall closed-loop current gain A_{Isf}, as

$$\boxed{A_{Isf} = \frac{i_o}{i_s} = \frac{R_s}{R_s + R_{if}} A_{if} \frac{R_{of}}{R_{of} + R_{C2}}}$$

where $i_s = \dfrac{v_s}{R_s}$

Thus, overall closed-loop voltage gain A_{Vsf} will be given by

$$\boxed{A_{Vsf} = \frac{v_o}{v_s} = \frac{i_o R_{C2}}{i_s R_s} = \frac{R_{C2}}{R_s} A_{Isf}}$$

1.2 Differential Amplifiers

Differential amplifier circuits have 2 inputs and 2 outputs, as shown by the model below.

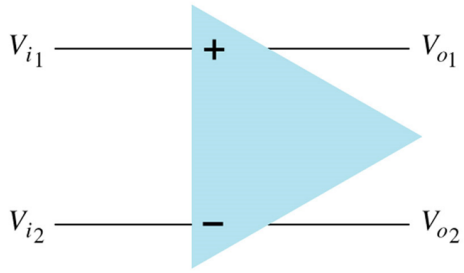


Figure 1.2.1: Differential amplifier model

Differential amplifiers are used to amplify the **difference** between the two inputs. Thus, differential amplifiers are **high gain** and **low noise** amplifiers.

Differential amplifier can be realized by using two BJTs by connecting their emitter terminals together, where inputs are given from the base terminals and outputs are taken from the collectors of the two transistors, as shown below.

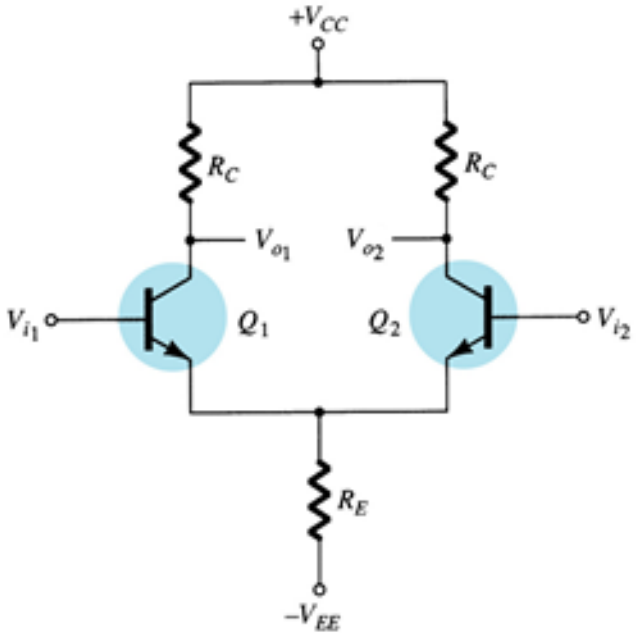


Figure 1.2.2: Differential amplifier with a common emitter resistance

It can be operated with a dual power supply: V_{CC} to $-V_{EE}$; or with a single supply: V_{CC} to GND.

1.2.0.1 Three Modes of Operation

There are three modes of operation for differential amplifiers:

1. **Single-ended mode**

- an input signal is applied to one of the inputs and the other input is grounded.

2. **Common-mode**

   - the **same** input signal is applied to both inputs.

3. **Differential-mode**

   - two **opposite polarity** input signals are applied to its inputs.

1.2.1 DC Biasing

Both inputs are **grounded** (no AC input) and we assume that both transistors are well matched ($Q_1 \equiv Q_2$).

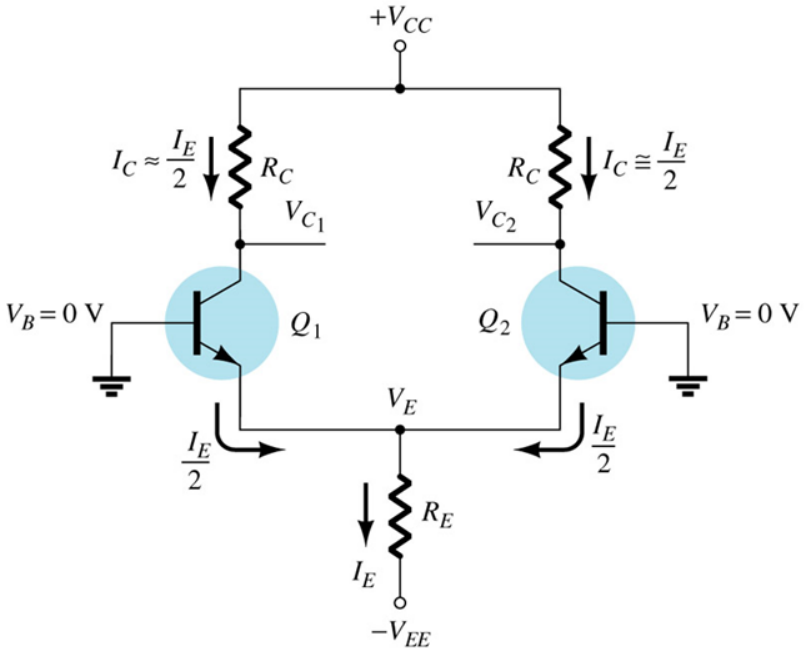


Figure 1.2.3: Differential amplifier DC biasing

$$V_{EQ} = 0 - V_{BE(ON)} = -V_{BE(ON)} \qquad \ldots (\text{as } V_{BE_1(ON)} = V_{BE_2(ON)}) \tag{1.2.1}$$

$$I_{EQ} = \frac{V_{EQ} - (-V_{EE})}{R_E} = \frac{V_{EE} - V_{BE(ON)}}{R_E} \tag{1.2.2}$$

$$I_{CQ} = I_{CQ_1} = I_{CQ_2} = \frac{I_{EQ}}{2} \qquad \ldots (\text{as } I_{BQ_1} = I_{BQ_2} \text{ and } \beta_1 = \beta_2 \gg 1) \tag{1.2.3}$$

We can now calculate the DC voltages around the circuit as follows

$$V_{CQ} = V_{CC} - I_{CQ} R_C \qquad \ldots V_{CQ_1} = V_{CQ_2} = V_{CQ} \tag{1.2.4}$$

$$V_{CEQ} = V_{CC} + V_{EE} - I_{CQ}\,(R_C + 2R_E) \qquad \ldots V_{CEQ_1} = V_{CEQ_2} = V_{CEQ} \tag{1.2.5}$$

Note that as $I_{BQ_1} = I_{BQ_2}$ and $\beta_1 = \beta_2$ (i.e., $h_{fe_1} = h_{fe_2}$),

$$h_{ie_1} = h_{ie_2} = h_{ie}. \tag{1.2.6}$$

1.2.2 Small-Signal Analysis

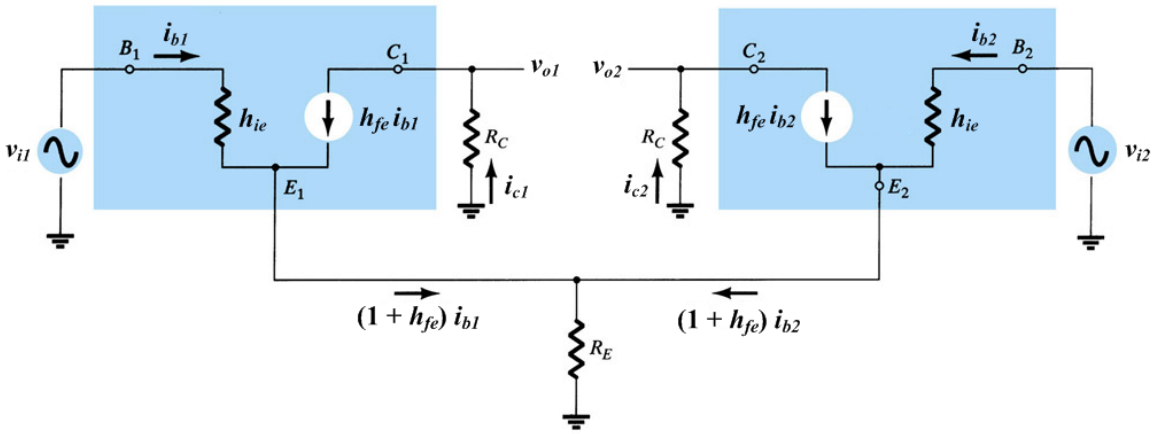


Figure 1.2.4: Differential amplifier small-signal analysis circuit.

Let us express the outputs in terms of the base currents assuming $h_{oe_1} = h_{oe_2} = 0$,

$$v_{o_1} = -h_{fe} i_{b_1} R_C \tag{1.2.7}$$

$$v_{o_2} = -h_{fe} i_{b_2} R_C. \tag{1.2.8}$$

Let us express the inputs in terms of the base currents where $v_e = [(h_{fe}+1)i_{b_1} + (h_{fe}+1)i_{b_2}]R_E$,

$$\begin{aligned} v_{i_1} &= v_{be_1} + v_e = h_{ie} i_{b_1} + [(h_{fe}+1)i_{b_1} + (h_{fe}+1)i_{b_2}]\, R_E \\ &= [h_{ie} + (h_{fe}+1)R_E]\, i_{b_1} + (h_{fe}+1)R_E i_{b_2} \end{aligned} \tag{1.2.9}$$

$$\begin{aligned} v_{i_2} &= v_{be_2} + v_e = h_{ie} i_{b_2} + [(h_{fe}+1)i_{b_1} + (h_{fe}+1)i_{b_2}]\, R_E \\ &= (h_{fe}+1)R_E i_{b_1} + [h_{ie} + (h_{fe}+1)R_E]\, i_{b_2} \end{aligned} \tag{1.2.10}$$

In order to obtain i_{b_1} and i_{b_2} in terms of let us first express (1.2.9) and (1.2.10) using matrices and take the inverse of the equation matrix (you can also obtain base currents using the classical variable **elimination method**)

$$\begin{bmatrix} v_{i_1} \\ v_{i_2} \end{bmatrix} = \begin{bmatrix} h_{ie} + (h_{fe}+1)R_E & (h_{fe}+1)R_E \\ (h_{fe}+1)R_E & h_{ie} + (h_{fe}+1)R_E \end{bmatrix} \begin{bmatrix} i_{b_1} \\ i_{b_2} \end{bmatrix} \tag{1.2.11}$$

Thus, base currents i_{b_1} and i_{b_2} are given by

$$\begin{bmatrix} i_{b_1} \\ i_{b_2} \end{bmatrix} = \frac{1}{h_{ie}\,[h_{ie} + 2(h_{fe}+1)R_E]} \begin{bmatrix} h_{ie} + (h_{fe}+1)R_E & -(h_{fe}+1)R_E \\ -(h_{fe}+1)R_E & h_{ie} + (h_{fe}+1)R_E \end{bmatrix} \begin{bmatrix} v_{i_1} \\ v_{i_2} \end{bmatrix}. \tag{1.2.12}$$

Hence,

$$i_{b_1} = \frac{[h_{ie} + (h_{fe}+1)R_E]\, v_{i_1} - (h_{fe}+1)R_E\, v_{i_2}}{h_{ie}\,[h_{ie} + 2(h_{fe}+1)R_E]} \tag{1.2.13}$$

$$i_{b_2} = \frac{[h_{ie} + (h_{fe}+1)R_E]\, v_{i_2} - (h_{fe}+1)R_E\, v_{i_1}}{h_{ie}\,[h_{ie} + 2(h_{fe}+1)R_E]}. \tag{1.2.14}$$

Finally, the output voltages are expressed in terms of the input voltages as follows,

$$v_{o_1} = -h_{fe}R_C\, \frac{[h_{ie} + (h_{fe}+1)R_E]\, v_{i_1} - (h_{fe}+1)R_E\, v_{i_2}}{h_{ie}\,[h_{ie} + 2(h_{fe}+1)R_E]} \tag{1.2.15}$$

$$v_{o_2} = -h_{fe}R_C\, \frac{[h_{ie} + (h_{fe}+1)R_E]\, v_{i_2} - (h_{fe}+1)R_E\, v_{i_1}}{h_{ie}\,[h_{ie} + 2(h_{fe}+1)R_E]}. \tag{1.2.16}$$

1.2.3 Single-Ended Mode Operation

In this mode a signal is connected to one input and the other is grounded, i.e., $v_{i_2} = 0$.

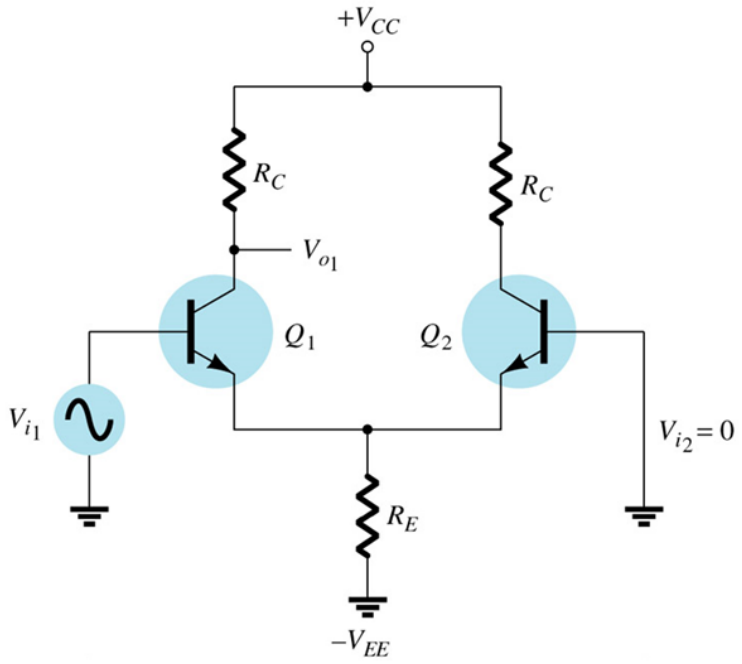


Figure 1.2.5: Single-ended differential amplifier.

By setting $v_{i_2} = 0$ in (1.2.15), we obtain

$$\boxed{A_v = \frac{v_{o_1}}{v_{i_1}} = \frac{-h_{fe}R_C\,[h_{ie} + (h_{fe}+1)R_E]}{[h_{ie} + 2(h_{fe}+1)R_E]\,h_{ie}} \cong \frac{-h_{fe}R_C}{2h_{ie}}} \tag{1.2.17}$$

Note that if take the output from the opposite collector (see (1.2.16)), the gain becomes positive,

$$\frac{v_{o_2}}{v_{i_1}} = \frac{h_{fe}R_C\,[(h_{fe}+1)R_E]}{[h_{ie} + 2(h_{fe}+1)R_E]\,h_{ie}} \cong \frac{h_{fe}R_C}{2h_{ie}} = -A_v. \tag{1.2.18}$$

- Input resistance of the single-ended mode is given as

$$R_{i_s} = \frac{v_{i_1}}{i_{b_1}} \tag{1.2.19}$$

$$= \frac{[h_{ie} + 2(h_{fe} + 1)R_E]\, h_{ie}}{h_{ie} + (h_{fe} + 1)R_E} \qquad \ldots \text{from (1.2.13)} \tag{1.2.20}$$

$$\cong 2h_{ie}.$$

Consequently, input resistance of the single-ended mode is given by

$$\boxed{R_{i_s} \cong 2h_{ie}.} \tag{1.2.21}$$

- Let us show the input and the two out-of-phase outputs in the figure below

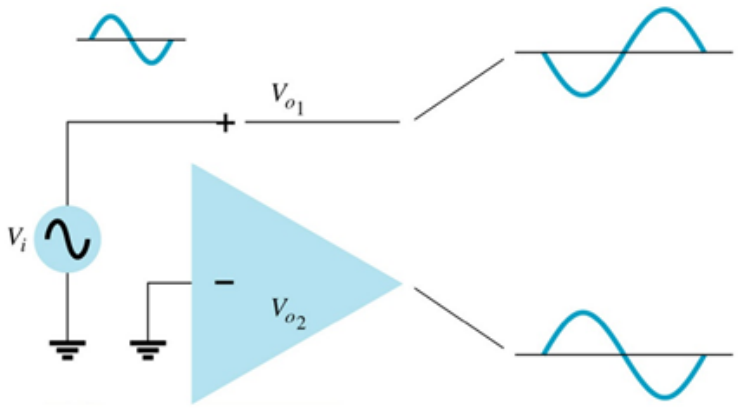


Figure 1.2.6: Two out-of-phase outputs of the single-ended differential amplifier.

- Now, let us show the input and the differential output in the figure below

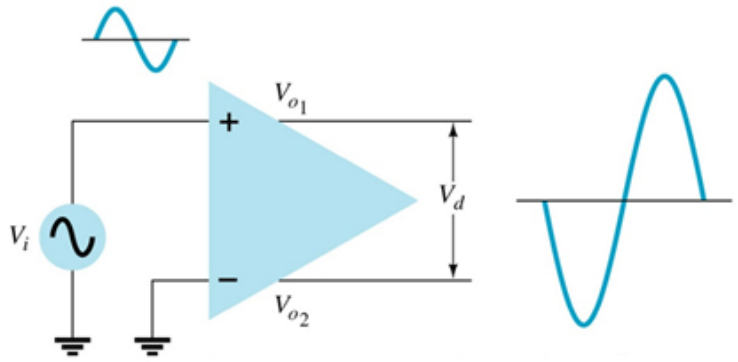


Figure 1.2.7: Differential output of the single-ended differential amplifier.

1.2.4 Common-Mode Operation

In this mode, the same signal is applied to both inputs, i.e., $v_{i_1} = v_{i_2} = v_i$. As the differential amplifier amplifies the difference between the inputs, common-mode gain should be quite small.

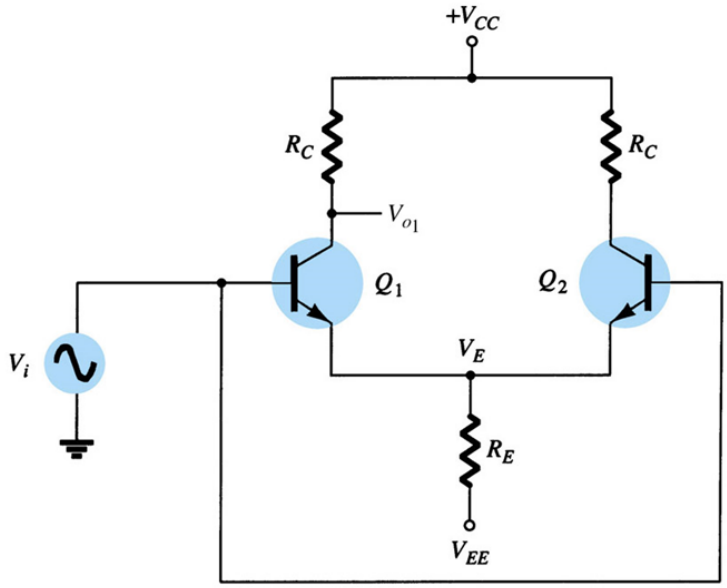


Figure 1.2.8: Common-mode differential amplifier.

By setting $v_{i_1} = v_{i_2} = v_i$ in (1.2.15) and (1.2.16), we obtain

$$\boxed{A_c = \frac{v_{o_1}}{v_i} = \frac{v_{o_2}}{v_i} = \frac{-h_{fe}R_C}{h_{ie} + 2(h_{fe}+1)R_E}} \tag{1.2.22}$$

- We see that input resistance of the common-mode, $R_{i_c} = \frac{v_i}{i_{b_1}+i_{b_2}}$, is

$$\boxed{R_{i_c} = \frac{h_{ie}}{2} + (h_{fe}+1)R_E \approx (h_{fe}+1)R_E} \tag{1.2.23}$$

- As we define the differential output as

$$v_o = v_{o_1} - v_{o_2},$$

if the differential amplifier is balanced, i.e.,

$$R_{C_1} = R_{C_2} = R_C,$$

then the **differential output common-mode gain** is **zero**,

$$\frac{v_o}{v_i} = \frac{v_{o_1} - v_{o_2}}{v_i} = \frac{-h_{fe}\left(R_{C_1} - R_{C_2}\right)}{h_{ie} + 2(h_{fe}+1)R_E} = \frac{-h_{fe}\left(R_C - R_C\right)}{h_{ie} + 2(h_{fe}+1)R_E} = 0. \tag{1.2.24}$$

1.2.5 Differential-Mode Operation

In this mode, two opposite polarity signals $v_{i_1} = -v_{i_2} = \frac{v_d}{2}$ are applied to the inputs

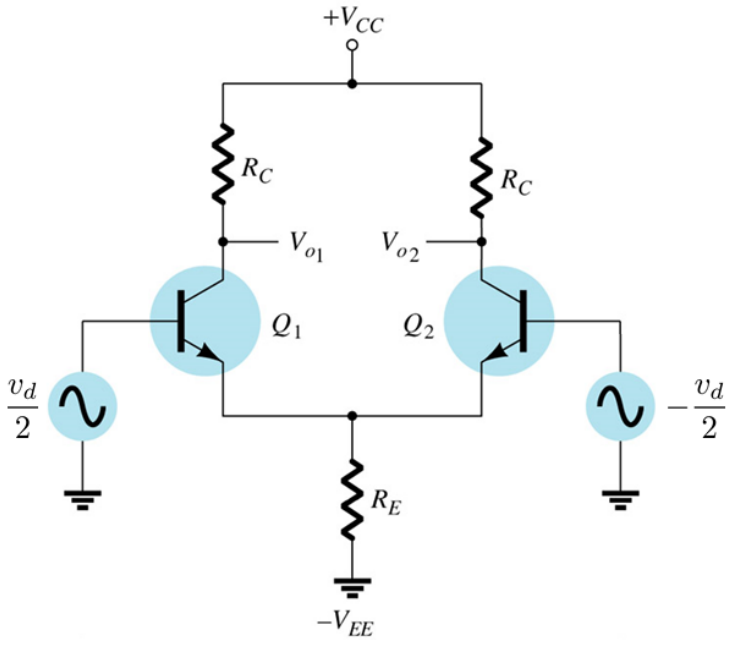


Figure 1.2.9: Differential-mode differential amplifier.

By setting $v_{i_1} = \frac{v_d}{2}$ and $v_{i_2} = -\frac{v_d}{2}$ in (1.2.15), we obtain

$$\boxed{A_d = \frac{v_{o_1}}{v_d} = \frac{-h_{fe}R_C}{2h_{ie}}} \tag{1.2.25}$$

Here, v_d is called the **differential input**, i.e.,

$$v_d = v_{i_1} - v_{i_2}.$$

- Note that if take the output from the opposite collector (see (1.2.16)), the gain becomes positive,

$$\frac{v_{o_2}}{v_d} = -\frac{v_{o_1}}{v_d} = \frac{h_{fe}R_C}{2h_{ie}}. \tag{1.2.26}$$

- We see that, input resistance of the differential-mode, $R_{i_d} = \frac{v_d}{i_{b_1}}$, is

$$\boxed{R_{i_d} = 2h_{ie}} \tag{1.2.27}$$

- As we define the differential output as

$$v_o = v_{o_1} - v_{o_2},$$

if the differential amplifier is balanced, i.e.,

$$R_{C_1} = R_{C_2} = R_C,$$

then the **differential output differential-mode gain** is **doubled**,

$$\frac{v_o}{v_d} = \frac{v_{o_1} - v_{o_2}}{v_d} = \frac{-h_{fe}\left(R_{C_1} + R_{C_2}\right)}{2h_{ie}} = \frac{-h_{fe}\left(2R_C\right)}{2h_{ie}} = 2A_d. \tag{1.2.28}$$

1.2.6 Linear Operation

- Let us represent the two input signals v_{i_1} and v_{i_2} in terms of their average $v_{\text{avg}} = \dfrac{v_{i_1} + v_{i_2}}{2}$ and difference $v_d = v_{i_1} - v_{i_2}$,

$$v_{i_1} = v_{\text{avg}} + \frac{v_d}{2} \tag{1.2.29}$$

$$v_{i_2} = v_{\text{avg}} - \frac{v_d}{2} \tag{1.2.30}$$

- If the system is linear then we can write the two outputs v_{o_1} and v_{o_2} as follows

$$\boxed{v_{o_1} = A_c\, v_{\text{avg}} + A_d\, v_d} \tag{1.2.31}$$

$$\boxed{v_{o_2} = A_c\, v_{\text{avg}} - A_d\, v_d} \tag{1.2.32}$$

- Similarly, the differential output v_o of a balanced differential amplifier becomes

$$v_o = v_{o_1} - v_{o_2} = 2A_d v_d \tag{1.2.33}$$

NOTE: Differential amplifier with a common emitter resistance (see Figure 1.2.2) can always be considered to be **linear**.

1.2.7 Common-Mode Rejection (Noise Rejection)

In common-mode, the signal common to both inputs will have a low gain (A_c).

In differential-mode (single-ended or double-ended), any signal that is common to both inputs will have a low gain. In differential-mode, any signal that is common to both inputs is noise.

The ability of the amplifier to have a low common-mode gain, i.e., not amplify signals that are common to both inputs, is called **Common-Mode Rejection**.

- Then, the Common-Mode Rejection Ratio (CMRR) is given by

$$\text{CMRR} = \left|\frac{A_d}{A_c}\right| \tag{1.2.34}$$

$$= \frac{h_{ie} + 2(h_{fe} + 1)R_E}{2h_{ie}} \tag{1.2.35}$$

- CMRR can be also represented in dBs, i.e.,

$$\text{CMRR} = 20 \log_{10} \left|\frac{A_d}{A_c}\right| \tag{1.2.36}$$

- To improve common-mode rejection:
  - A_d must increase
  - A_c must decrease, i.e., R_E must increase.
- One method is to increase the value of R_E by replacing it with a **constant-current source** circuit.

1.2.8 Differential Amplifier with a Constant-Current Source

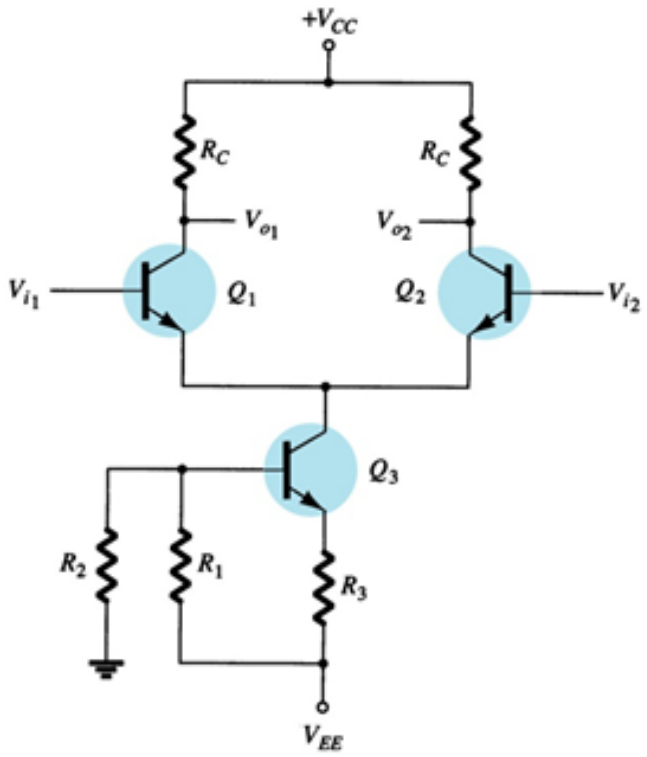


Figure 1.2.10: Differential amplifier with a constant-current source.

This increases the AC impedance for R_E.

Constant-current sources can be built using FETs, BJTs and a combination of these devices.

1.2.8.1 Constant-Current Source Circuits

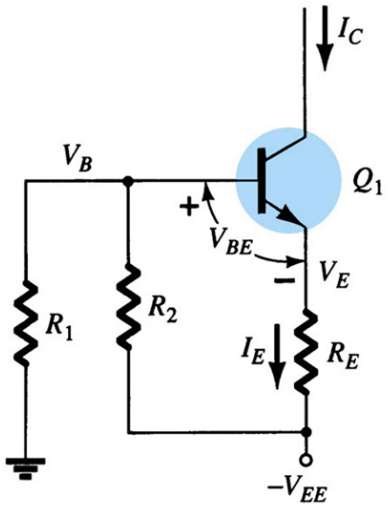


Figure 1.2.11: A BJT constant-current source with resistors.

Collector current I_C is independent of the load circuit connected to the collector and given by

$$I_C \cong I_E \tag{1.2.37}$$

$$= \frac{V_B - V_{BE(ON)} - (-V_{EE})}{R_E} \tag{1.2.38}$$

$$\approx \frac{\dfrac{R_2}{R_1 + R_2} V_{EE} - V_{BE(ON)}}{R_E} \qquad \ldots \text{where } (I_{R_1} \cong I_{R_2}) \gg I_B. \tag{1.2.39}$$

Current source with a Zener diode

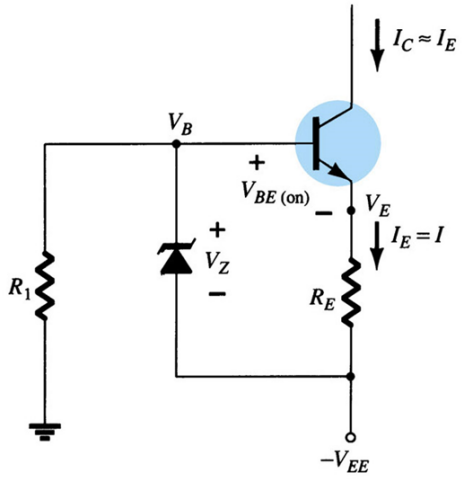


Figure 1.2.12: A BJT constant-current source with a Zener diode.

Collector current I_C is independent of the load circuit connected to the collector and given by

$$I_C \cong I_E \tag{1.2.40}$$

$$= \frac{V_Z - V_{BE(ON)}}{R_E}. \tag{1.2.41}$$

Current Mirror

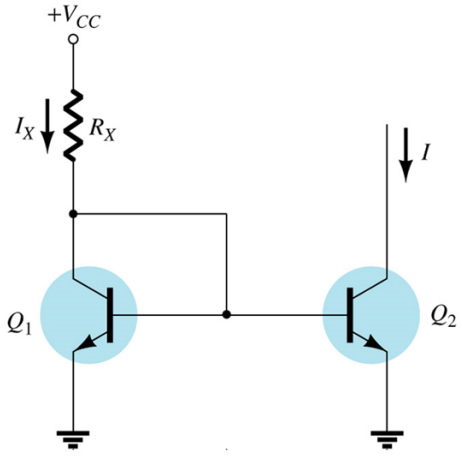


Figure 1.2.13: A current-mirror constant-current source.

Current-source current I is given by

$$I = I_{C_2} \tag{1.2.42}$$
$$= I_{C_1} \qquad \ldots \text{as } Q_1 \equiv Q_2, \text{ i.e., } V_{BE_1(ON)} = V_{BE_2(ON)} \text{ and } \beta_1 = \beta_2, \tag{1.2.43}$$
$$\cong I_X \qquad \ldots \text{as } I_{C_1} \gg 2I_B \text{ where } I_X = I_{C_1} + 2I_B, \tag{1.2.44}$$
$$= \frac{V_{CC} - V_{BE(ON)}}{R_X}. \tag{1.2.45}$$

Current-mirror circuits are used to provide constant current in integrated circuits.

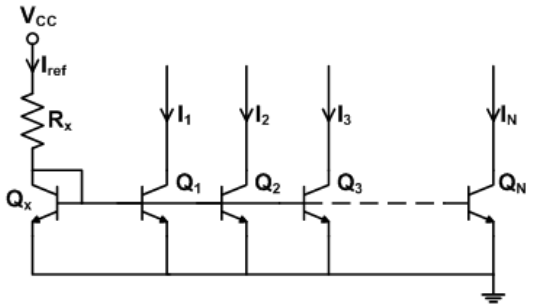


Figure 1.2.14: Identical current-mirror constant-current sources ($I_1 = I_2 = \cdots = I_N$).

Identical current-mirror constant-current sources ($I_1 = I_2 = \cdots = I_N$) can be made as shown in Figure 1.2.14.

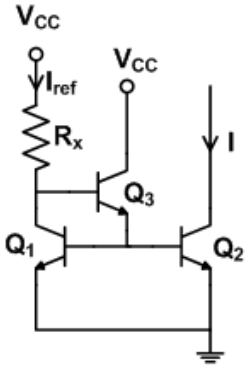


Figure 1.2.15: An improved current-mirror constant-current source.

Homework 1.1: Consider Figure 1.2.15 above and find I.

1.2.8.2 Analysis of Differential Amplifier with a Constant-Current Source

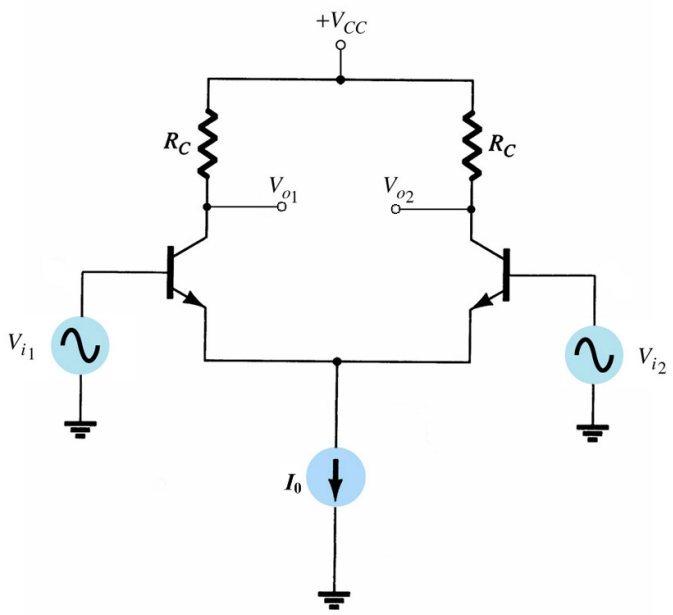


Figure 1.2.16: Differential amplifier with a constant-current source.

Let us analyse the differential amplifier with a constant-current source shown in Figure 1.2.16. Note that sum of the emitter currents is constant due to the constant-current source, i.e.,

$$i_{E_1} + i_{E_2} = I_0 \tag{1.2.46}$$

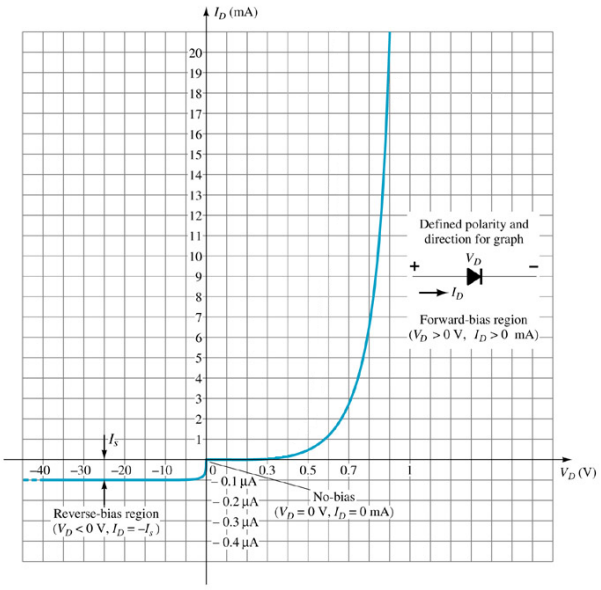


Figure 1.2.17: Diode IV characteristics.

Before continuing any further, let us remember the *pn*-junction diode characteristic equation,

$$I_D = I_S \left(e^{V_D/\gamma} - 1 \right), \tag{1.2.47}$$

where I_S is the saturation current and γ is the thermo-equivalent potential given by $\gamma = \frac{kT}{q}$, where k is the Boltzman constant, T is the temperature in Kelvins and q is the Coulomb charge. At the room temperature, $T = 300K$ (i.e., $T = 27°C$), thermo-equivalent potential γ is given by

$$\gamma = 26\,\text{mV}. \tag{1.2.48}$$

Under forward bias, the diode current I_D simplifies to

$$I_D \cong I_S\, e^{V_D/\gamma} \tag{1.2.49}$$

In a BJT, as BE-junction is as pn-junction, under forward bias we can write down the emitter currents of a differential amplifier as follows

$$i_{E_1} = I_{ES}\, e^{v_{BE_1}/\gamma} \tag{1.2.50}$$

$$i_{E_2} = I_{ES}\, e^{v_{BE_2}/\gamma} \qquad \ldots\text{Note that } Q_1 \equiv Q_2. \tag{1.2.51}$$

Let us express the ratio of constant-current source current I_0 to the emitter current I_{E_1} using (1.2.46) as follows

$$\frac{I_0}{i_{E_1}} = 1 + \frac{i_{E_2}}{i_{E_1}} \tag{1.2.52}$$

$$= 1 + \frac{I_{ES}\, e^{v_{BE_2}/\gamma}}{I_{ES}\, e^{v_{BE_1}/\gamma}} \tag{1.2.53}$$

$$= 1 + e^{\left(v_{BE_2} - v_{BE_1}\right)/\gamma} \tag{1.2.54}$$

$$= 1 + e^{\left(v_{i_2} - v_{i_1}\right)/\gamma} \tag{1.2.55}$$

where $v_{BE_1} = V_{BE(ON)} + v_{i1}$ and $v_{BE_2} = V_{BE(ON)} + v_{i2}$.

We can now express the inverse ratios $\frac{i_{E_1}}{I_0}$ and $\frac{i_{E_2}}{I_0}$ as

$$\boxed{\frac{i_{E_1}}{I_0} = \frac{1}{1 + e^{\left(v_{i_2} - v_{i_1}\right)/\gamma}}} \tag{1.2.56}$$

and

$$\boxed{\frac{i_{E_2}}{I_0} = \frac{1}{1 + e^{\left(v_{i_1} - v_{i_2}\right)/\gamma}}} \tag{1.2.57}$$

respectively. Note that

$$\boxed{\frac{i_{E_1}}{I_0} + \frac{i_{E_2}}{I_0} = 1}. \tag{1.2.58}$$

As the collector currents are (almost) equal to the emitter currents, we can plot these ratios as follows

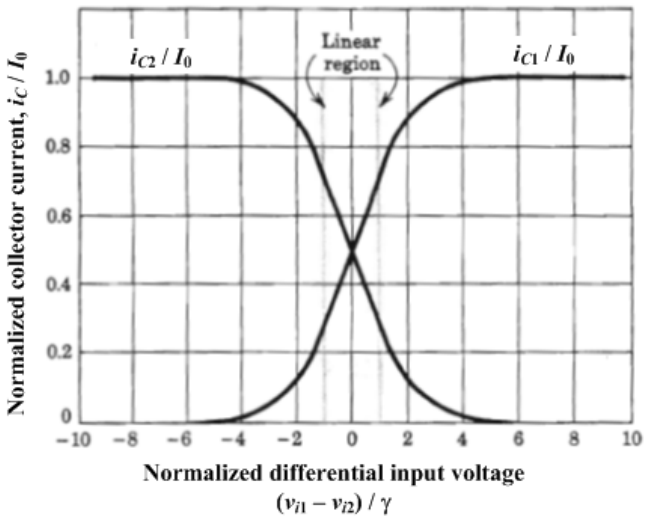


Figure 1.2.18: Ratio of the collector currents to the constant-current source.

From the figure Figure 1.2.18, we see that the linear region resides in between $\pm(1.15\,\gamma)$. Thus, if

$$\boxed{|v_{i_1} - v_{i_2}| = |v_d| \leq 30\,\text{mV}} \tag{1.2.59}$$

then, differential amplifier with constant-current source is in the linear region and the following linear operations will hold,

$$\begin{aligned} v_{o_1} &= A_c\, v_{\text{avg}} + A_d\, v_d \\ v_{o_2} &= A_c\, v_{\text{avg}} - A_d\, v_d. \end{aligned}$$

Example 1.7: For the circuit in Figure 1.2.19 below find $v_o = v_{o_1} - v_{o_2}$ for

$$v_{i_1} = 0\,\text{V} \text{ and } v_{i_2} = 58.5\,\text{mV}$$

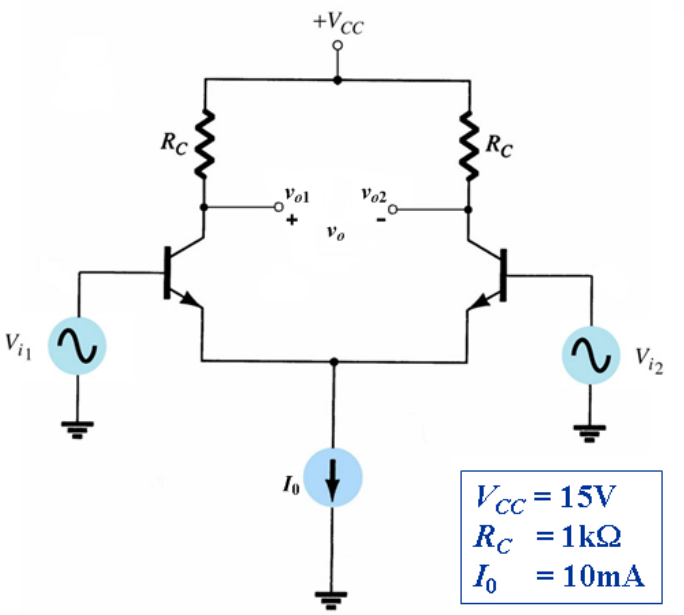


Figure 1.2.19: A differential amplifier with constant-current source (a differential amplifier example)

Solution: Let us first calculate the $\frac{i_{C_1}}{I_0}$ ratio

$$\begin{aligned}\frac{i_{C_1}}{I_0} &= \frac{1}{1+e^{(v_{i_2}-v_{i_1})/\gamma}} \\ &= \frac{1}{1+e^{(58.5m-0)/26m}} \\ &= \frac{1}{1+e^{2.25}} \\ &\cong 0.095.\end{aligned}$$

Thus, i_{C_1} and i_{C_2} are given by

$$\begin{aligned}i_{C_1} &= \frac{i_{C_1}}{I_0} I_0 = (0.095)(10m) = 0.95\,\text{mA}, \\ i_{C_2} &= I_0 - I_{C_1} = 10m - 0.95m = 9.05\,\text{mA}.\end{aligned}$$

Consequently, v_o is given by

$$\begin{aligned}v_o &= (V_{CC} - i_{C_1}R_C) - (V_{CC} - i_{C_2}R_C) \\ &= (i_{C_2} - i_{C_1})\,R_C \\ &= (9.05m - 0.95m)\,1k \\ &= \underline{8.1\,\text{V}.}\end{aligned}$$

1.2.9 Differential Amplifier Parameters

- Input offset voltage : V_{IO}

- Input voltage difference $(V_{B_1} - V_{B_2})$ which makes $v_o = 0\,\text{V}$.
  - Due to the $V_{BE(ON)}$ difference of the two BJTs, i.e., when $V_{BE_1(ON)} \neq V_{BE_2(ON)}$.

- Input offset current : I_{IO}
  - Input current difference $(I_{B_1} - I_{B_2})$ which makes $v_o = 0\,\text{V}$.
    - Due to the h_{fe} difference of the two BJTs, i.e., when $h_{fe_1} \neq h_{fe_2}$.

1.2.10 Improvements

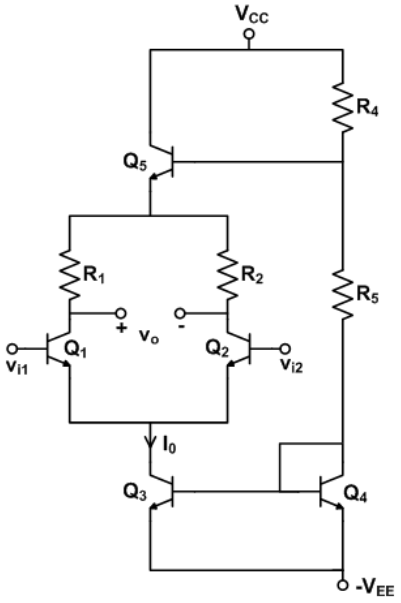


Figure 1.2.20: Differential amplifier with a transistor at the collector.

The differential amplifier in Figure 1.2.14 has an improved output voltage swing.

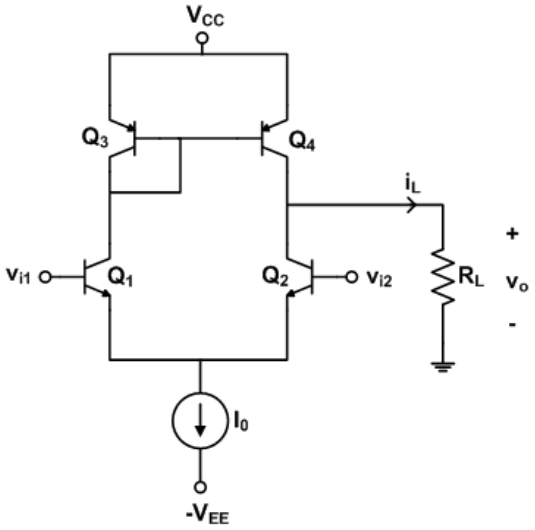


Figure 1.2.21: Differential amplifier with a current mirror at the collector.

Homework 1.2: Considering the circuit in Figure 1.2.21 above, find the common-mode gain A_c and differential mode gain A_d during linear operation.

HINT: While performing small-signal analysis, consider $R_E = \infty$ and employ current-mirroring. You may start from DC analysis to understand the effect of the current mirror.

1.2.11 FET Differential Amplifier

Differential amplifier can also be realized by using two FETs by connecting their source terminals together, where inputs are given from the gate terminals and outputs are taken from the drains of the two transistors, as shown below.

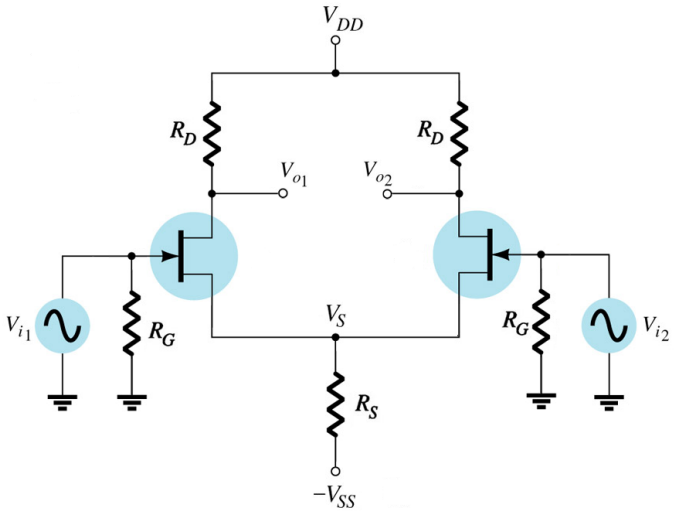


Figure 1.2.22: FET differential amplifier with a common source resistance.

1.2.11.1 Small-Signal Analysis

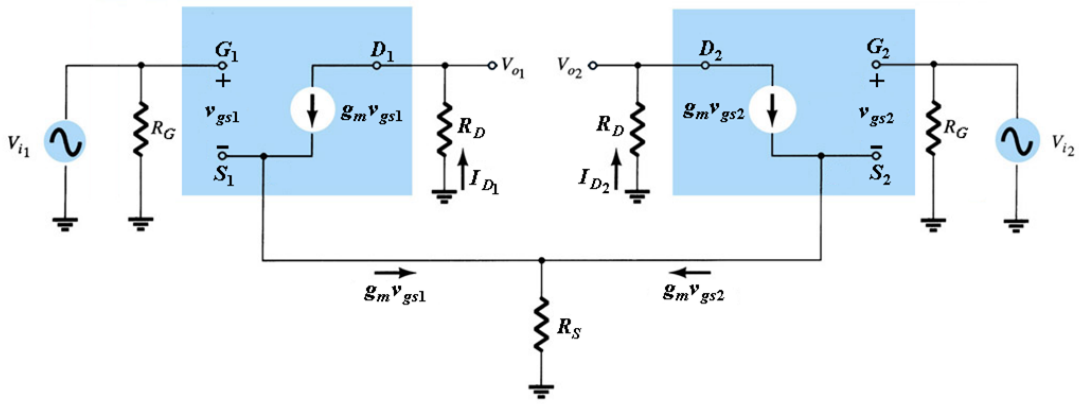


Figure 1.2.23: FET differential amplifier small-signal analysis circuit.

Let us express the outputs in terms of the base currents assuming $r_{ds_1} = r_{ds_2} = \infty$,

$$v_{o_1} = -g_m v_{gs_1} R_D \tag{1.2.60}$$

$$v_{o_2} = -g_m v_{gs_2} R_D. \qquad \ldots \text{As } Q_1 \equiv Q_2 \text{ and } I_{DQ_1} = I_{DQ_2},\ g_m = g_{m_1} = g_{m_2}. \tag{1.2.61}$$

Let us express the inputs in terms of the gate-to-source voltages using matrices, where $v_s = [g_m v_{gs_1} + g_m v_{gs_2}]R_S$

$$\begin{bmatrix} v_{i_1} \\ v_{i_2} \end{bmatrix} = \begin{bmatrix} 1 + g_m R_S & g_m R_S \\ g_m R_S & 1 + g_m R_S \end{bmatrix} \begin{bmatrix} v_{gs_1} \\ v_{gs_2} \end{bmatrix} \tag{1.2.62}$$

Thus, employing the linear algebra principles voltages we obtain v_{gs_1} and v_{gs_2} as the following

$$\begin{bmatrix} v_{gs_1} \\ v_{gs_2} \end{bmatrix} = \frac{1}{1 + 2g_m R_S} \begin{bmatrix} 1 + g_m R_S & -g_m R_S \\ -g_m R_S & 1 + g_m R_S \end{bmatrix} \begin{bmatrix} v_{i_1} \\ v_{i_2} \end{bmatrix}. \tag{1.2.63}$$

- Hence, by setting $v_{i_1} = v_{i_2} = v_i$ in (1.2.63) and employing (1.2.60) and (1.2.61), we obtain the **common-mode gain** as

$$\boxed{A_c = \frac{v_{o_1}}{v_i} = \frac{v_{o_2}}{v_i} = \frac{-g_m R_D}{1 + 2g_m R_S}}. \tag{1.2.64}$$

- Similarly, by setting $v_{i_1} = \frac{v_d}{2}$ and $v_{i_2} = -\frac{v_d}{2}$ in (1.2.63) and employing (1.2.60) and (1.2.61), we obtain the **differential-mode gain** as

$$\boxed{A_d = \frac{v_{o_1}}{v_d} = \frac{-g_m R_D}{2}} \tag{1.2.65}$$

- NOTE: FET differential amplifier with a common source resistance (see Figure 1.2.22) can be always considered to be **linear**. Thus, the linear operation holds:

$$v_{o_1} = A_c\, v_{\text{avg}} + A_d\, v_d$$
$$v_{o_2} = A_c\, v_{\text{avg}} - A_d\, v_d.$$

1.2.12 Uses of Differential Amplifiers

1. Gain amplifiers in operational amplifiers
   - Due to high voltage gain
2. Comparators
   - Due to high sensitivity to the differential input, e.g., measurement circuit below

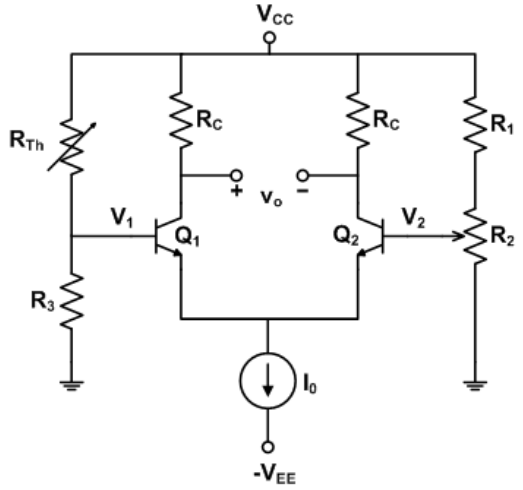


Figure 1.2.24: A differential amplifier measurement circuit

Here, R_{Th} signifies a **thermistor** whose resistance varies with temperature. Note that, the output is zero, i.e., $v_o = 0\,\text{V}$, only when $V_1 = V_2$.

1.2.13 Examples

Example 1.8: For the circuit below,

i. Calculate the value of R_C in order to make $v_o = 0\,\text{V}$ when $v_i = 0\,\text{V}$.

ii. Find v_o when $v_i = 1\,\text{mV}\sin(\omega t)$.

$$\boxed{h_{fe} = h_{FE} = 100, \alpha = 1, V_{BE(ON)} = 0.6\,\text{V}}$$

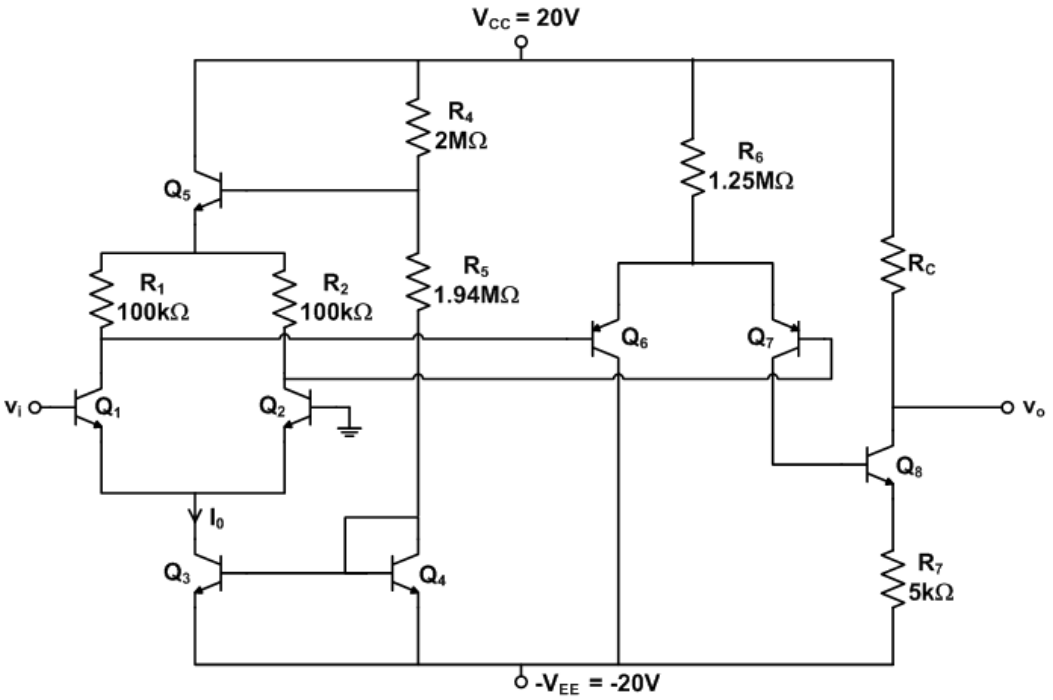


Figure 1.2.25: Differential amplifier circuit for Example 1.8.

Solution: i. Let us first calculate the value of the constant-current source I_0

$$\begin{aligned} I_0 &\cong \frac{V_{CC} - V_{BE(ON)} - (-V_{EE})}{R_4 + R_5} \qquad \ldots \text{ignoring } I_{B_5},\ I_{B_4} \text{ and } I_{B_3} \\ &= \frac{20 - 0.6 - (-20)}{2M + 1.94M} \\ &= 10\,\mu\text{A}. \end{aligned}$$

Thus, $I_{CQ_1} = I_{CQ_2} = \frac{I_0}{2} = \frac{10\mu}{2} = 5\,\mu\text{A}$.

In order to find I_{R6}, we need to write a KVL equation for the (R_6, R_1, R_4)-loop

$$V_{CC} - R_6 I_{R6} - V_{BE_6(ON)} + R_1 I_{R1} + V_{BE_3(ON)} + R_4 I_{R4} = V_{CC}$$

Thus I_{R6} is given by

$$\begin{aligned} I_{R6} &= \frac{R_1 I_{R1} + R_4 I_{R4}}{R_6} \\ &= \frac{(0.1M)(5\mu) + (2M)(10\mu)}{1.25M} \qquad \ldots I_{R4} \cong I_0 = 10\,\mu\text{A} \\ &= 16.4\,\mu\text{A}. \end{aligned}$$

Thus, $I_{CQ_6} = I_{CQ_7} = \frac{I_{R6}}{2} = \frac{16.4\mu}{2} = 8.2\,\mu\text{A}$.

Hence, $I_{BQ_8} = I_{CQ_7} = 8.2\,\mu\text{A}$.

$I_{CQ_8} = h_{FE} I_{BQ_8} = (100)(8.2\mu) = 0.82\,\text{mA}$.

Consequently, R_C is given by

$$\begin{aligned} R_C &= \frac{V_{CC} - v_o}{I_{CQ_8}} \\ &= \frac{20 - 0}{0.82m} \\ &= 24.39\,\text{k}\Omega. \end{aligned}$$

ii. First stage differential amplifier (with a constant-current source) is in the linear mode (as $v_d = 1\,\text{mV} < 30\,\text{mV}$), so let us calculate the h_{ie} values for the relevant transistors and the input resistance R_{i_8} of the last stage as $R_{C_7} = R_{i_8}$

$$\begin{aligned} h_{ie_1} = h_{ie_2} = h_{fe}\frac{\gamma}{I_{CQ_1}} &= 100\frac{25m}{5\mu} = 500\,\text{k}\Omega, \\ h_{ie_6} = h_{ie_7} = h_{fe}\frac{\gamma}{I_{CQ_7}} &= 100\frac{25m}{8.2\mu} = 305\,\text{k}\Omega, \\ h_{ie_8} = h_{fe}\frac{\gamma}{I_{CQ_8}} &= 100\frac{25m}{0.82m} = 3.05\,\text{k}\Omega \\ R_{C_7} = R_{i_8} = h_{ie_8} + (h_{fe} + 1)R_7 &= 3.05k + (101)(5k) = 508.05\,\text{k}\Omega. \end{aligned}$$

Linear-mode differential output of the first stage, $(v_{C_2} - v_{C_1})$, is given by

$$\begin{aligned} v_{C_2} - v_{C_1} = \frac{h_{fe} 2R_C || 2h_{ie_6}}{2h_{ie_1}}\, v_i &= \frac{h_{fe} R_C || h_{ie_6}}{h_{ie_1}}\, v_i \\ &= \frac{(100)(100k||305k)}{500k}(1m) \\ &= 0.015\,\text{V}. \end{aligned}$$

Output of the second stage, v_{C_7}, is given by

$$\begin{aligned} v_{C_7} &= \frac{-h_{fe} R_{C_7}}{2h_{ie_7}}\,(v_{B_7} - v_{B_6}) \\ &= \frac{-(100)(508.05k)}{(2)(305k)}(0.015) \\ &= -1.25\,\text{V}. \end{aligned}$$

Finally output v_o is given by,

$$\begin{aligned} v_o &= \frac{-h_{fe}R_C}{h_{ie_8} + (h_{fe}+1)R_7} v_{C_7} \qquad \ldots v_o \cong -\frac{R_C}{R_7} v_{C_7} \\ &= \frac{-(100)(24.39k)}{508.05k}(-1.67) \\ &= \underline{6\,\text{V}\sin(\omega t)}. \end{aligned}$$

Example 1.9: For the circuit below, (HINT: Use forward bias diode equation for diodes)

i. Calculate the value of R in order to make $v_o = 0\,\text{V}$ when $v_i = 0\,\text{V}$.

ii. Find v_o when $v_i = 20\,\text{mV}\sin(\omega t)$.

$$\boxed{h_{fe} = h_{FE} = 20, \alpha = 1, V_{BE(ON)} = 0.6\,\text{V}, \gamma = 25\,\text{mV}}$$

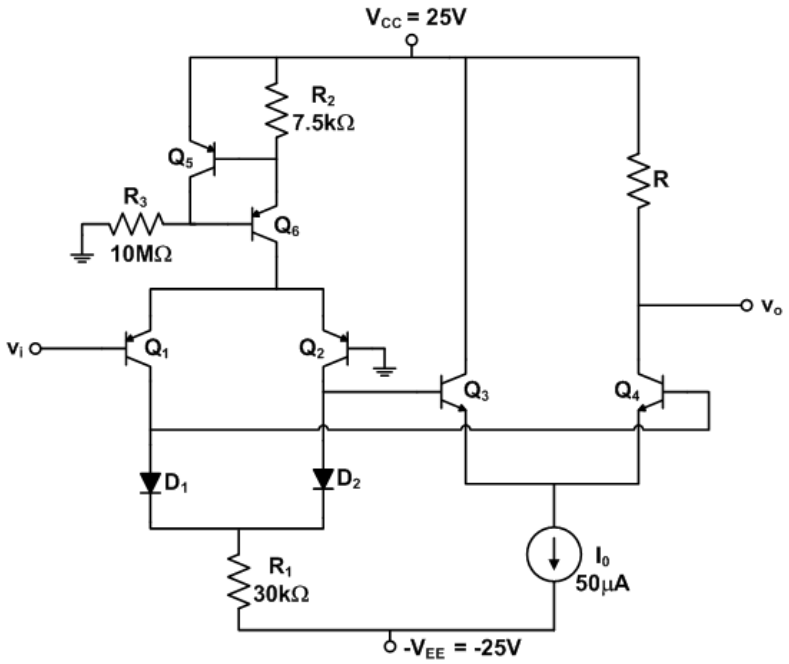


Figure 1.2.26: Differential amplifier circuit for Example 1.9.

Example 1.10: For the circuit below, calculate the value of R_2/R_1 in order to make $v_o = 0\,\text{V}$ when $v_i = 0\,\text{V}$.

$$\boxed{h_{fe} = h_{FE} = 100, \alpha = 1, V_{BE(ON)} = 0.6\,\text{V}}$$

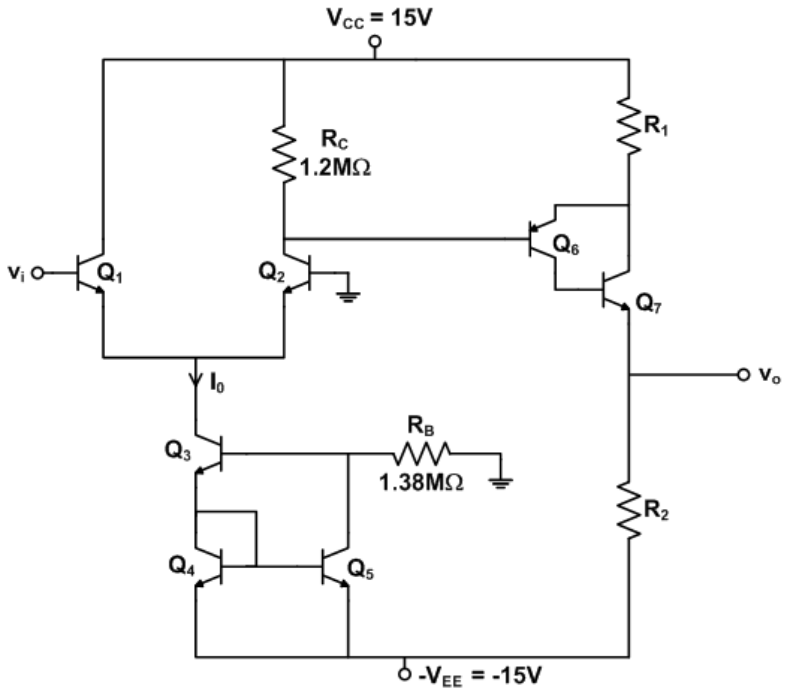


Figure 1.2.27: Differential amplifier circuit for Example 1.10.

1.3 Operational Amplifiers

Operational amplifier or op-amp, is a **very high gain** differential amplifier with a **high input impedance** (typically a few mega ohms) and **low output impedance** (less than 100 ohms).

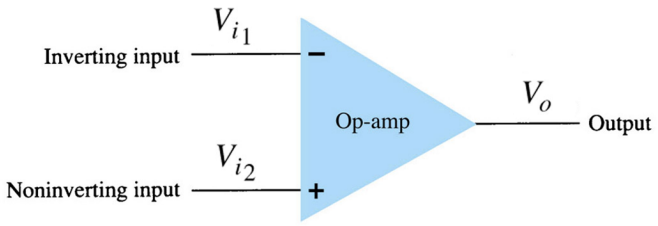


Figure 1.3.1: Operational amplifier block diagram

Note the op-amp has two inputs and one output, and op-amp amplifier model is shownin Figure 1.3.2 below.

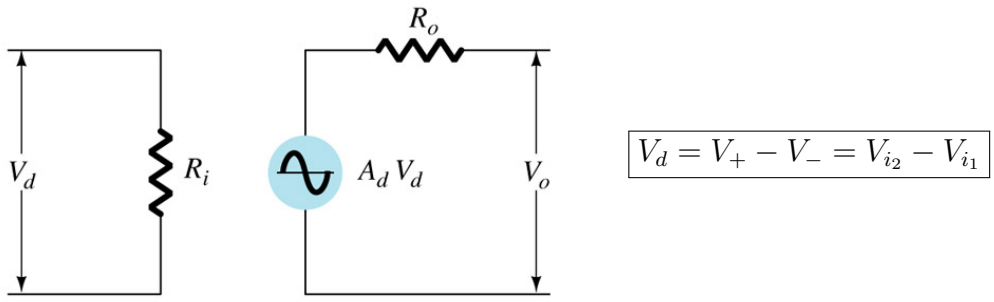


Figure 1.3.2: Operational amplifier model

1.3.1 Ideal Op-Amp Properties

1. Infinite Input Resistance: $R_i = \infty$
2. Zero Output Resistance: $R_o = 0$
3. Infinite Voltage Gain: $A_d = \infty$
4. Infinite Bandwidth: $BW = \infty$
5. Infinite output current
6. Perfect Balance, i.e., $v_o = 0$ when $v_{i_2} = v_{i_1}$
7. Above characteristics do not drift with temperature

1.3.2 MC1530 Operational Amplifier

Let us perform DC and AC analysis on the electronic circuit of the MC1530 op-amp shown below.

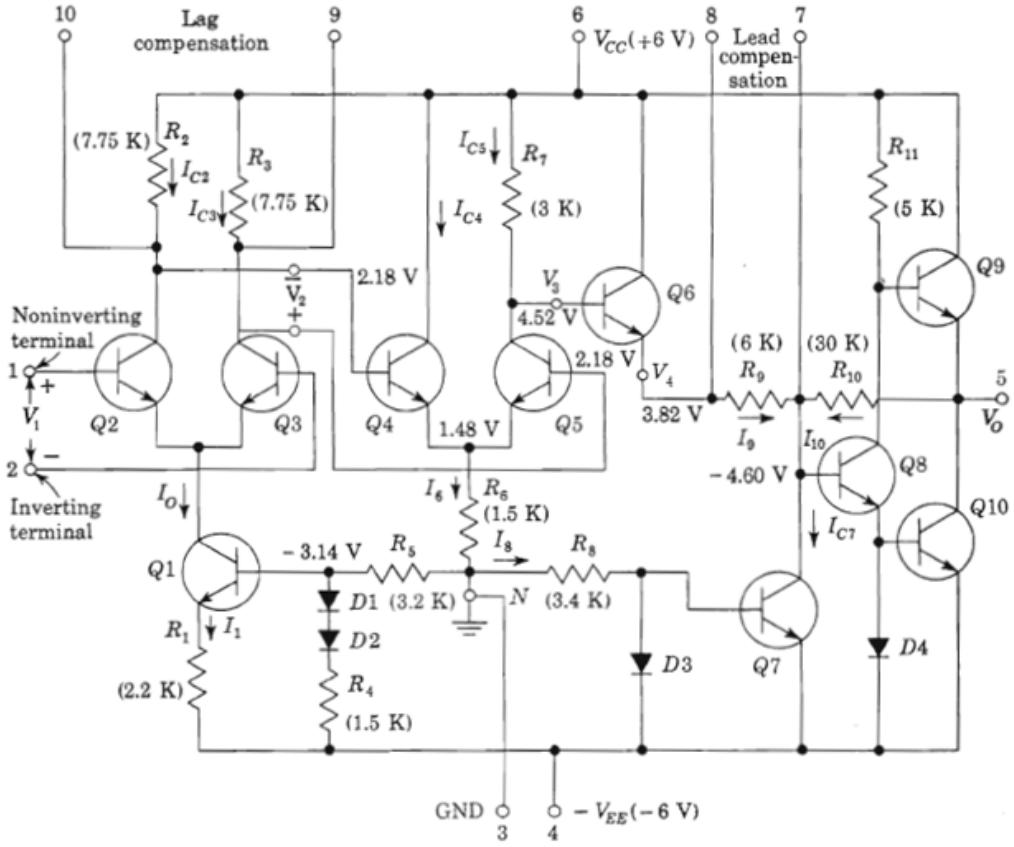


Figure 1.3.3: Electronic circuit of the MC1530 op-amp

Amplifier stages in Figure 1.3.3 can be identified as shown in Figure 1.3.4 below.

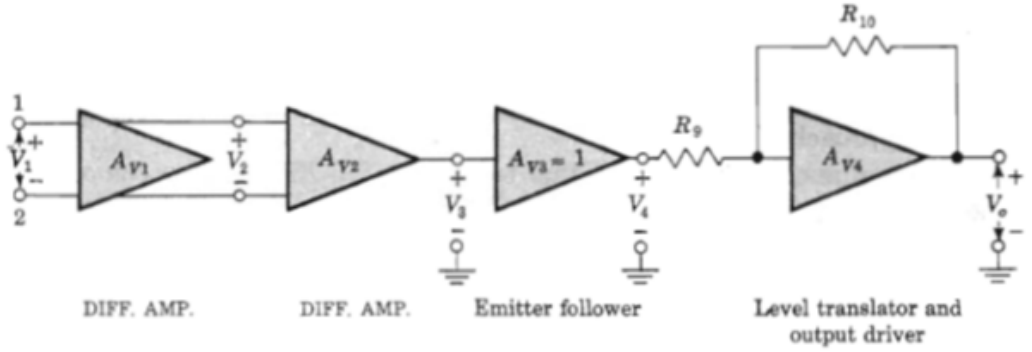


Figure 1.3.4: Block diagram of the MC1530 electronic circuit in Figure 1.3.3

1.3.2.1 DC Analysis

Let us perform DC analysis calculations on the MC1530 opamp internal circuitry.

$$\boxed{h_{fe} = h_{FE} = 100, \alpha = 1, V_{BE(ON)} = V_{D(ON)} = 0.7\,\text{V}}$$

$$V_{B_1} \cong \left(-V_{EE} + 2V_{D(ON)}\right) \frac{R_5}{R_4 + R_5} = -3.14\,\text{V}$$

$$I_0 \cong I_1 = \frac{V_{EE} + V_{B_1} - V_{BE(ON)}}{R_1} = 0.99\,\text{mA}$$

$$I_{C_2} = I_{C_3} \cong \frac{I_0}{2} = 0.495\,\text{mA}$$

$$V_{B_4} \cong V_{CC} - I_{C_2} R_2 = 2.18\,\text{V}$$

$$I_6 = \frac{V_{E_4}}{R_6} = \frac{V_{B_4} - V_{BE(ON)}}{R_6} = 0.986\,\text{mA}$$

$$I_{C_5} \cong \frac{I_6}{2} = 0.493\,\text{mA}$$

$$V_3 \cong V_{CC} - I_{C_5} R_7 = 4.52\,\text{V}$$

$$\boxed{V_4 = V_3 - V_{BE(ON)} = 3.82\,\text{V}}$$

$$\boxed{I_8 \cong I_{C_7} = \frac{V_{EE} - V_{D_3(ON)}}{R_8} = 1.56\,\text{mA}}$$

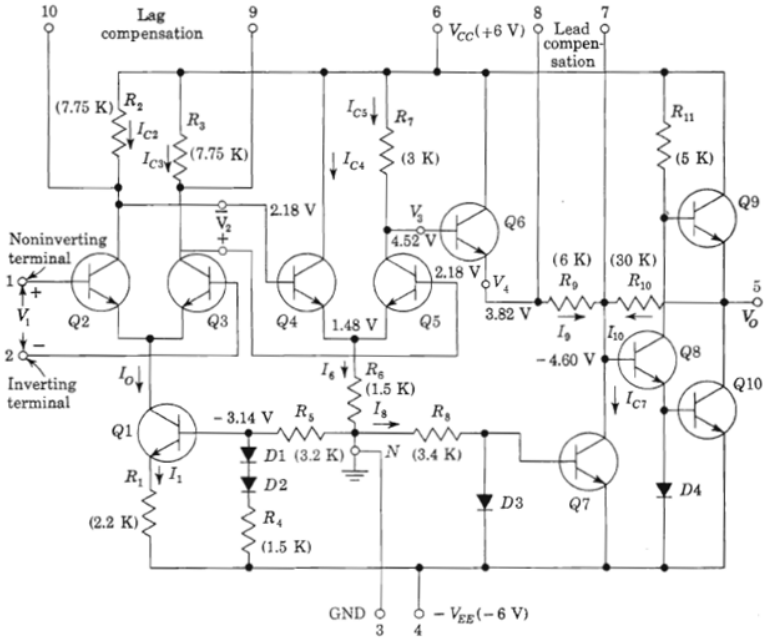


Figure 1.3.5: MC1530 DC analysis calculations - 1

Let us continue with the DC calculations on the output stage consisting of Q_8, Q_9 and Q_{10} transistors

$$V_{B_8} = -V_{EE} + 2V_{BE(ON)} = -4.6\,\text{V}$$

$$I_9 = \frac{V_4 - V_{B_8}}{R_9} = 1.4\,\text{mA}$$

$$I_{10} = I_{C_7} + I_{B_8} - I_9 \cong I_{C_7} - I_9 = 0.16\,\text{mA}$$

$$\boxed{V_o = V_{B_8} + I_{10} R_{10} = 200\,\text{mV} \cong 0\,\text{V}.}$$

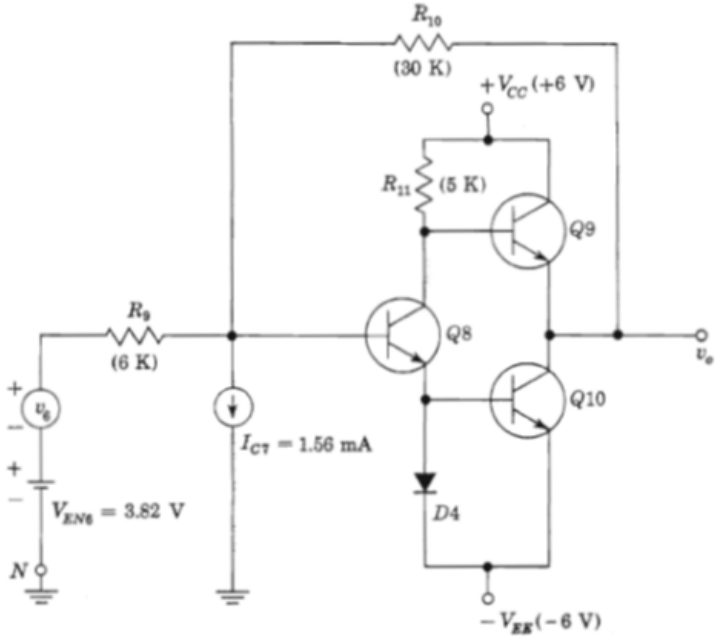


Figure 1.3.6: MC1530 DC analysis calculations - 2: Output stage

1.3.2.2 Small-signal Analysis

Let us perform small-signal analysis calculations on the MC1530 opamp internal circuitry.

$$h_{ie_2} = h_{ie_3} \cong h_{ie_4} = h_{ie_5} = \frac{h_{fe}\gamma}{I_{C_2}} = 5.2\,\text{k}\Omega$$

$$2R_2' = 2R_2 || 2h_{ie_4} = 6.22\,\text{k}\Omega$$

$$R_7' = R_7 || R_{i_6} \cong R_7 = 3\,\text{k}\Omega$$

$$A_{v_1}^* = \frac{v_2}{v_1} = \frac{h_{fe}2R_2'}{2h_{ie_2}} = 59.81$$

$$A_{v_2}^* = \frac{v_3}{v_2} = \frac{-h_{fe}R_7'}{2h_{ie_5}} = -28.85$$

$$A_{v_3}^* = \frac{v_4}{v_3} \cong 1$$

$$A_{v_4} = \frac{v_o}{v_4} \cong \frac{-R_{10}}{R_9} = -5$$

$$\boxed{A_v = A_{v_1}^* A_{v_2}^* A_{v_3}^* A_{v_4} = 8628}$$

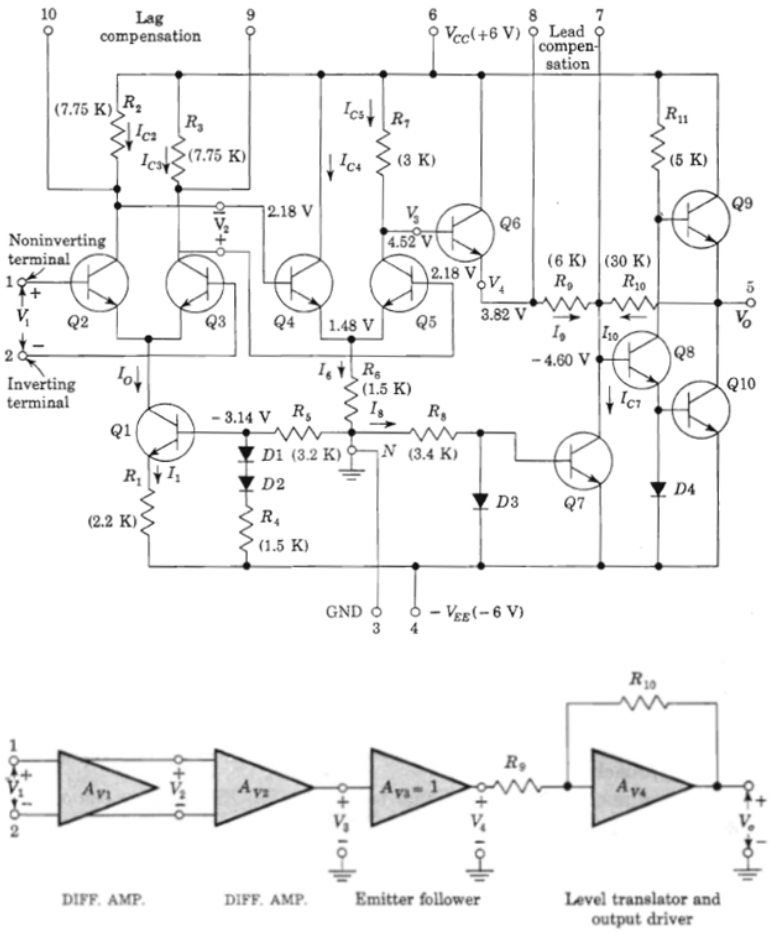


Figure 1.3.7: MC1530 small-signal analysis calculations

1.3.3 Op-Amp Gain

Op-Amps have a very high open-loop gain. They can be connected open- or closed loop.

Open-loop refers to a configuration where there is no feedback from output back to the input. In the open-loop configuration the gain can exceed 10000.

Closed-loop configuration reduces the gain. In order to control the gain of an op-amp it must have feedback. This feedback is a **negative feedback**. A negative feedback will reduce the gain and improve many characteristics of the op-amp

1.3.4 Inverting Op-Amp Amplifier

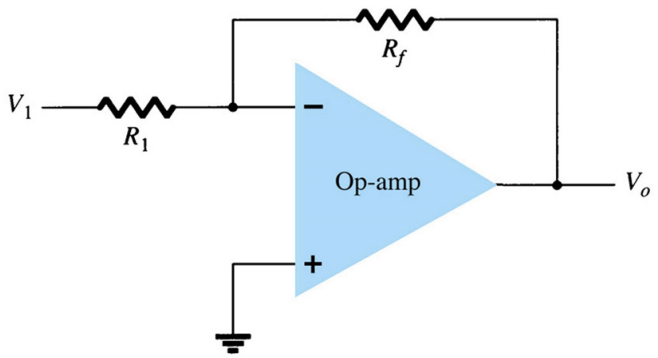


Figure 1.3.8: Inverting op-amp amplifier.

The input is applied to the inverting (−)-input; the non-inverting (+)-input is grounded. The resistor R_f is the feedback resistor; it is connected from the output to the negative (inverting) input. This is **negative feedback**.

1.3.4.1 Virtual Ground

An understanding of the concept of virtual ground provides a better understanding of how an ideal op-amp operates.

- The non-inverting input pin is at ground. The inverting input pin is also at 0 V for an AC signal. This is because ideal op-amp **open-loop gain** is **infinity**. As $A = \infty$,

$$v_+ - v_- = \frac{v_o}{A} = \frac{v_o}{\infty} = 0.$$

  Thus, $v_+ = v_-$.

- As the ideal op-amp **input resistance** is **infinity**, i.e., $R_i = \infty$, no current goes through the terminals of the op-amp, i.e.,

$$i_+ = -i_- = \frac{v_+ - v_-}{R_i} = 0.$$

  Thus, all of the current is through R_f.

Consequently, the inverting op-amp circuit simplifies to the following circuit below

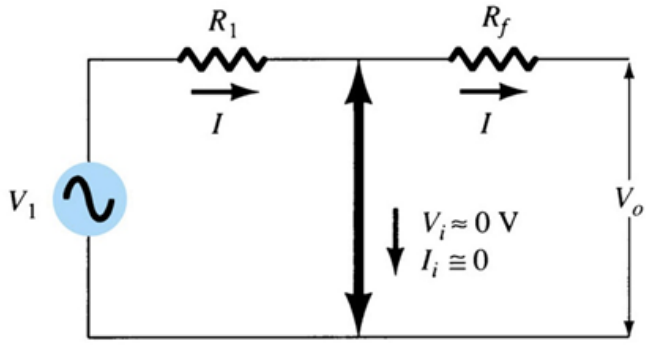


Figure 1.3.9: Simplified inverting amplifier circuit for an ideal op-amp.

1.3.4.2 Gain

From the simplified inverting amplifier circuit,shown in Figure 1.3.9, gain can be determined by external resistors: R_f and R_1.

$$A_v = \frac{v_o}{v_i} = -\frac{R_f}{R_1} \tag{1.3.1}$$

The **negative sign** denotes a 180° phase shift between input and output.

Homework 1.3: Derive the gain when $A \neq \infty$ using normal KVL and KCL equations and observe that when $A \to \infty$ it gives the result above.

Homework 1.4: Derive the same gain using **feedback analysis**, i.e., determine the feedback type, draw the open-loop circuit, find the open-loop gain, obtain the closed-loop gain and then obtain the voltage gain v_o/v_i. Observe that the result is exactly same as the one derived in Homework 1 above.

Homework 1.5: Repeat Homework 1.3 and Homework 1.4 above for the **noninverting amplifier** configuration.

1.3.5 Practical Op-Amp Circuits

Most commonly used opamp circuits are given below:

1. Inverting Amplifier
2. Non-inverting Amplifier
3. Summing Amplifier
4. Unity Follower
5. Integrator
6. Differentiator

1.3.5.1 Inverting Amplifier

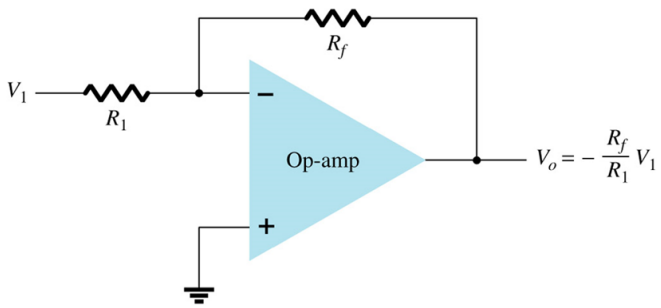


Figure 1.3.10: Inverting amplifier.

$$v_o = -\frac{R_f}{R_1} v_i \tag{1.3.2}$$

1.3.5.2 Non-Inverting Amplifier

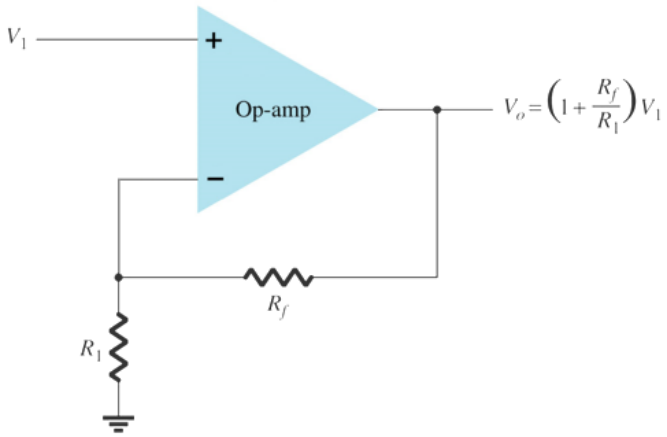


Figure 1.3.11: Non-inverting amplifier.

$$v_o = \left(1 + \frac{R_f}{R_1}\right) v_i \tag{1.3.3}$$

1.3.5.3 Summing Amplifier

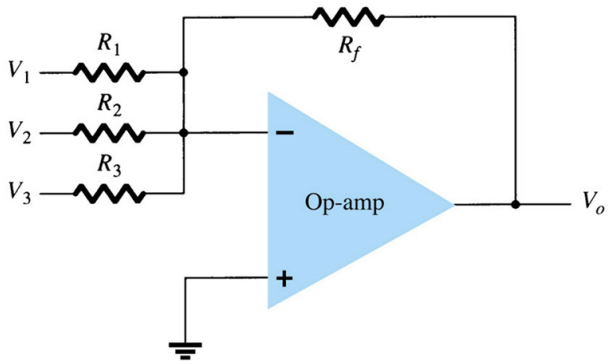


Figure 1.3.12: Summing Amplifier.

$$v_o = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right) \tag{1.3.4}$$

1.3.5.4 Unity Follower

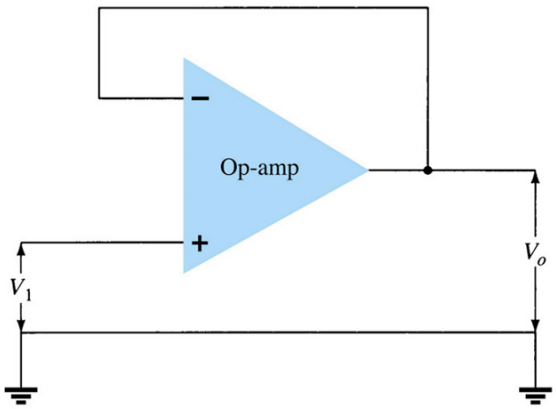


Figure 1.3.13: Unity Follower.

$$v_o = v_i \tag{1.3.5}$$

Any amplifier with no gain (or loss) is called a unity gain amplifier or a voltage buffer. Realistically these circuits will be designed using resistors that are equal ($R_1 = R_f$) to void out problems with offset voltages.

The advantages of using a unity gain amplifier:

- very high input impedance
- very low output impedance

1.3.5.5 Integrator

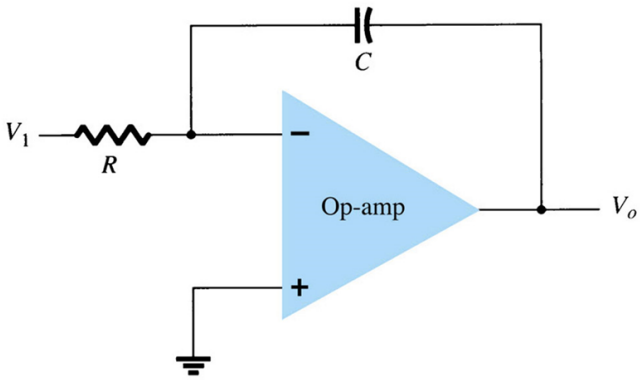


Figure 1.3.14: Integrator.

The output is the integral of the input. Integration is the operation of summing the area under a waveform or curve over a period of time. This circuit is useful in low-pass filter circuits and sensor conditioning circuits.

$$v_o = -\frac{1}{RC}\int v_1(t)dt \tag{1.3.6}$$

1.3.5.6 Differentiator

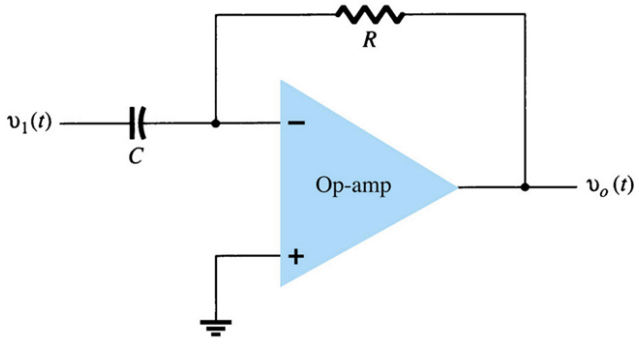


Figure 1.3.15: Differentiator.

The differentiator takes the derivative of the input. This circuit is useful in high-pass filter circuits.

$$v_o = -RC\frac{dv_1(t)}{dt} \tag{1.3.7}$$

1.3.5.7 Logarithmic Amplifier

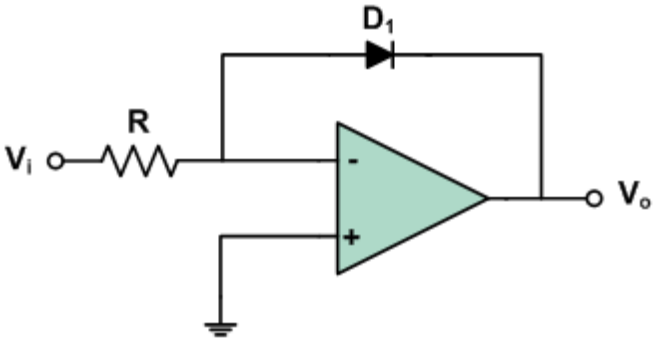


Figure 1.3.16: Integrator.

Homework 1.6: Derive V_o.

HINT: Use the diode characteristic equation under forward bias.

1.3.6 Op-Amp Specifications - DC Bias and Offset Parameters

Even though the input voltage is zero, i.e., $v_{i1} = v_{i2} = 0$, there will be an output, i.e., $v_o \neq 0$. This is called offset. Some of the following can cause this offset.

1. Input Bias Current
2. Input Offset Current

3. Input Offset Voltage
4. Input Offset Voltage and Current Drifts
5. Power Supply Rejection Ratio
6. Open-Loop Voltage Gain
7. Slew Rate
8. Common-Mode Rejection Ratio
9. Input Resistance
10. Output Resistance
11. Open-Loop Bandwidth
12. Power Consumption (no input, no load)
13. Power Dissipation (with input, with load)

1.3.6.1 Input Bias and Offset Currents

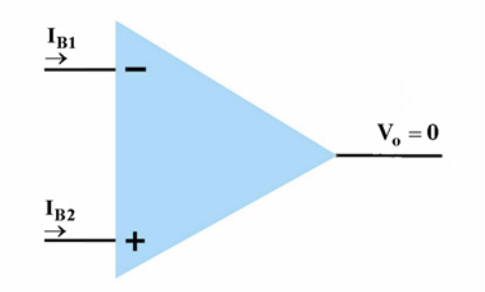


Figure 1.3.17: Input bias currents.

Even though the input voltage is zero, i.e., $v_{i1} = v_{i2} = 0$, sometimes the output is not zero, i.e., $v_o \neq 0$. Then, bias currents I_{B_1} and I_{B_2} are supplied to the opamp to make the output zero, i.e., $v_o = 0$.

- **Input Bias Current** (I_{IB}) is defined as the average of the two bias currents:

$$I_{IB} = \frac{I_{B_1} + I_{B_2}}{2} \tag{1.3.8}$$

- Similarly, **Input Offset Current** (I_{IO}) is defined as the difference of the two bias currents:

$$I_{IO} = I_{B_1} - I_{B_2} \tag{1.3.9}$$

1.3.6.2 Input Offset Voltage

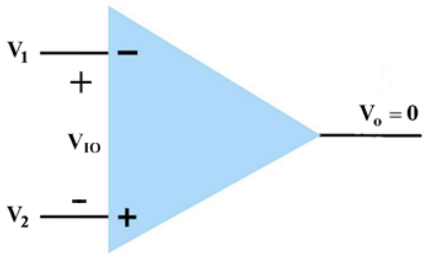


Figure 1.3.18: Input offset voltage.

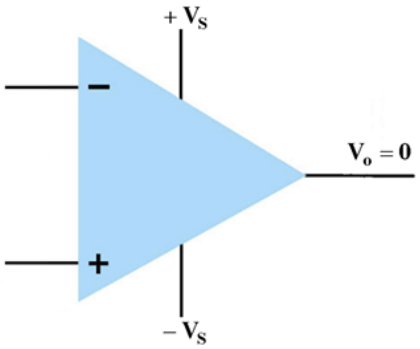
Even though the input voltage is zero, i.e., $v_{i1} = v_{i2} = 0$, sometimes the output is not zero, i.e., $v_o \neq 0$. Then, an offset voltage V_{IO} is supplied to the opamp to make the output zero, i.e., $v_o = 0$. This offset voltage is called the **Input Offset Voltage** defined by

$$V_{IO} = V_1 - V_2 \tag{1.3.10}$$

1.3.6.3 Input Offset Voltage and Current Drifts

Input Offset Voltage Drift, $\frac{\Delta V_{IO}}{\Delta T}$, and Input Offset Current Drift, $\frac{\Delta I_{IO}}{\Delta T}$, where T denotes the temperature, indicate the sensitivities of the input offset voltage and input offset currents to the change in temperature.

1.3.6.4 Power Supply Rejection Ratio



$$S^+ = \left.\frac{\Delta V_{IO}}{\Delta V_S^+}\right|_{V_S^-=0}$$

$$S^- = \left.\frac{\Delta V_{IO}}{\Delta V_S^-}\right|_{V_S^+=0}$$

Figure 1.3.19: Power supply rejection ratio

1.3.6.5 Open-loop voltage gain

Open-loop voltage gain, A_v, of an opamp is **very high**, e.g., for 741, $A_v \cong 2 \times 10^5$.

1.3.6.6 Slew Rate

Slew rate is the time rate of change of the closed-loop amplifier output voltage under large-signal conditions, that is, the maximum rate at which an op-amp can change output without distortion.

$$\text{SR} = \frac{\Delta V_o}{\Delta t}$$

The SR rating is given in the specification sheets as $V/\mu s$ rating.

Maximum Signal Frequency

The slew rate determines the highest frequency of the op-amp without distortion:

$$f \leq \frac{SR}{2\pi V_p}$$

where V_p is the peak voltage.

1.3.6.7 Common-Mode Rejection Ratio

One rating worth mentioning that is unique to op-amps is CMRR or Common-Mode Rejection Ratio.

Because the op-amp has two inputs that are opposite in phase (inverting input and the non-inverting input) any signal that is common to both inputs will be cancelled. A measure of the ability to cancel out common signals is called CMRR and it is given by

$$\text{CMRR (dB)} = 20 \log_{10} \left| \frac{A_d}{A_c} \right| \tag{1.3.11}$$

1.3.6.8 Open-Loop Bandwidth

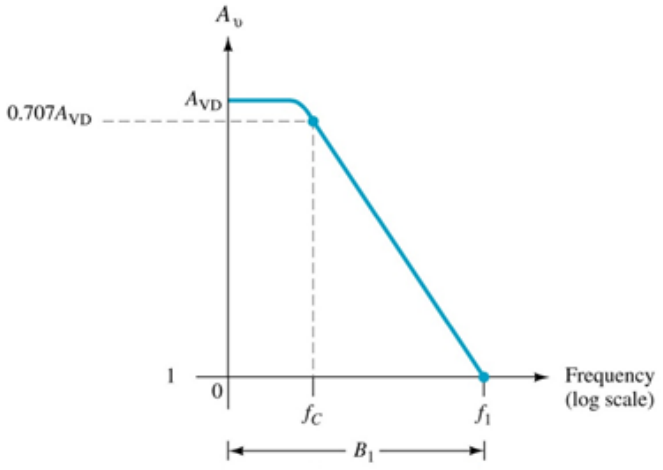


Figure 1.3.20: Op-amp open-loop bandwidth.

The op-amp's high frequency response is limited by internal circuitry. The plot shown is for an open loop gain (A_{OL} or A_{VD}).

This means that the op-amp is operating at the highest possible gain with no feedback resistor.

In the open loop, the op-amp has a narrow bandwidth.

Gain-bandwidth product is constant. So, the bandwidth will widen in closed loop operation, but then the gain will be lower.

1.3.6.9 Op-Amp Performance

The specification sheets will also include graphs that indicate the performance of the op-amp over a wide range of conditions.

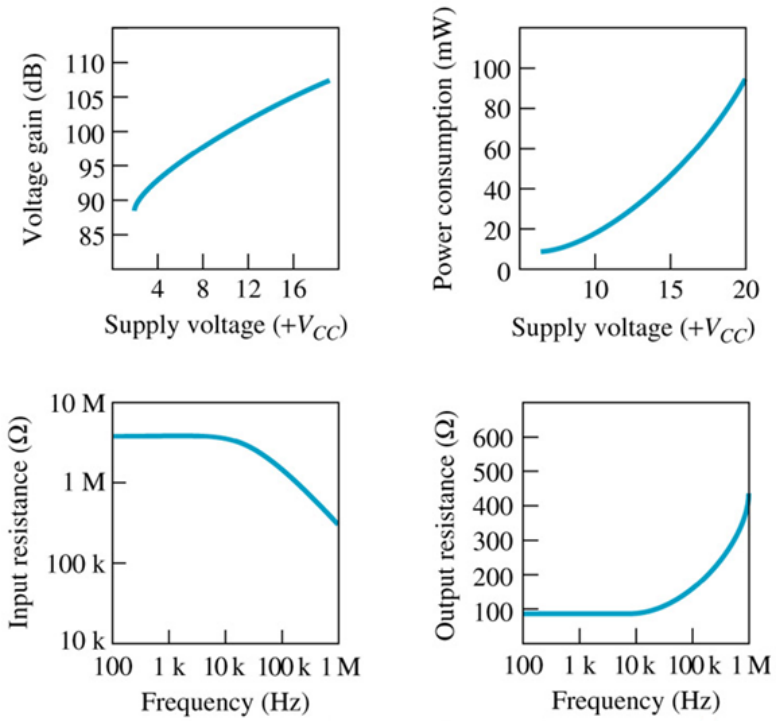


Figure 1.3.21: Some op-amp performance graphs.

The table in Figure 1.3.22 below shows some characteristics of a 741 opamp.

TABLE 13.2 uA741 Electrical Characteristics: $V_{CC} = \pm 15$ V, $T_A = 25°C$

Characteristic	*MIN*	*TYP*	*MAX*	*Unit*
V_{IO} Input offset voltage		1	6	mV
I_{IO} Input offset current		20	200	nA
I_{IB} Input bias current		80	500	nA
V_{ICR} Common-mode input voltage range	±12	±13		V
V_{OM} Maximum peak output voltage swing	±12	±14		V
A_{VD} Large-signal differential voltage amplification	20	200		V/mV
r_i Input resistance	0.3	2		MΩ
r_o Output resistance		75		Ω
C_i Input capacitance		1.4		pF
CMRR Common-mode rejection ratio	70	90		dB
I_{CC} Supply current		1.7	2.8	mA
P_D Total power dissipation		50	85	mW

Figure 1.3.22: Some characteristics of a 741 opamp.

Note that, these ratings are for specific circuit conditions, and they often include minimum, maximum and typical values.

1.3.7 Effects of Offset Voltage and Bias Currents

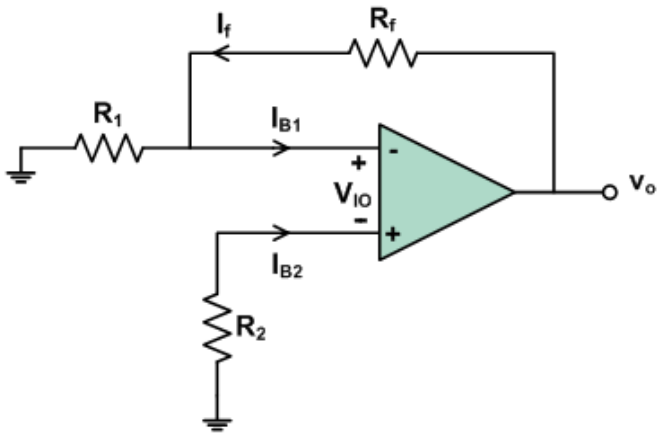


Figure 1.3.23: Effects of offset voltages and bias currents.

Let us write down the two KVL equations (implicitly using KCL) available in Figure 1.3.23 above in order to express output v_o in terms of the input offset voltage, V_{IO}, and input bias currents, I_{B_1} and I_{B_2} when there is no input present, i.e., $v_{i_1} = v_{i_2} = 0$.

$$(I_{B_1} - I_f)R_1 - I_f R_f + v_o = 0 \tag{1.3.12}$$

$$(I_{B_1} - I_f)R_1 + V_{IO} - I_{B_2}R_2 = 0 \tag{1.3.13}$$

Thus, we obtain output v_o by eliminating I_f in the KVL equations above as:

$$\boxed{v_o = \left(1 + \frac{R_f}{R_1}\right) V_{IO} + R_f I_{B_1} - \left(1 + \frac{R_f}{R_1}\right) R_2 I_{B_2}.} \tag{1.3.14}$$

You can also obtain the result in Figure 1.3.14 above by applying the **superposition** theorem.

Note that, the value of R_2 does not affect the gain equations. However, we can select a value of for R_2 in order to **eliminate** the effects of the offset voltage and bias currents. Hence, from the output equation (1.3.14), the value of R_2 which makes the output zero, i.e., $v_o = 0$, is found to be:

$$\boxed{R_2 = \frac{V_{IO}}{I_{B_2}} + (R_f || R_1)\frac{I_{B_1}}{I_{B_2}}.} \tag{1.3.15}$$

Note that, as a rule of thumb we can always select $R_2 = R_f || R_1$. Then, the output equation (1.3.14) reduces to

$$\boxed{v_o = \left(1 + \frac{R_f}{R_1}\right) V_{IO} + R_f I_{IO}.} \tag{1.3.16}$$

So, the output will be zero if both the input offset voltage and current are zero, i.e., $v_o = 0$ if $V_{IO} = 0$ and $I_{IO} = 0$.

Example 1.11: Change the circuit below, in order to eliminate the effect of input offset voltage and current, i.e., make $v_o = 0$, where $V_{IO} = 0\,\text{V}$ and $I_{B_1} = I_{B_2} = 100\,\text{nA}$.

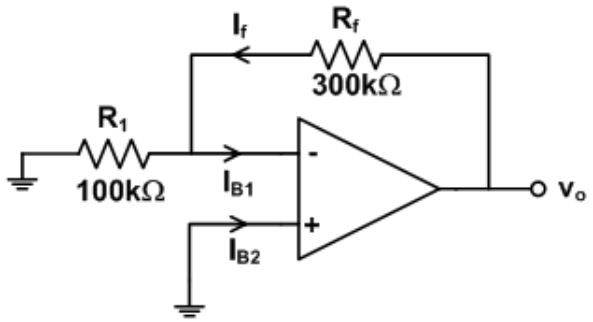


Figure 1.3.24: Opamp Offset Elimination Problem for Example 1.11.

Solution: Let us first show that $v_o \neq 0$ when there is no resistor the non-inverting terminal, i.e., when $R_2 = 0$, as $v_o = R_f I_{B_1} = (0.3M)(0.1\mu) = 30\,\text{mV}$. Thus, the value of R_2 which eliminates the offset is $R_2 = R_1||R_f = 100k||300k = 75\,\text{k}\Omega$.

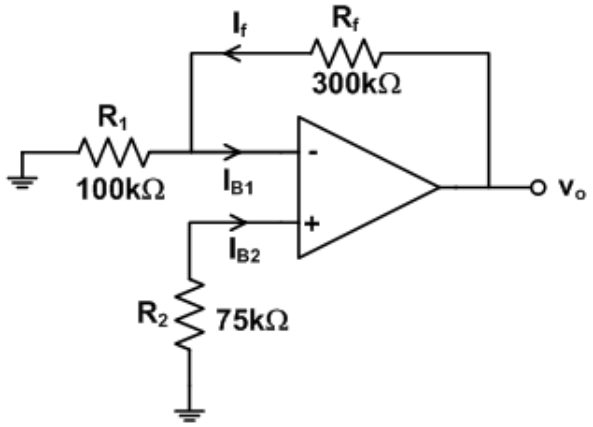


Figure 1.3.25: Opamp Offset Elimination Solution for Example 1.11.

Example 1.12: Change the circuit below, in order to eliminate the effect of input offset voltage and current, i.e., make $v_o = 0$, where $V_{IO} = 0\,\text{V}$, $I_{B_1} = 100\,\text{nA}$ and $I_{B_2} = 80\,\text{nA}$.

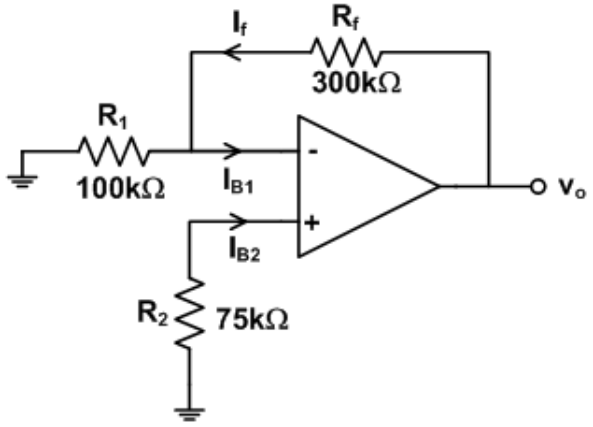


Figure 1.3.26: Opamp Offset Elimination Problem for Example 1.12.

Solution: Let us first show that $v_o \neq 0$ when $R_2 = 75\,\text{k}\Omega$, as $v_o = R_f I_{IO} = (0.3M)(0.02\mu) = 6\,\text{mV}$. Thus, the value of R_2 which eliminates the offset is $R_2 = (R_1||R_f)\frac{I_{B_1}}{I_{B_2}} = 75k(100n/80n) = 93.75\,\text{k}\Omega$.

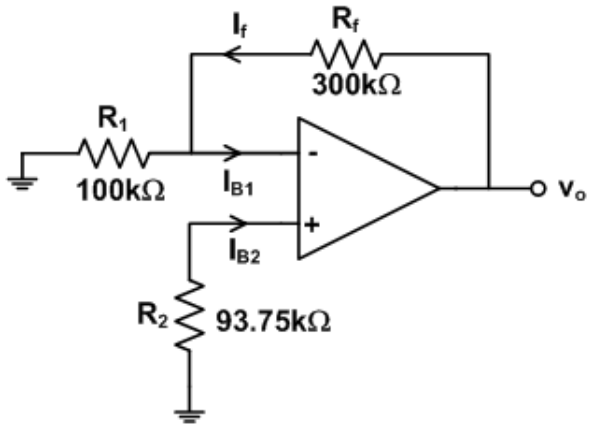


Figure 1.3.27: Opamp Offset Elimination Solution for Example 1.12.

Example 1.13: Change the circuit below, in order to eliminate the effect of input offset voltage and current, i.e., make $v_o = 0$, where $V_{IO} = 2\,\text{mV}$, $I_{B_1} = 100\,\text{nA}$ and $I_{B_2} = 80\,\text{nA}$.

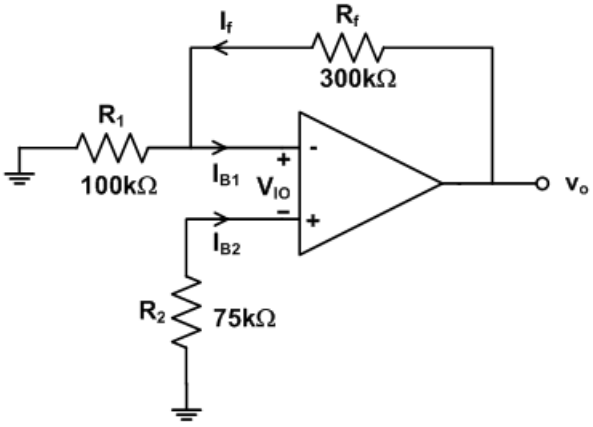


Figure 1.3.28: Opamp Offset Elimination Problem for Example 1.13.

Solution: Let us first show that $v_o \neq 0$ when $R_2 = 75\,\text{k}\Omega$, as $v_o = \left(1 + \dfrac{R_f}{R_1}\right) V_{IO} + R_f I_{IO} = (1 + 0.3M/0.1M)(2m) + (0.3M)(0.02\mu) = 14\,\text{mV}$. Thus, the value of R_2 which eliminates the offset is $R_2 = \frac{V_{IO}}{I_{B_2}} + (R_1||R_f)\frac{I_{B_1}}{I_{B_2}} = 25k + 93.75k = 118.75\,\text{k}\Omega$.

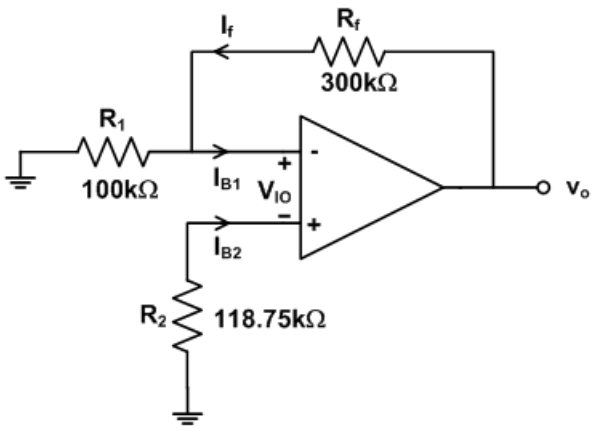


Figure 1.3.29: Opamp Offset Elimination Solution for Example 1.13.

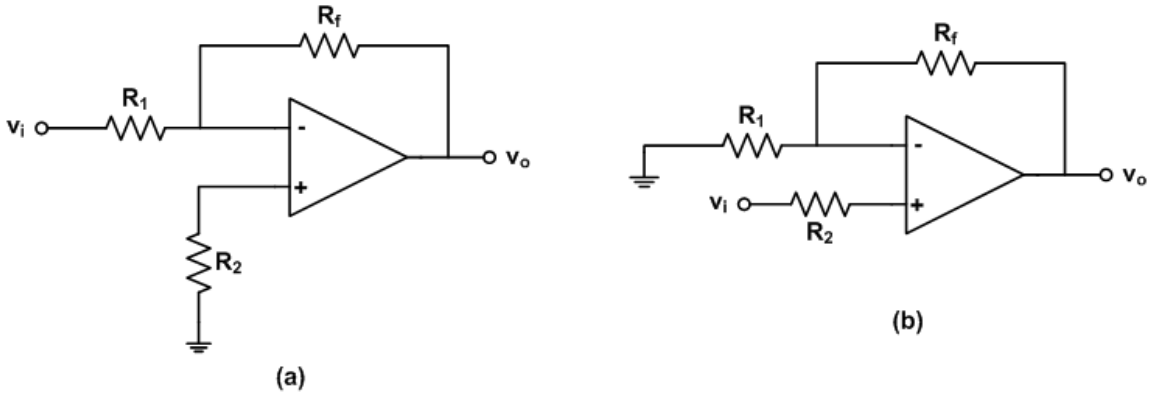


Figure 1.3.30: Opamp amplifier with R_2 resistor: (a) inverting (b) noninverting.

Figure 1.3.30a and Figure 1.3.30b above show inverting and noninverting amplifiers both with an offset compensation R_2 resistors, respectively.

As a rule of thumb, always use an R_2 resistor in your opamp circuit, at least with a value of $R_2 = R_1||R_f$.

1.3.8 Multistage Gains

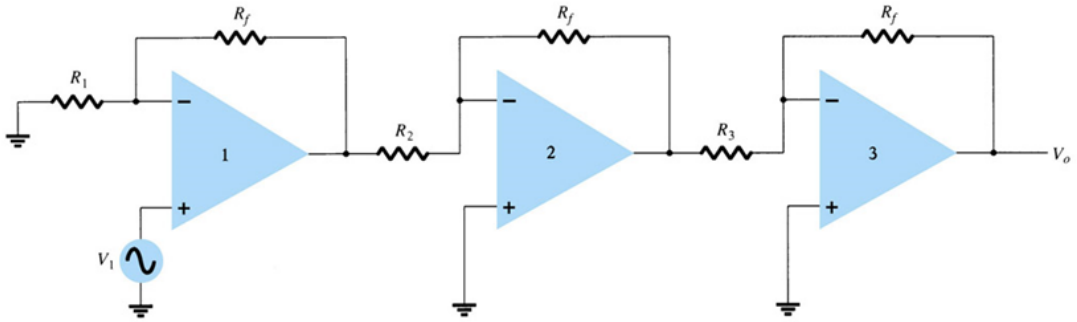


Figure 1.3.31: Multistage opamp amplifiers.

As a voltage-gain amplifier, the input resistance of op-amp amplifiers are high and the output resistances are small. So, when cascaded we can ignore the loading effects and multiply the gains of each stage in order to find overall gain, i.e.,

$$A_v = \frac{v_o}{v_i} = A_{V_1} A_{V_2} A_{v_3} \tag{1.3.17}$$

$$= \left(A_{v_1} \frac{R_{i_2}}{R_{i_2} + R_{o_1}} \right) \left(A_{v_2} \frac{R_{i_3}}{R_{i_3} + R_{o_2}} \right) A_{v_3} \tag{1.3.18}$$

$$\cong A_{v_1} \times A_{v_2} \times A_{v_3} \tag{1.3.19}$$

$$= \left(1 + \frac{R_f}{R_1} \right) \left(-\frac{R_f}{R_2} \right) \left(-\frac{R_f}{R_3} \right) \tag{1.3.20}$$

1.3.9 Active Filters

Adding capacitors to op-amp circuits provides an external control for the cutoff frequencies. The op-amp active filter provides controllable cutoff frequencies and controllable gain

- Lowpass Filter
- Highpass Filter
- Bandpass Filter

1.3.9.1 Lowpass Filter

- First-order lowpass filter

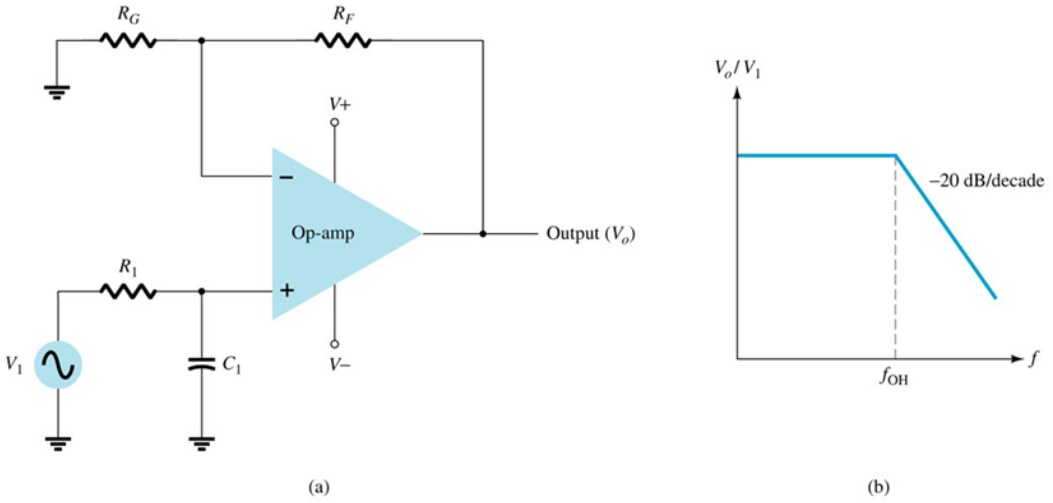


Figure 1.3.32: First-order lowpass filter (a) Circuit (b) Bode magnitude plot

- The upper (or higher) cutoff frequency f_{OH} is

$$\boxed{f_{OH} = \frac{1}{2\pi R_1 C_1}} \tag{1.3.21}$$

- Low frequency gain A_v is

$$\boxed{A_v = 1 + \frac{R_F}{R_G}} \tag{1.3.22}$$

- Second-order lowpass filter

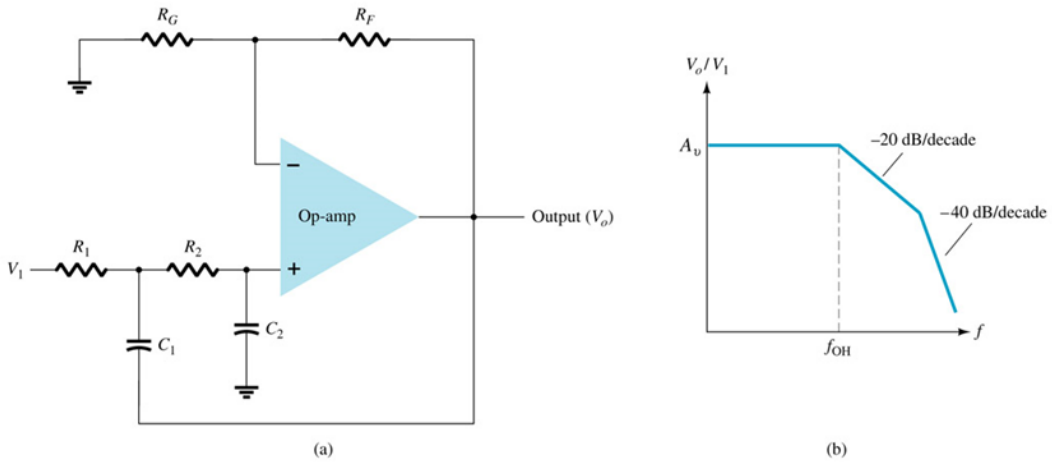


Figure 1.3.33: Second-order lowpass filter (a) Circuit (b) Bode magnitude plot

- By adding more RC networks the roll-off can be made steeper. Each RC network adds and additional 20 dB/decade (or 6 dB/octave) slope.

1.3.9.2 Highpass Filter

- First-order highpass filter

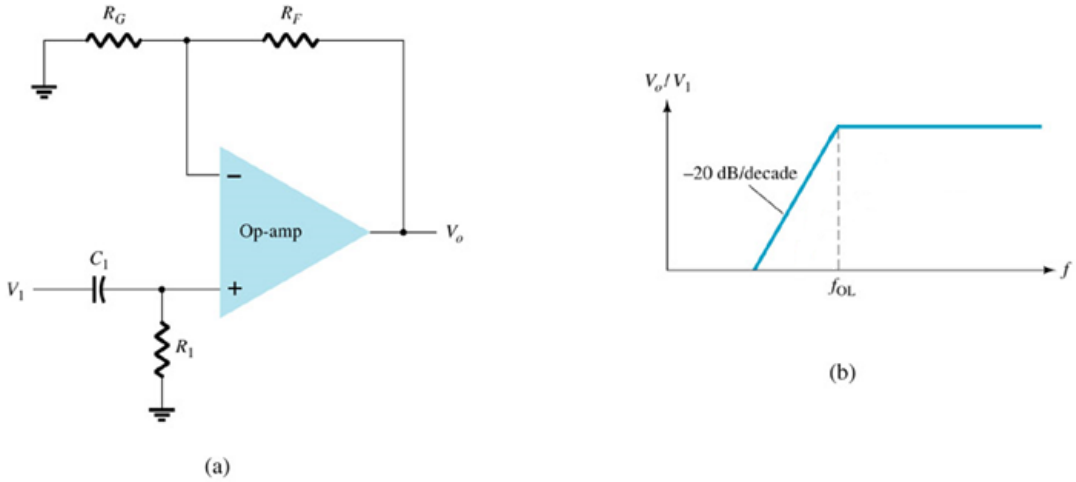


Figure 1.3.34: First-order highpass filter (a) Circuit (b) Bode magnitude plot

- The lower cutoff frequency f_{OL} is

$$\boxed{f_{OL} = \frac{1}{2\pi R_1 C_1}} \tag{1.3.23}$$

- High frequency gain A_v is

$$\boxed{A_v = 1 + \frac{R_F}{R_G}} \tag{1.3.24}$$

1.3.9.3 Bandpass Filter

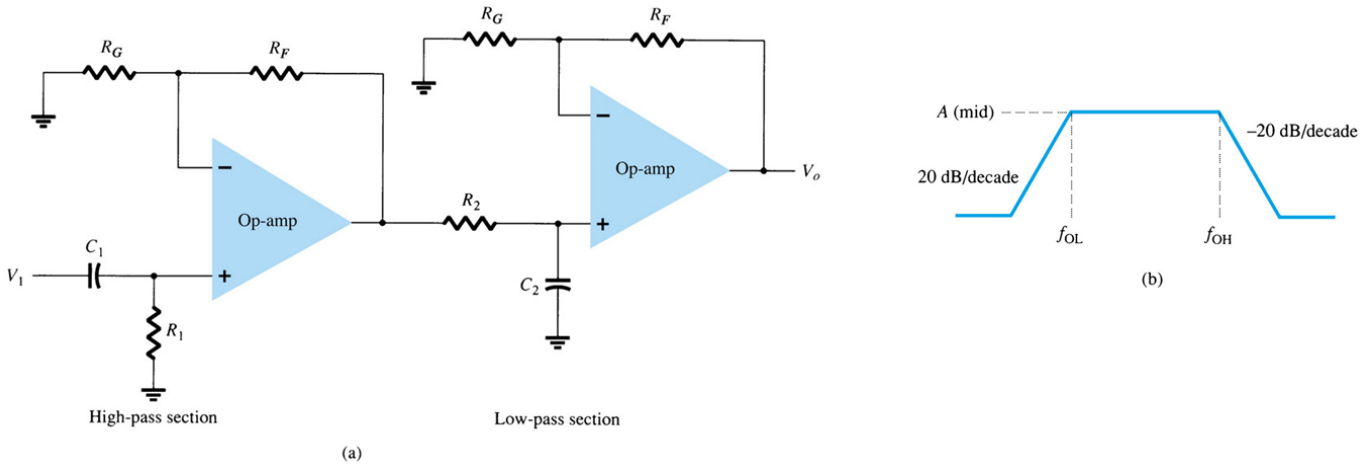


Figure 1.3.35: First-order bandpass filter (a) Circuit (b) Bode magnitude plot

- There are two cutoff frequencies: upper and lower. They can be calculated using the same low-pass cutoff and high-pass cutoff frequency formulas given in the previous sections.

1.4 Power Amplifiers

So far we have dealt with only small-signal amplifiers. In small-signal amplifiers the main factors were

- amplification
- linearity
- gain

Large-signal or **power amplifiers** function primarily to provide sufficient power to drive the output device. These amplifier circuits will handle large voltage signals and high current levels. The main factors are

- efficiency
- maximum power capability
- impedance matching to the output device

1.4.1 Power Amplifier Types

Main classes of power amplifiers are given below

1. Class A
2. Class B
3. Class AB
4. Class C
5. Class D

1.4.1.1 Class A Operation

The output of a Class A amplifier conducts for the full 360° of the cycle as shown below.

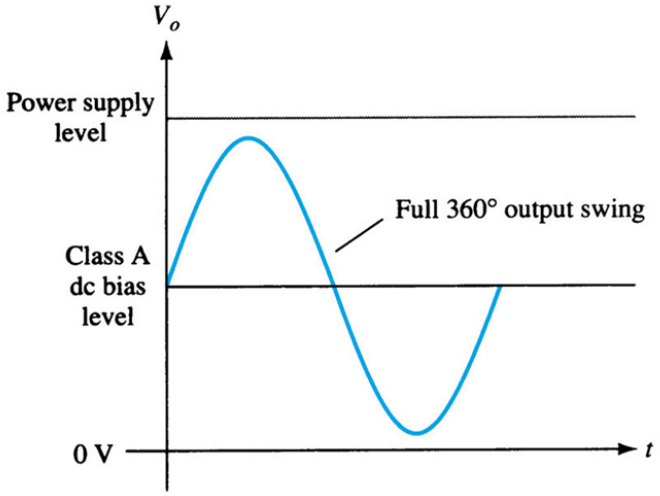


Figure 1.4.1: Class A amplifier output (full-cycle operation)

The Q-point (bias level) must be biased towards the middle of the load line so that the AC signal can swing a full cycle. Remember that the DC load line indicates the maximum and minimum limits set by the DC power supply.

The efficiency is **low**, because the transistor is **always on**, even when there is no AC input.

1.4.1.2 Class B Operation

A Class B amplifier output only conducts for 180° or half-cycle of the input signal as shown below.

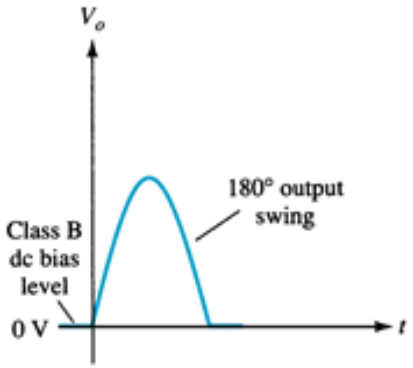


Figure 1.4.2: A Class B amplifier output (half-cycle operation)

The Q-point (bias level) is at **cut-off** (i.e., current is zero) on the load line, so that the AC signal can only swing for one half of a cycle.

The efficiency is **high**, because the transistor is **off**, when there is no AC input. However, we will need two transistor in order to produce a full cycle-output.

1.4.1.3 Class AB Operation

A Class AB amplifier output conducts between 180° and 360° of the AC input signal.

This amplifier is in between the Class A and Class B. The Q-point (bias level) is above the Class B but below the Class A.

1.4.1.4 Class C Operation

The output of the Class C conducts for less than 180° of the AC cycle and will operate only with a tuned (resonant) circuit. The Q-point (bias level) is at cutoff, the output signal is very small.

1.4.1.5 Class D Operation

The Class D output is more like pulse signals which are on for a short interval and off for a longer interval. It does not resemble the AC sine wave input, however it is possible to obtain full sine wave output using digital signal processing techniques.

1.4.1.6 Amplifier Efficiency

Efficiency refers to the ratio of output to input power. The lower the amount of conduction of the amplifier the higher the efficiency, so the efficiency improves (gets higher) going from Class A to Class D.

TABLE 15.1 Comparison of Amplifier Classes

	Class A	Class AB	Class B	Class C*	Class D
Operating cycle	360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%		Typically over 90%

*Class C is usually not used for delivering large amounts of power, thus the efficiency is not given here.

Figure 1.4.3: Comparison of amplifier classes

Efficiency η is defined as the ratio of the power output to the power input, i.e.,

$$\boxed{\eta\% = \frac{P_L}{P_{CC}} \times 100} \tag{1.4.1}$$

where P_L is the **power output** and P_{CC} is the **power input**.

1.4.1.7 Power Input

The power into the amplifier is from the DC supply. With no input signal, the DC current drawn is the collector bias current, I_{CQ}.

Thus, power input P_{CC} is defined as the power drawn from the power supply

$$P_{CC} = V_{CC} I_{CQ} \tag{1.4.2}$$

1.4.1.8 Power Output

$$P_L = v_{o(rms)} i_{o(rms)} \tag{1.4.3}$$

$$= \frac{v_{o_{peak}} i_{o_{peak}}}{2}$$

$$= \frac{v_{o_{peak}}^2}{2R_L} \tag{1.4.4}$$

$$= \frac{v_{o_{peak-peak}}^2}{8R_L}$$

1.4.1.9 Transistor Power Dissipation

Power dissipated as heat across a transistor is given as

$$P_Q = \frac{1}{N_Q}(P_{CC} - P_L) \tag{1.4.5}$$

where N_Q is the number of transistors used in the power amplifier configuration.

NOTE: The larger the output signal, the lower the heat dissipation.

1.4.1.10 Figure of Merit

Figure of Merit (FoM) is a quantity used to characterize the cost performance of the power amplifier in terms of the ratio of the maximum power dissipated by a transistor and the maximum power delivered to the load, i.e.,

$$\text{FoM} = \frac{P_{Q_{max}}}{P_{L_{max}}} \tag{1.4.6}$$

NOTE: The **lower** the FoM, the **better** the cost performance. Because the higher the maximum power rating of a transistor, the higher the price.

1.4.2 Series-Fed Class A Amplifier

This is similar to the small-signal amplifier except that it will handle higher voltages. The Q-point (bias level) is biased in the middle of the load line for maximum efficiency.

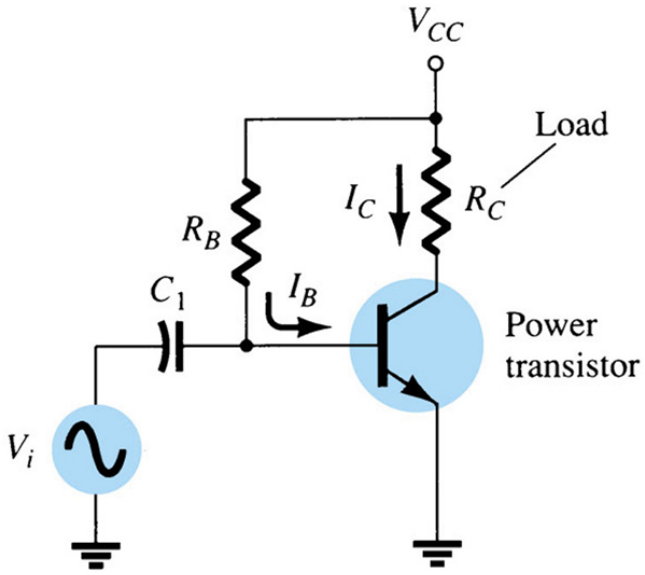


Figure 1.4.4: Series-fed Class A large-signal amplifier

The transistor used is a high power transistor. The current gain β of a power transistor is generally less than 100. Power transistors are capable of handling large power or current while not providing much voltage gain.

1.4.2.1 AC-DC Load Lines

As overall resistances of DC and AC output-loops are equal to each other, i.e., $R_{DC} = R_{ac} = R_C$, AC load line is equal to the DC load line ($V_{CE} = V_{CC} - I_C R_C$)as shown in Figure 1.4.5 below.

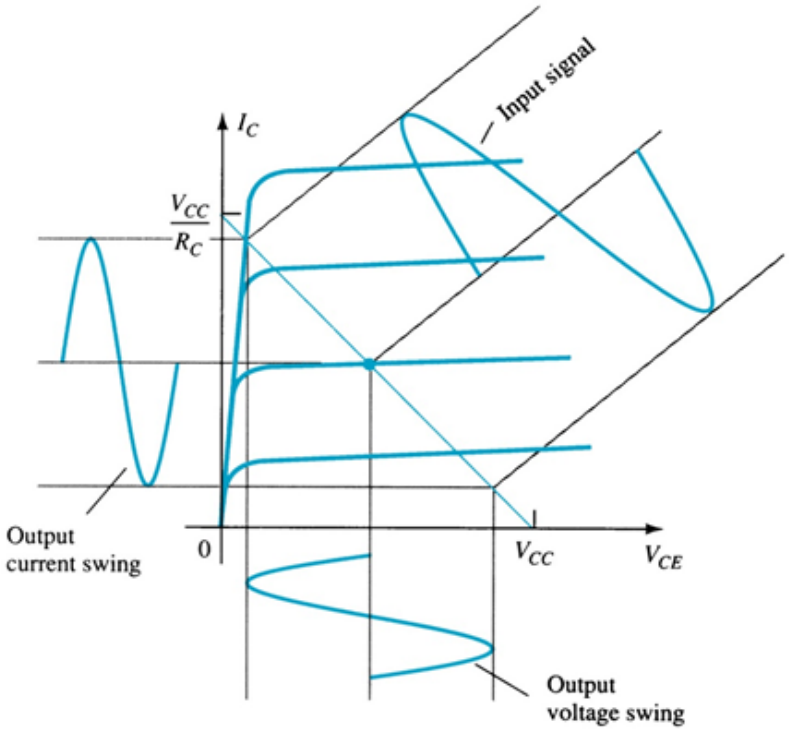


Figure 1.4.5: AC-DC load-line for the series-fed Class A amplifier in Figure 1.4.4

For maximum undistorted output swing, we need to set the Q-point at the middle of the AC load line, i.e.,

$$V_{CEQ} = \frac{V_{CC}}{2}$$

and

$$I_{CQ} = \frac{V_{CC}}{2R_C}.$$

Thus, peak value of the maximum output voltage swing is given by

$$\boxed{v_{o(max)_{peak}} = v_{ce(max)_{peak}} = \frac{V_{CC}}{2}}. \tag{1.4.7}$$

Then, we can choose a value for R_B in order to obtain the desired Q-point values, i.e.,

$$R_B = \frac{V_{CC} - V_{BE(ON)}}{I_{BQ}} = \frac{V_{CC} - V_{BE(ON)}}{I_{CQ}/\beta} \tag{1.4.8}$$

NOTE: Once the value of R_B is given, it means that the Q-point is already set. Then, we have to make (or adjust) our calculations according to the given Q-point. For example, according to a given

Q-point maximum undistorted output voltage swing will be the minimum of V_{CEQ} and $V_{CC} - V_{CEQ}$, i.e.,

$$v_{ce(max)_{peak}}\big|_{Q\text{-point}} = \min\left(V_{CEQ}, V_{CC} - V_{CEQ}\right) \tag{1.4.9}$$

1.4.2.2 Power Input

$$P_{CC} = V_{CC} I_{CQ}$$

1.4.2.3 Power Output

$$\begin{aligned} P_L &= \frac{v_{o_{peak}}^2}{2R_C} \\ &= \frac{v_{o_{peak-peak}}^2}{8R_C} \end{aligned} \tag{1.4.10}$$

1.4.2.4 Efficiency

$$\begin{aligned} \eta\% &= \frac{P_L}{P_{CC}} \times 100 \\ &= \frac{v_{o_{peak}}^2/(2R_C)}{V_{CC} I_{CQ}} \times 100 \end{aligned} \tag{1.4.11}$$

1.4.2.5 Transistor Power Dissipation

Power dissipated as heat across a transistor is given as

$$\begin{aligned} P_Q &= P_{CC} - P_L \\ &= V_{CC} I_{CQ} - \frac{v_{o_{peak}}^2}{2R_C} \end{aligned} \tag{1.4.12}$$

1.4.2.6 Maximum Efficiency

Maximum efficiency η_{max} is achieved at the maximum output power $P_{L(max)}$, i.e., at the maximum output swing $v_{o(max)_{peak}} = \frac{V_{CC}}{2}$. Thus,

$$P_{L(max)} = \frac{v_{o(max)_{peak}}^2}{2R_C} = \frac{\left(V_{CC}/2\right)^2}{2R_C} = \frac{V_{CC}^2}{8R_C} \tag{1.4.13}$$

Similarly, the input power at the maximum undistorted swing is given as

$$P_{CC}|_{P_{L(max)}} = V_{CC}\ I_{CQ}|_{v_{o(max)}} = V_{CC}\left(\frac{V_{CC}}{2R_C}\right) = \frac{V_{CC}^2}{2R_C} \tag{1.4.14}$$

Thus, maximum efficiency η_{max} is given as

$$\eta_{max}\% = \frac{P_{L(max)}}{P_{CC}|_{P_{L(max)}}} \times 100 \tag{1.4.15}$$

$$= \frac{V_{CC}^2/(8R_C)}{V_{CC}^2/(2R_C)} \times 100 \tag{1.4.16}$$

$$= \frac{1}{4} \times 100 \tag{1.4.17}$$

$$= 25\%. \tag{1.4.18}$$

1.4.2.7 Figure of Merit

As transistor power dissipation is given by (1.4.12), maximum transistor power is dissipated when there is no AC input and output, i.e., $P_L = 0$

$$P_{Q(max)} = P_{CC}|_{P_{L(max)}} - 0 = P_{CC}|_{P_{L(max)}} = \frac{V_{CC}^2}{2R_C}. \tag{1.4.19}$$

Thus, figure of merit (FoM) is given as

$$\text{FoM} = \frac{P_{Q(max)}}{P_{L(max)}} \tag{1.4.20}$$

$$= \frac{V_{CC}^2/(2R_C)}{V_{CC}^2/(8R_C)} \tag{1.4.21}$$

$$= 4. \tag{1.4.22}$$

This FoM value shows that a series-fed Class A amplifier is not a good choice as a power amplifier. Because, if we want to deliver 10 W to the load, we need to select a 40 W-transistor.

1.4.3 Transformer-Coupled Class A Amplifier

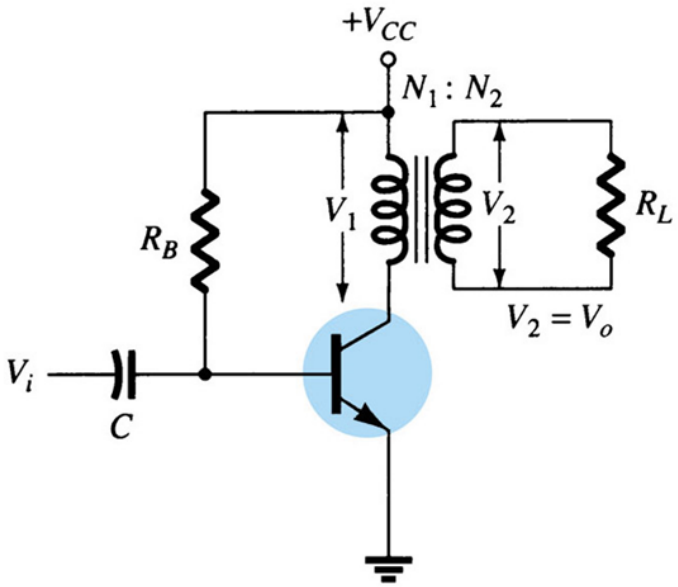


Figure 1.4.6: Transformer-coupled Class A power amplifier

This circuit uses a transformer to couple to the load. This improves the efficiency of the Class A to 50%.

1.4.3.1 AC-DC Load Lines

DC Load-Line

In DC operation, transformer action is not present we only have the DC resistance of the primary winding which is taken as **zero**. So, the overall DC resistance of the output-loop, R_{DC} is also zero, i.e.,

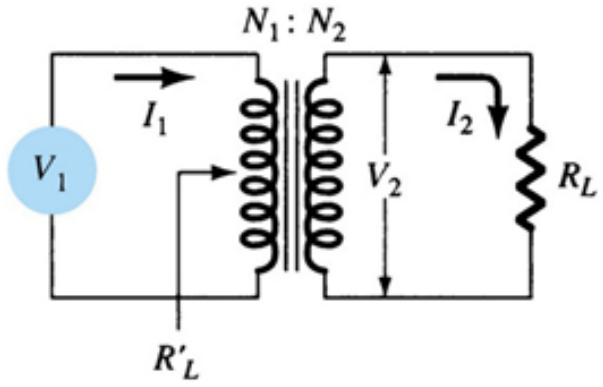
$$R_{DC} = 0. \tag{1.4.23}$$

Thus, the **DC load-line equation** is given by

$$\boxed{V_{CE} = V_{CC}}. \tag{1.4.24}$$

AC Load-Line

In AC operation, transformer action is present as shown in Figure 1.4.7 below. Transformers transform voltage, current and **impedance**.



$a = \frac{N_1}{N_2}$, $V_1 = aV_2$, $I_2 = aI_1$ and

$$\boxed{R'_L = a^2 R_L}$$

Figure 1.4.7: Transformer operation

So, overall AC resistance of the output-loop, R_{ac} is equal to the equivalent primary-side load R'_L, i.e.,

$$R_{ac} = R'_L \tag{1.4.25}$$

where

$$R'_L = a^2 R_L, \tag{1.4.26}$$

and a is the turns ratio of the transformer, i.e., $a = \frac{N_1}{N_2}$. Thus, **AC load-line equation** is then given by

$$\boxed{i_C = \frac{-1}{R'_L} v_{CE} + I_{CQ} + \frac{V_{CEQ}}{R'_L}}. \tag{1.4.27}$$

Finally, we can plot the AC-DC load-lines together as shown in below.

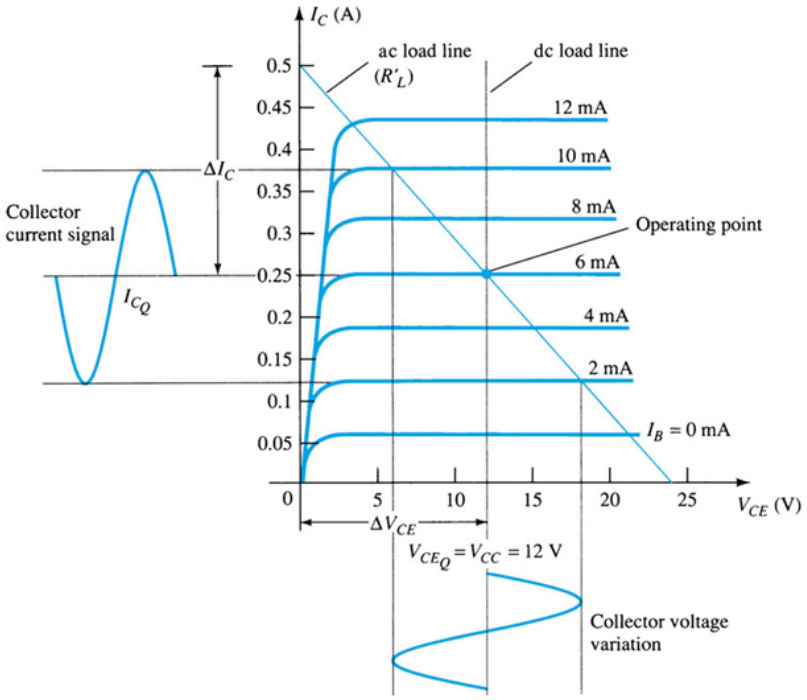


Figure 1.4.8: AC-DC load-line of the transformer-coupled Class A amplifier in Figure 1.4.6

For maximum undistorted output swing, we need to set the Q-point at the middle of the AC load line, to satisfy

$$v_{o(max)_{peak}} = v_{ce(max)_{peak}} = V_{CEQ} = V_{CC} \tag{1.4.28}$$

with

$$I_{CQ} = \frac{V_{CEQ}}{R'_L} = \frac{V_{CC}}{R'_L}$$

.

Then, we can choose a value for R_B in order to obtain the desired Q-point values, i.e.,

$$R_B = \frac{V_{CC} - V_{BE(ON)}}{I_{BQ}} = \frac{V_{CC} - V_{BE(ON)}}{I_{CQ}/\beta} \tag{1.4.29}$$

NOTE: Once the value of R_B is given, it means that the Q-point is already set. Then, we have to make (or adjust) our calculations according to the given Q-point. For example, according to a given Q-point maximum undistorted output voltage swing will be the minimum of V_{CEQ} and $I_{CQ}R'_L$, i.e.,

$$v_{ce(max)_{peak}}\big|_{Q\text{-point}} = \min\left(V_{CC}, I_{CQ}R'_L\right) \tag{1.4.30}$$

1.4.3.2 Power Input

$$P_{CC} = V_{CC}I_{CQ}$$

1.4.3.3 Power Output

$$P_L = \frac{v^2_{o_{peak}}}{2R'_L} \tag{1.4.31}$$

1.4.3.4 Efficiency

$$\begin{aligned} \eta\% &= \frac{P_L}{P_{CC}} \times 100 \\ &= \frac{v^2_{o_{peak}}/(2R'_L)}{V_{CC}I_{CQ}} \times 100 \end{aligned} \tag{1.4.32}$$

1.4.3.5 Transistor Power Dissipation

Power dissipated as heat across a transistor is given as

$$\begin{aligned} P_Q &= P_{CC} - P_L \\ &= V_{CC}I_{CQ} - \frac{v^2_{o_{peak}}}{2R'_L} \end{aligned} \tag{1.4.33}$$

1.4.3.6 Maximum Efficiency

Maximum efficiency η_{max} is achieved at the maximum output power $P_{L(max)}$, i.e., at the maximum output swing $v_{o(max)_{peak}} = V_{CC}$. Thus,

$$P_{L(max)} = \frac{v^2_{o(max)_{peak}}}{2R'_L} = \frac{V^2_{CC}}{2R'_L} \tag{1.4.34}$$

Similarly, the input power at the maximum undistorted swing is given as

$$P_{CC}|_{P_{L(max)}} = V_{CC}\ I_{CQ}|_{v_{o(max)}} = V_{CC}\left(\frac{V_{CC}}{R'_L}\right) = \frac{V^2_{CC}}{R'_L} \tag{1.4.35}$$

Thus, maximum efficiency η_{max} is given as

$$\begin{aligned}
\eta_{max}\% &= \frac{P_{L(max)}}{P_{CC}|_{P_{L(max)}}} \times 100 \\
&= \frac{V^2_{CC}/(2R'_L)}{V^2_{CC}/R'_L} \times 100 && (1.4.36) \\
&= \frac{1}{2} \times 100 && (1.4.37) \\
&= 50\%. && (1.4.38)
\end{aligned}$$

1.4.3.7 Figure of Merit

As transistor power dissipation is given by (1.4.33), maximum transistor power is dissipated when there is no AC input and output, i.e., $P_L = 0$

$$P_{Q(max)} = P_{CC}|_{P_{L(max)}} - 0 = P_{CC}|_{P_{L(max)}} = \frac{V^2_{CC}}{R'_L}. \tag{1.4.39}$$

Thus, figure of merit (FoM) is given as

$$\begin{aligned}
\text{FoM} &= \frac{P_{Q(max)}}{P_{L(max)}} && (1.4.40) \\
&= \frac{V^2_{CC}/R'_L}{V^2_{CC}/(2R'_L)} && (1.4.41) \\
&= 2. && (1.4.42)
\end{aligned}$$

This FoM value is not also very good. Because, if we want to deliver 10 W to the load, we need to select a 20 W-transistor.

1.4.4 Class B Amplifiers

In Class B the DC bias leaves the transistor biased just off (i.e., at cut-off). The AC signal turns the transistor on. This is essentially no bias. The transistor only **conducts** when it is turned on by **half** of the AC cycle.

In order to get a **full** AC cycle out of a Class B amplifier, you need **two** transistors.

In a transformer-coupled push-pull arrangement, two *npn*-transistors are one works on the positive half of the input signal and the other works on the inverted negative half of the input signal. In a complementary-symmetry push-pull arrangement, one is an *npn*-transistor that provides the positive half of the AC cycle and the other is a *pnp* transistor that provides the negative half.

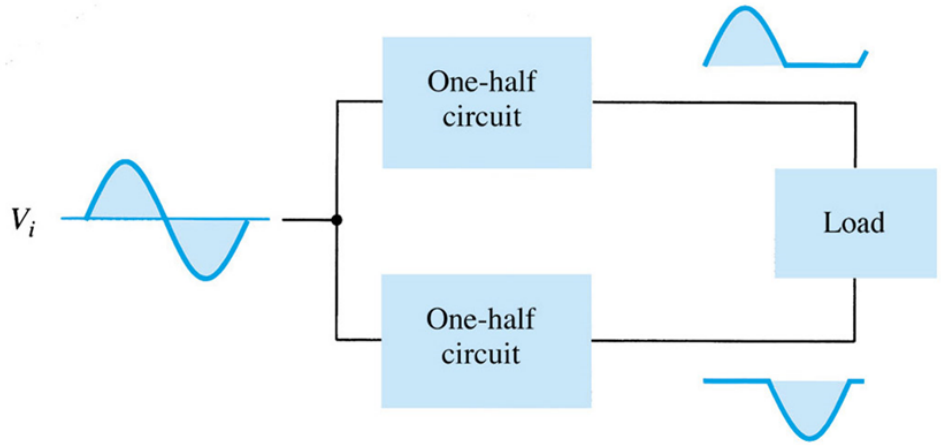


Figure 1.4.9: Class B amplifier push-pull operation block diagram

1.4.4.1 Phase Splitter Circuits

If the input is in the form of two opposite polarity signals, two similar stages could be used, each operating on the alternate cycle because of the input signal. Figure 1.4.10 shows a center-tapped transformer to provide opposite phase signals. If the transformer is exactly center-tapped, the two signals are exactly opposite in phase and of the same magnitude. The circuit of Figure 1.4.10 uses a BJT stage with in-phase output from the emitter and opposite phase output from the collector. If the gain is made nearly 1 for each output, the same magnitude results. Probably most common would be using op-amp stages similar to Figure 1.4.11, one to provide an inverting gain of unity and the other a non-inverting gain of unity, to provide two outputs of the same magnitude but of opposite phase.

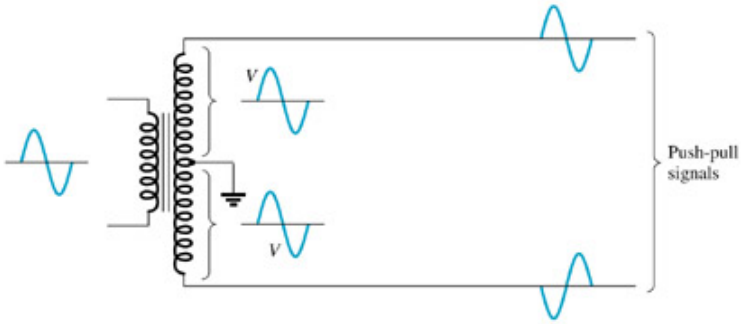


Figure 1.4.10: Phase splitter circuit with a center-tapped transformer

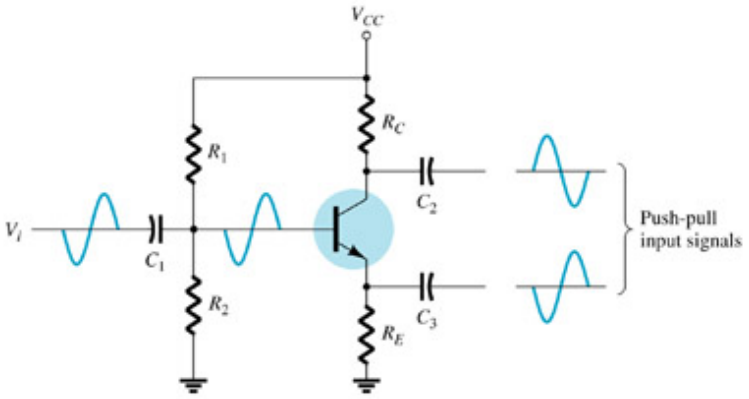


Figure 1.4.11: Phase splitter circuit with a BJT transistor

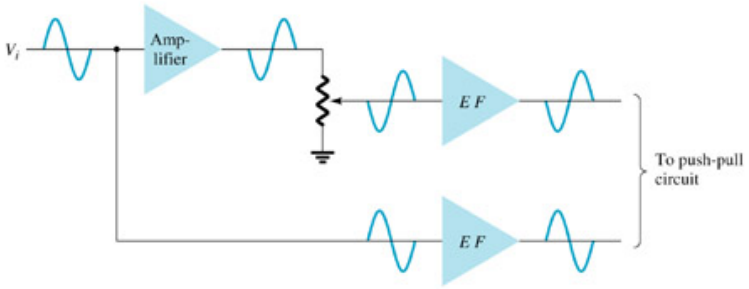


Figure 1.4.12: Phase splitter circuit with op-amp(s)

1.4.4.2 Transformer-Coupled Push-Pull Class B Amplifier

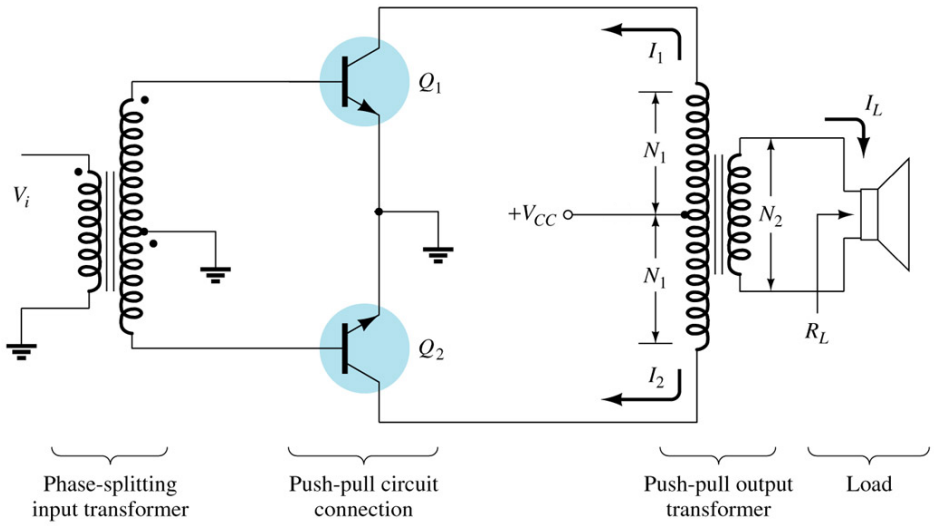


Figure 1.4.13: Transformer-coupled push-pull Class B power amplifier

The center-tapped transformer on the input produces **opposite polarity** signals to the two transistor inputs.

The center-tapped transformer on the output **combines** the two halves of the AC waveform together.

Push-Pull Operation

- During the **positive half** of the AC input cycle:
  - Transistor Q_1 is conducting and Q_2 is off.
- During the **negative half** of the AC input cycle:
  - Transistor Q_2 is conducting and Q_1 is off.

Each transistor produces half of an AC cycle. The output transformer combines the two outputs to form a full AC cycle.

1.4.4.3 Complementary-Symmetry Push-Pull Class B Amplifier

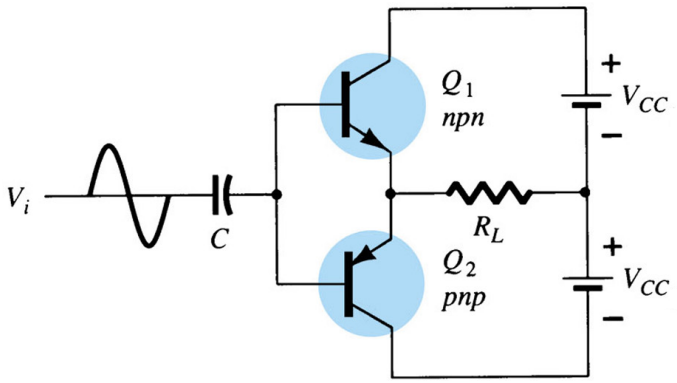


Figure 1.4.14: Complementary-symmetry push-pull Class B power amplifier

Using complementary transistors (*npn* and *pnp*), it is possible to obtain a full cycle output across a load using half-cycles of operation from each transistor, as shown in Figure 1.4.14. While a single input signal is applied to the base of both transistors, the transistors, being of opposite type, will conduct on opposite half-cycles of the input. The *npn*-transistor will be biased into conduction by the positive half-cycle of signal, with a resulting half-cycle of signal across the load as shown in Figure 1.4.15. During the negative half-cycle of signal, the pnp transistor is biased into conduction when the input goes negative, as shown in Figure 1.4.16. During a complete cycle of the input, a complete cycle of output signal is developed across the load. One big advantage of this configuration is avoiding the need for a transformer.

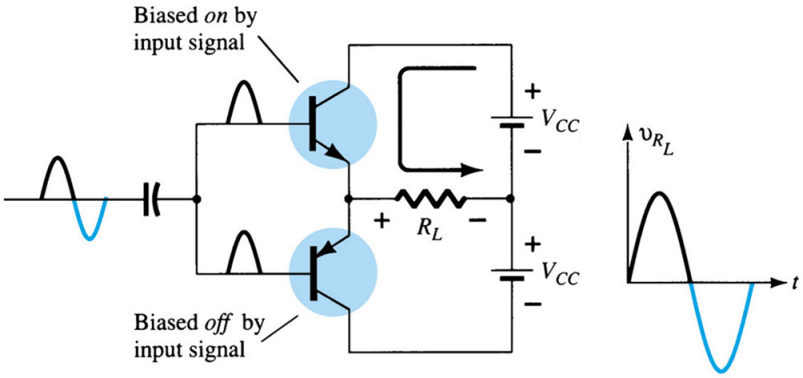


Figure 1.4.15: Operation on the positive half-cycle of the input

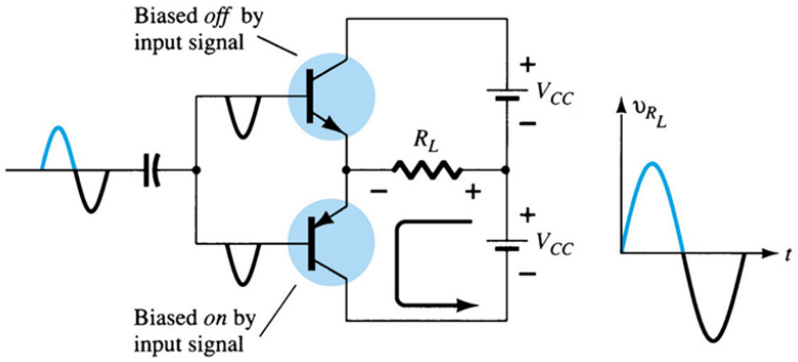


Figure 1.4.16: Operation on the negative half-cycle of the input

1.4.4.4 Power Input

The power supplied to the load by an amplifier is drawn from the power supply (or power supplies) that provides the input or dc power. The amount of this input power can be calculated using

$$P_{CC} = V_{CC} I_{CC}$$

where I_{CC} is the average or DC current drawn from the power supplies. In Class B operation, the current drawn from a single power supply has the form of a full-wave rectified signal, while that drawn from two power supplies has the form of a half-wave rectified signal from each supply. In either case, the value of the average current drawn can be expressed as

$$I_{CC} = \frac{2}{\pi} i_{o_{peak}} = \frac{2}{\pi} \frac{v_{o_{peak}}}{R_L} \tag{1.4.43}$$

where $i_{o_{peak}}$ and $v_{o_{peak}}$ are the peak values of the output current and voltage waveforms, respectively. Thus, the power input equation becomes

$$P_{CC} = \frac{2}{\pi} \frac{V_{CC}\, v_{o_{peak}}}{R_L} \tag{1.4.44}$$

1.4.4.5 Power Output

$$P_L = \frac{v_{o_{peak}}^2}{2R_L} \tag{1.4.45}$$

1.4.4.6 Efficiency

$$\begin{aligned} \eta\% &= \frac{P_L}{P_{CC}} \times 100 \\ &= \frac{v_{o_{peak}}^2/(2R_L)}{(2/\pi)(V_{CC}\, v_{o_{peak}}/R_L)} \times 100 && (1.4.46) \\ &= \frac{\pi}{4} \frac{v_{o_{peak}}}{V_{CC}} \times 100 && (1.4.47) \\ &= \frac{v_{o_{peak}}}{V_{CC}} \times 78.54 && (1.4.48) \end{aligned}$$

1.4.4.7 Transistor Power Dissipation

Power dissipated as heat across a transistor in a Class B push-pull configuration is given as

$$P_Q = \frac{1}{2}\left(P_{CC} - P_L\right) \tag{1.4.49}$$

$$= \frac{1}{2}\left(\frac{2}{\pi}\frac{V_{CC}\, v_{o_{peak}}}{R_L} - \frac{v_{o_{peak}}^2}{2R_L}\right) \tag{1.4.50}$$

$$= \frac{1}{\pi}\frac{V_{CC}\, v_{o_{peak}}}{R_L} - \frac{v_{o_{peak}}^2}{4R_L} \tag{1.4.51}$$

1.4.4.8 Maximum Efficiency

Maximum efficiency η_{max} is achieved at the maximum output power $P_{L(max)}$, i.e., at the maximum output swing

$$v_{o(max)_{peak}} = V_{CC}. \tag{1.4.52}$$

where each transistor provides half cycle of the output swing.

Thus, maximum efficiency η_{max} is given as

$$\eta_{max}\% = \frac{P_{L(max)}}{P_{CC}|_{P_{L(max)}}} \times 100$$

$$= \frac{\pi}{4}\frac{v_{o(max)_{peak}}}{V_{CC}} \times 100 \qquad \ldots \text{ from (1.4.47)} \tag{1.4.53}$$

$$= \frac{\pi}{4}\frac{V_{CC}}{V_{CC}} \times 100 \tag{1.4.54}$$

$$= \frac{\pi}{4} \times 100 \tag{1.4.55}$$

$$= 78.54\%. \tag{1.4.56}$$

1.4.4.9 Figure of Merit

Let us find the value of $v_{o_{peak}}$in (1.4.51) to give the maximum transistor power dissipation $P_{Q(max)}$ as follows

$$\left.\frac{dP_Q}{dv_{o_{peak}}}\right|_{P_{Q(max)}} = 0 \tag{1.4.57}$$

$$\frac{V_{CC}}{\pi} - \frac{v_{o_{peak}}}{2} = 0 \tag{1.4.58}$$

$$v_{o_{peak}}\Big|_{P_{Q(max)}} = \frac{2}{\pi}V_{CC}. \tag{1.4.59}$$

Substituting (1.4.59) in (1.4.51) we obtain $P_{Q_{max}}$ as follows

$$P_{Q(max)} = \frac{1}{\pi^2}\frac{V_{CC}^2}{R_L}. \tag{1.4.60}$$

Using (1.4.45) and (1.4.52), we obtain the maximum output power as

$$P_{L(max)} = \frac{V_{CC}^2}{2R_L}.$$

Thus, figure of merit (FoM) is given as

$$\text{FoM} = \frac{P_{Q(max)}}{P_{L(max)}} \tag{1.4.61}$$

$$= \frac{V_{CC}^2/(\pi^2 R_L)}{V_{CC}^2/(2R_L)} \tag{1.4.62}$$

$$= \frac{2}{\pi^2} \tag{1.4.63}$$

$$\cong \frac{1}{5}. \tag{1.4.64}$$

This FoM value is quite good. Because, if we want to deliver 10 W to the load, we only need to select **two** 2 W-transistors.

1.4.4.10 Crossover Distortion

One big disadvantage of the Class B amplifiers is the **crossover distortion** produced at the output as shown in below.

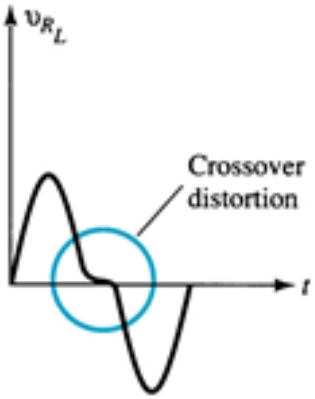


Figure 1.4.17: Cross-over distortion at the Class B amplifier output

Crossover distortion refers to the fact that during the signal crossover from positive to negative (or vice versa) there is some nonlinearity in the output signal. This results from the fact that transistor turn-on voltage is not actually zero volts, i.e., $V_{BE(ON)} \neq 0\,\text{V}$. Input voltage $v_i(t)$ itself turns the transistors ON and OFF. So, during the time when the magnitude of the input signal is less than the turn-on voltage, i.e., $|v_i(t)| < V_{BE(ON)}$, **both** transistors are **OFF** producing zero output and causing the crossover distortion.

Biasing the transistors just to the turn-on level $V_{BEQ} \cong V_{BE(ON)}$, will be the solution. However, this DC biasing causes static power dissipation, even when there is no AC input. So, the amplifier now becomes a **Class AB amplifier**.

1.4.5 Class AB Amplifiers

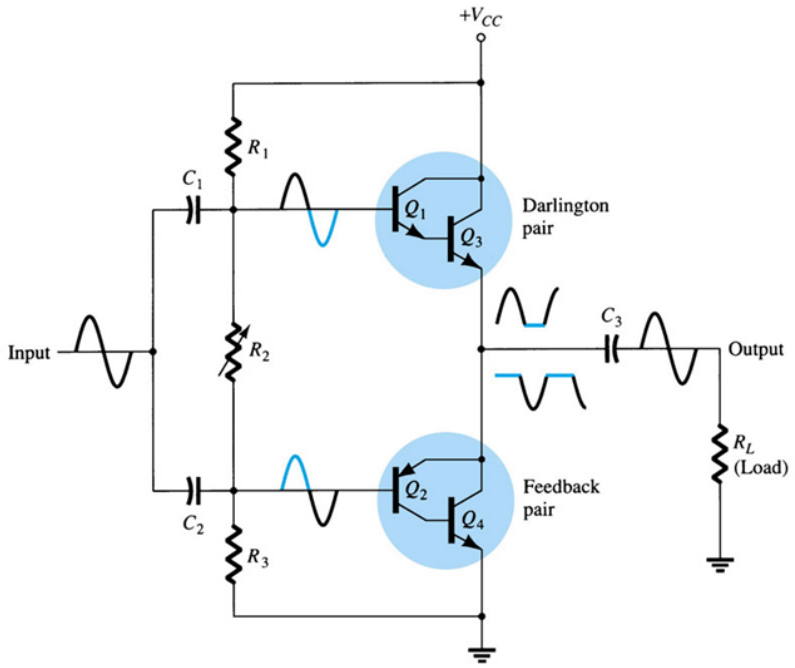


Figure 1.4.18: Quasi-complementary push-pull Class AB power amplifier

Notice that transistors Q_1 and Q_3 in Figure 1.4.18 form a Darlington connection that provides output from a low-impedance emitter-follower. The connection of transistors Q_2 and Q_4 forms a feedback-pair, which similarly provides a low-impedance drive to the load. Resistor R_2 can be adjusted to minimize crossover distortion by adjusting the DC bias condition. The single input signal applied to the push-pull stage then results in a full cycle output to the load. The quasi-complementary push-pull amplifier is presently the most popular form of power amplifier. The voltage across over R_2 is adjusted to provide turn-on voltages for the Darlington and feedback pairs, i.e.,

$$V_{R_2} \cong \frac{R_2}{R_1 + R_2 + R_3} V_{CC} = 2V_{BE(ON)} + V_{EB(ON)} = 3V_{BE(ON)}. \tag{1.4.65}$$

Note that in this configuration we need the capacitor C_3 at the output, because the DC bias-level at that point is not zero, i.e., $V_{E_3} = V_{E_2} = \frac{V_{CC}-GND}{2} = \frac{V_{CC}}{2}$.

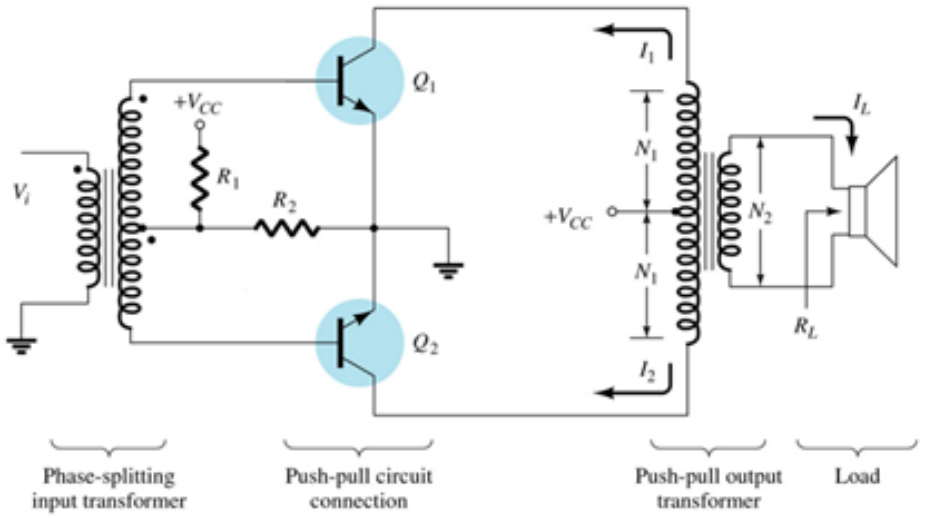


Figure 1.4.19: Transformer-coupled push-pull Class AB power amplifier.

Configuration in Figure 1.4.19 uses R_1 and R_2 resistors to bias the two transistors, as shown below

$$\frac{R_2}{R_1 + R_2} V_{CC} = V_{BE(ON)}. \tag{1.4.66}$$

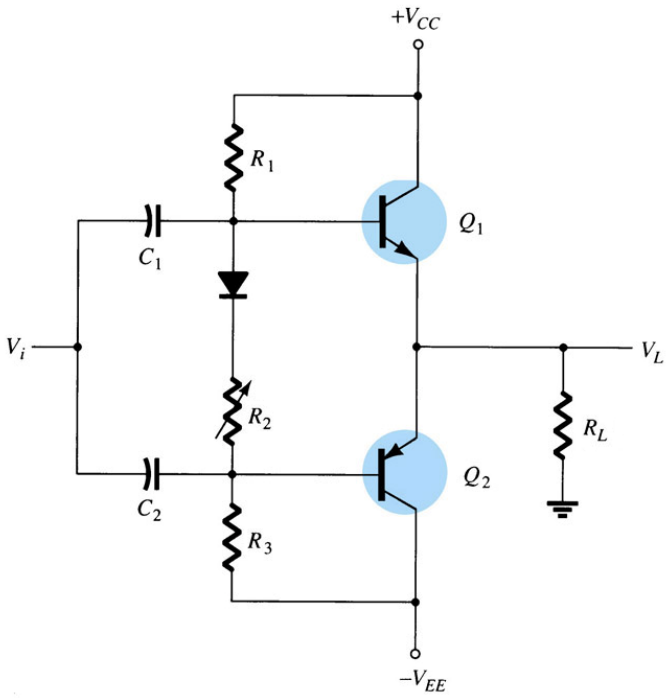


Figure 1.4.20: Complementary push-pull Class AB power amplifier

Configuration in Figure 1.4.20 uses a diode (matched to the Q_1 transistor, i.e., $V_{D(ON)} = V_{BE(ON)}$) and an adjustable R_3 resistor to bias the two transistors, as shown below

$$V_{R_2} \cong \frac{R_2}{R_1 + R_2 + R_3}\left(V_{CC} + V_{EE} - V_{D(ON)}\right) = V_{BE(ON)}. \tag{1.4.67}$$

As the diode is matched with one of the transistors, any changes on the turn-on voltage of this transistor will be compensated by the change in the turn-on voltage of the diode, e.g., changes due to temperature.

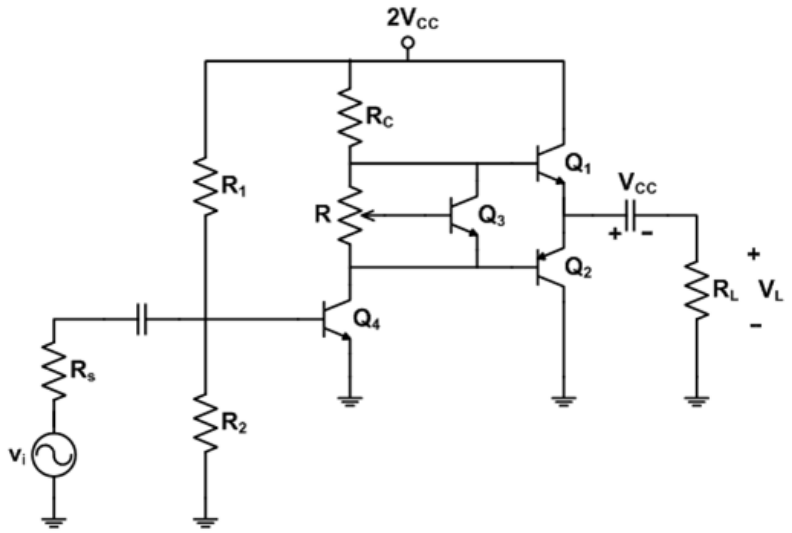


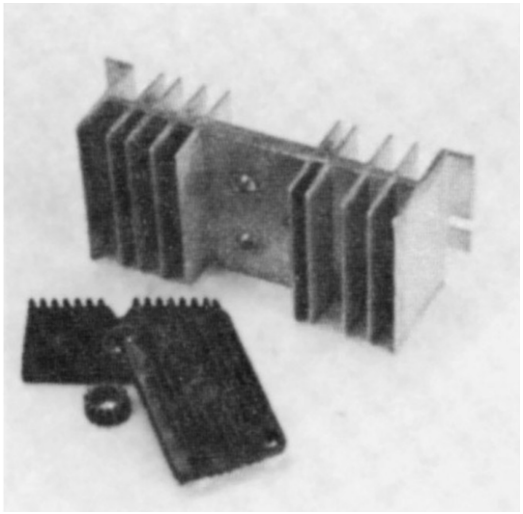
Figure 1.4.21: Another complementary push-pull Class AB power amplifier

Configuration in Figure 1.4.21 uses variable R resistor (or potentiometer) to bias the transistors. Note that, Q_3 transistor increases the turn-off speeds of the power transistors Q_1 and Q_2.

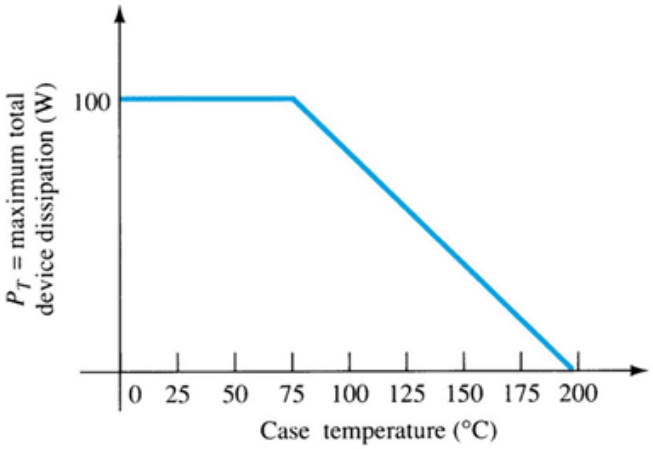
1.4.6 Power Transistor Heat Sinking

The maximum power handled by a particular device and the temperature of the transistor junctions are related since the power dissipated by the device causes an increase in temperature at the junction of the device. Rated power dissipation is allowed only up to a maximum temperature. Above this temperature, the device power dissipation capacity gets reduced (or derated), so that at higher case temperatures the power-handling capacity is reduced, down to 0 W at the device maximum case temperature. When the device is mounted on some form of heat sink, its power handling capacity can approach the rated maximum value more closely. A few heat sinks are shown in Figure 1.4.22(a). When the heat sink is used, the heat produced by the transistor dissipating power has a larger area from which to radiate (transfer) the heat into the air, thereby holding the case temperature to a much lower value than would result without the heat sink.

Figure 1.4.22(b) shows a typical power derating curve for a silicon transistor. The curve shows that the manufacturer will specify an upper temperature point, after which a linear derating takes place. For silicon, the maximum power that should be handled by the device does not reduce to 0 W until the case temperature is 200 °C.



(a)



(b)

Figure 1.4.22: Heat-related figures: (a) heat sinks, (b) a typical power derating curve.

1.4.6.1 Thermal-to-Electrical Analogy

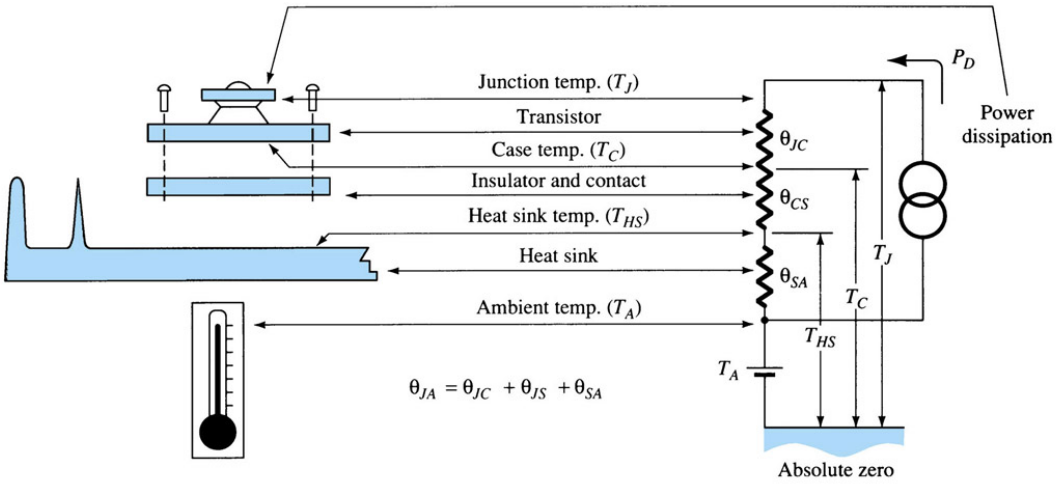


Figure 1.4.23: Thermal-to-electrical analogy.

A picture of how the junction temperature (T_J), case temperature (T_C), and ambient (air) temperature (T_A) are related by the device heat-handling capacity–a temperature coefficient usually called thermal resistance–is presented in the thermal-electric analogy shown in Figure 1.4.23.

In providing a thermal-electrical analogy, the term *thermal resistance* is used to describe heat effects by an electrical term. The terms in Figure 1.4.23 are defined as follows:

- θ_{JC} = transistor thermal resistance (junction to case)
- θ_{CS} = insulator thermal resistance (case to heat sink)
- θ_{SA} = heat-sink thermal resistance (heat sink to ambient)
- θ_{JA} = total thermal resistance (junction to ambient)

Using the electrical analogy for thermal resistances, we can write:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \tag{1.4.68}$$

The analogy can also be used in applying Kirchhoff's law to obtain:

$$T_J = P_D\theta_{JA} + T_A \tag{1.4.69}$$

The last relation shows that the junction temperature *floats* on the ambient temperature and that the higher the ambient temperature, the lower the allowed value of device power dissipation.

Example 1.14: A silicon power transistor is operated with a heat sink ($\theta_{SA} = 1.5\,^\circ\text{C/W}$). The transistor, rated at 150 W (25 °C), has $\theta_{JC} = 0.5\,^\circ\text{C/W}$, and the mounting insulation has $\theta_{CS} = 0.6\,^\circ\text{C/W}$. What maximum power can be dissipated if the ambient temperature is 40 °C and $T_{J_{max}} = 200\,^\circ\text{C}$?

Solution:

$$P_D = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} = \frac{200 - 40}{0.5 + 0.6 + 1.5} \approx 61.5\,\text{W}.$$

1.4.7 Class C Amplifiers

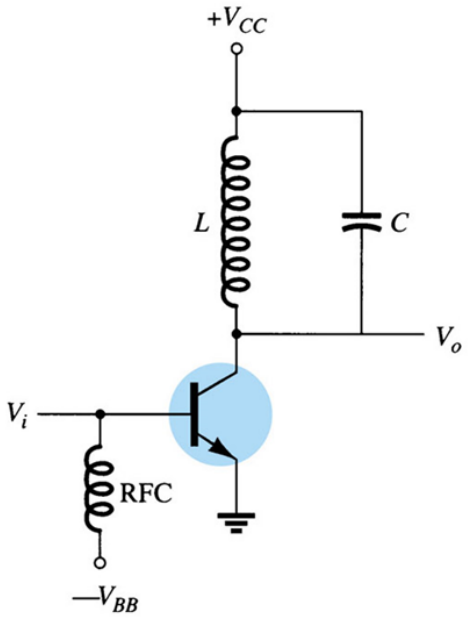


Figure 1.4.24: Class C amplifier circuit.

A Class C amplifier, as that shown in Figure 1.4.24, is biased to operate for less than 180° of the input signal cycle. The tuned circuit in the output, however, will provide a full cycle of output signal for the fundamental or resonant frequency of the tuned circuit (L and C tank circuit) of the output. This type of operation is therefore limited to use at one fixed frequency, as occurs in a **communications** circuit, for example.

Operation of a Class C circuit is **not intended** for large-signal or power amplifiers.

1.4.8 Class D Amplifiers

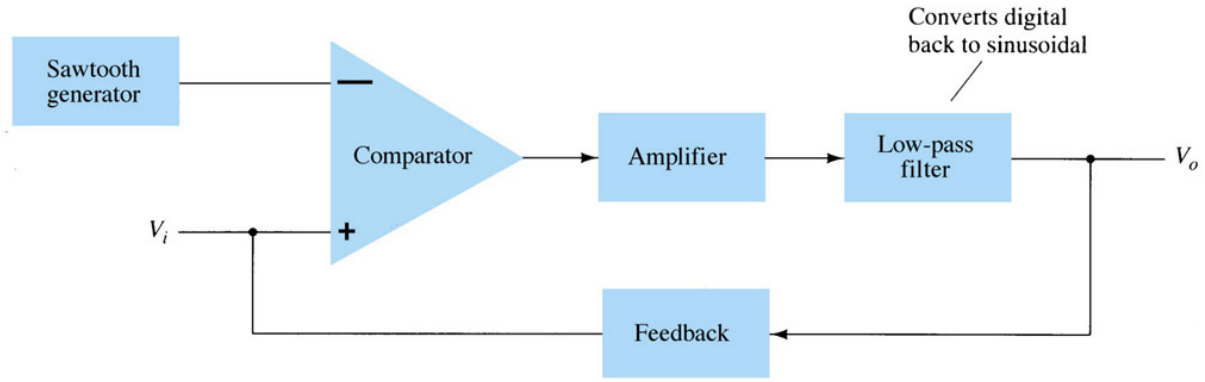


Figure 1.4.25: Block diagram of a Class D amplifier.

A Class D amplifier is designed to operate with digital or pulse-type signals in a configuration shown in Figure 1.4.25. An efficiency of over 90% is achieved using this type of circuit, making it quite desirable in power amplifiers. It is necessary, however, to convert any input signal into a pulse-type waveform before using it to drive a large power load and to convert the signal back to a sinusoidal-type signal to recover the original signal. Figure 1.4.26 shows how a sinusoidal signal may be converted into a pulse-type signal using some form of sawtooth or chopping waveform to be applied with the input into a comparator-type op-amp circuit so that a representative pulse-type signal is produced.

Figure 1.4.25 shows a block diagram of the unit needed to amplify the Class D signal and then convert back to the sinusoidal-type signal using a low-pass filter. Since the amplifier's transistor devices used to provide the output are basically either off or on, they provide current only when they are turned on. Since most of the power applied to the amplifier is transferred to the load, the efficiency of the circuit is typically very high. Power MOSFET devices have been quite popular as the driver devices for the Class D amplifier.

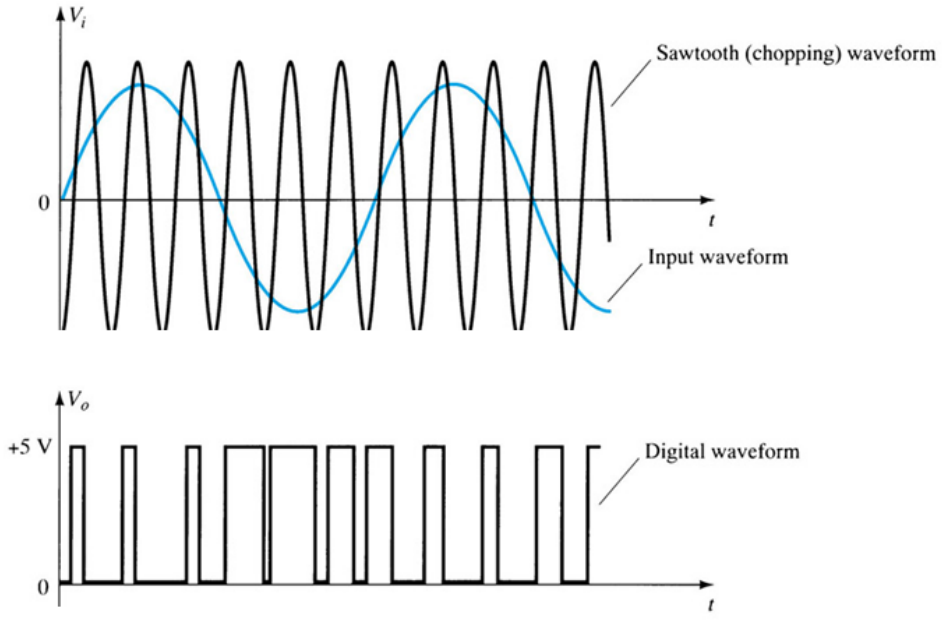


Figure 1.4.26: Chopping of sinusoidal waveform to produce digital waveform.

Example 1.15: (2005-2006 MII) Consider the amplifier circuits given in the figures belowwhere $V_{BE(ON)} = 0.7\,\text{V}$.

For the circuit shown in Fig-A with $v_i = 1\,\text{V}\sin(\omega t)$

a) Draw v_o,

b) Calculate the power P_L dissipated over R_L,

c) Calculate the efficiency of the power amplifier consisting of transistors Q_1 and Q_2.

For the circuit shown in Fig-B with $v_i = 1\,\text{V}\sin(\omega t)$

d) Draw v_o,

e) Compare the two amplifier circuit designs given in Fig-A and Fig-B, and express which design is more preferable. Briefly explain your answer.

HINT: Consider your answers to items "a)" and "d)".

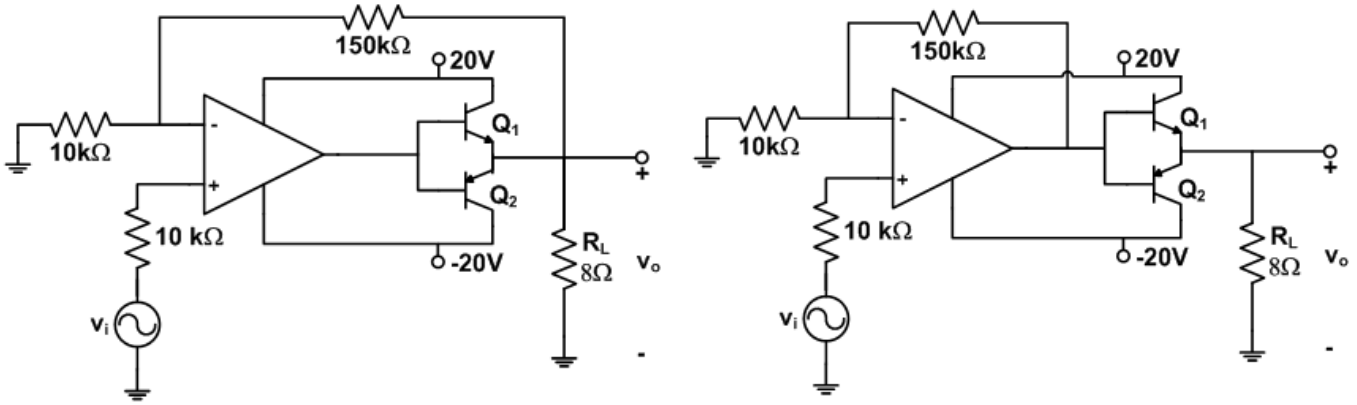


Fig-A Fig-B

Figure 1.4.27: Power amplifier circuits for Example 1.15.

Solution: a) We can calculate the voltage gain A_v as

$$A_v = \frac{v_o}{v_i} = 1 + \frac{150k}{10k} = 16.$$

So, the output v_o is given by

$$v_o = A_v v_i = 16\,\text{V}\sin(\omega t).$$

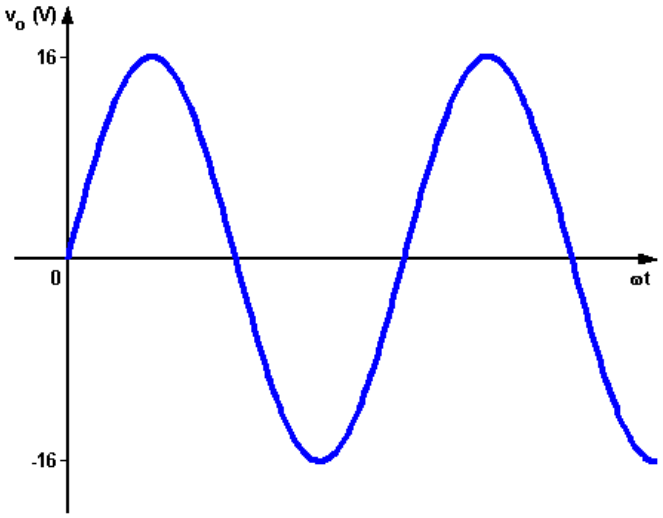


Figure 1.4.28: Output for the circuit of Fig-A in Figure 1.4.27.

b) $P_L = \dfrac{v_{o(peak)}^2}{2R_L} = \dfrac{16^2}{2(8)} = 16\,\text{W}$

c) As we know the output power let us calculate the total power P_{CC} drawn from the voltage supplies

$$\begin{aligned} P_{CC} &= V_{CC} I_{CC} \\ &= V_{CC} \frac{2}{\pi} \frac{v_{o(peak)}}{R_L} \\ &= 20 \frac{2}{\pi} \frac{16}{8} \\ &= 25.465\,\text{W}. \end{aligned}$$

Now, efficiency η is given by

$$\begin{aligned} \eta\% &= \frac{P_L}{P_{CC}} \times 100 \\ &= \frac{16}{25.465} \times 100 \\ &= 62.83\%. \end{aligned}$$

d) There is a cross-over distortion at the output due to the 0.7 V turn-on voltage drop across the base-emitter junctions of the transistors Q_1 and Q_2. So, the output v_o of Fig-B will be plotted as below

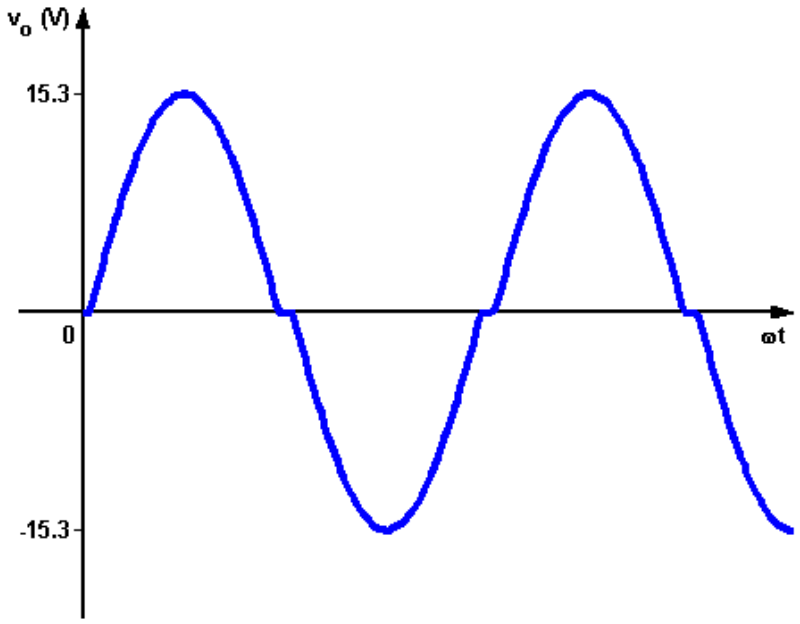


Figure 1.4.29: Output for the circuit of Fig-B in Figure 1.4.27.

e) In Fig-B, Class B power amplifier (in a complementary push-pull structure) is connected after a pre-amplifier stage consisting of a non-inverting opamp amplifier. This complementary push-pull Class B amplifier configuration acts like a voltage-buffer amplifier (i.e. like an emitter-follower).

However the complementary (*npn-pnp*) BJT amplifiers turn-on when sufficient voltage difference($\geq$ 0.7 V) exists between their base-emitter terminals (BE-EB). Q_1 is ON at the positive-half cycle when $(V_{B_1}V_{E_1}) \geq 0.7\,\text{V}$ and similarly Q_2 is ON at the negative-half cycle when $(V_{B_2}V_{E_2}) \leq -0.7\,\text{V}$.

Due to this 0.7 V turn-on voltage drop across the base-emitter junctions of the complementary BJT transistors, we observe a **cross-over distortion** at the output of Fig-B as shown in the answer of item “d)".

In Fig-A, negative feedback is connected to the output of the power amplifier eliminating the cross-over distortion by enforcing the suitable biasing voltage at the transistor bases. So, the configuration in **Fig-A** is **more preferable** to the configuration in Fig-B.

1.5 Oscillators

How the feedback circuit provides operation as an oscillator is obtained by noting the denominator in the basic **negative feedback** equation(1.1.20),

$$A_f(\omega) = \frac{A(\omega)}{1 + \beta(\omega)A(\omega)}. \tag{1.5.1}$$

When $\beta(\omega)A(\omega) = -1$ or magnitude 1 at a phase angle of 180°, the denominator becomes 0 and the gain with feedback, $A_f(\omega)$, becomes infinite. Thus, an infinitesimal signal (noise voltage) can provide a measurable output voltage, and the circuit will be unstable and have oscillations. So, this criterion

$$\beta(\omega)A(\omega) = -1 \tag{1.5.2}$$

is known as the **Barkhausen criterion** for oscillation.

If we have the negative feedback loop-gain βA to be -1 only at a single frequency, i.e.,

$$\boxed{\beta(\omega_0)A(\omega_0) = -1,} \tag{1.5.3}$$

then we will have oscillations only at $\omega = \omega_0$.Thus, this circuit will act as an oscillator even without an input signal (noise in the circuit acts as an input signal), will be called an **oscillator circuit** where it produces a signal only at the frequency of $\omega = \omega_0$.

To understand how a feedback circuit performs as an oscillator, consider the **positive feedback** circuit Figure 1.5.1 below.

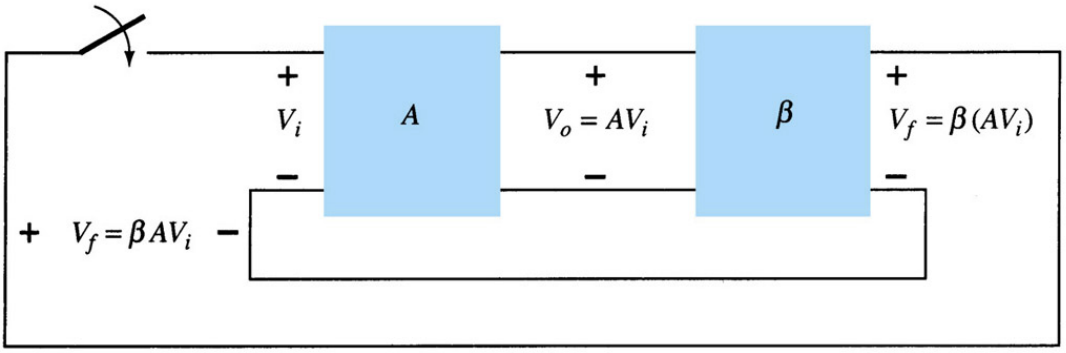


Figure 1.5.1: Positive feedback circuit used as an oscillator.

When the switch at the amplifier input is open, no oscillation occurs. Consider that we have a fictitious voltage at the amplifier input, v_i. This results in an output voltage $v_o = Av_i$ after the amplifier stage and in a voltage $v_f = \beta Av_i$ after the feedback stage.Thus, we have a feedback voltage $v_f = \beta Av_i$, where βA is referred to as the **loop-gain**. If the circuits of the base amplifier and feedback network provide βA of a correct magnitude and phase, v_f can be made equal to v_i. Then, when the switch is closed and fictitious voltage v_i is removed, the circuit will continue operating since the feedback voltage is sufficient to drive the amplifier and feedback circuits resulting in a proper input voltage to sustain the loop operation. The output waveform will still exist after the switch is closed if the condition $\beta A = 1$ is met.

In reality, no input signal is needed to start the oscillator going. Only the condition $\beta A = 1$ must be satisfied for self-sustained oscillations to result. In practice, βA is made greater than 1 and

the system is started oscillating by amplifying **noise voltage**, which is always present. Saturation factors in the practical circuit provide an average value of $\beta A = 1$. The resulting waveforms are never exactly sinusoidal. However, the closer the value βA is to exactly 1, the more nearly sinusoidal is the waveform.

Figure 1.5.2 below shows how the noise signal results in a buildup of a steady-state oscillation condition.

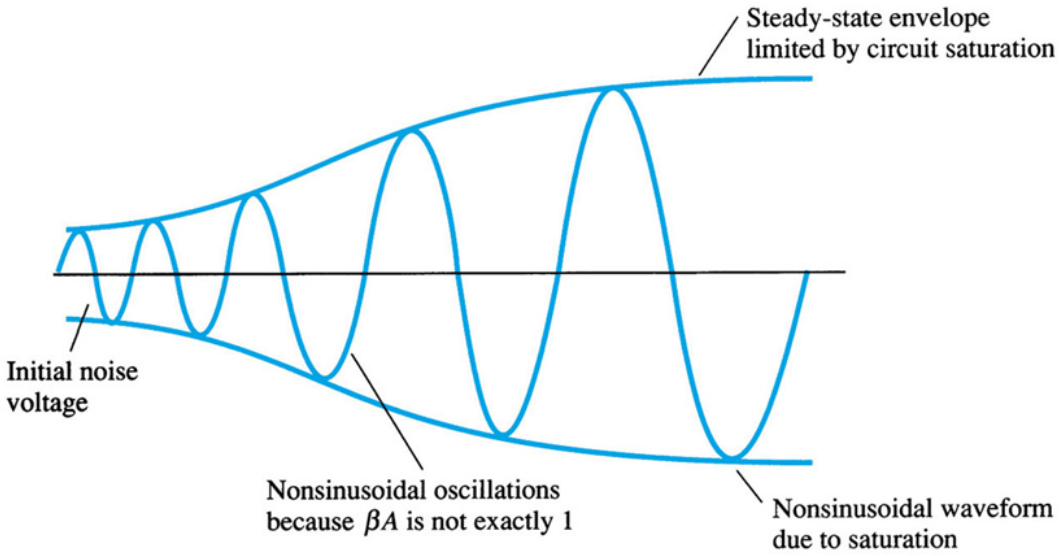


Figure 1.5.2: Build-up of steady-state oscillations.

1.5.1 Types of Oscillator Circuits

Main classes of oscillator circuits are given below

1. Phase-Shift Oscillator
2. Wien-Bridge Oscillator
3. Tuned Oscillator Circuits
4. Crystal Oscillator
5. Unijunction Oscillator

1.5.2 Phase-Shift Oscillator

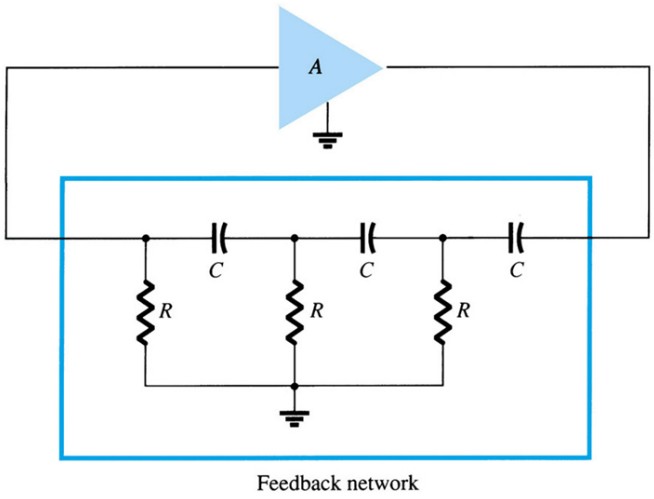


Figure 1.5.3: Idealized phase-shift oscillator.

- In this configuration (where A is **negative**), feedback gain is given by

$$\beta(\omega) = \frac{1}{1 - 5\alpha^2 - j\,(6\alpha - \alpha^3)} \tag{1.5.4}$$

where $\alpha = 1/(\omega RC)$. The oscillation occurs at a frequency ω_0 where $\angle\beta(\omega_0) = 180°$.

Thus, the oscillation frequency f_0 which cancels the imaginary part is given by

$$\boxed{f_0 = \frac{1}{2\pi RC\sqrt{6}}} \tag{1.5.5}$$

- As $\alpha|_{\omega_0} = \sqrt{6}$, feedback gain at the oscillation frequency is given by

$$\beta(\omega_0) = -\frac{1}{29} \tag{1.5.6}$$

The amplifier must supply enough gain to compensate for losses. The overall gain must be unity. Thus, the absolute gain of the amplifier stage must be greater than $|1/\beta(\omega_0)|$, i.e.,

$$\boxed{|A| > 29.} \tag{1.5.7}$$

- The RC networks provide the necessary phase shift for a positive feedback. They also determine the frequency of oscillation.

1.5.2.1 FET Phase-Shift Oscillator

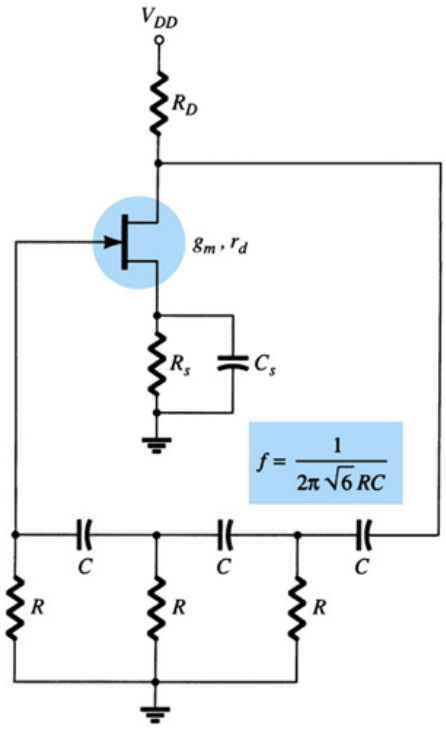


Figure 1.5.4: FET phase-shift oscillator.

Example 1.16: It is desired to design phase-shift oscillator(as in Figure 1.5.4) using an FET having $g_m = 5\,\text{mS}$, $r_{ds} = 40\,\text{k}\Omega$, and feedback circuit resistor value of $R = 10\,\text{k}\Omega$. Select the value of C for oscillator operation at $1\,\text{kHz}$ and R_D for $A > 29$ to ensure oscillator operation.

Solution: Since $f_0 = \frac{1}{2\pi RC\sqrt{6}}$, we can solve for C as follows

$$\begin{aligned} C &= \frac{1}{2\pi f_0 R\sqrt{6}} = \frac{1}{2\pi(1k)(10k)\sqrt{6}} \\ &= 6.5\,\text{nF}. \end{aligned}$$

Next, we solve for R'_D where $R'_D = r_{ds}||R_D$ to provide a gain of $A = 40$ (this allows for some loading between R'_D and the feedback network input impedance):

$$\begin{aligned} |A| &= g_m R'_D = 40 \\ R'_D &= \frac{|A|}{g_m} = \frac{40}{5 \times 10^{-3}} = 8\,\text{k}\Omega. \end{aligned}$$

Finally, we solve for R_D to be

$$R_D = \frac{r_{ds}R'_D}{r_{ds} - R'_D} = 10\,\text{k}\Omega.$$

1.5.2.2 BJT Phase-Shift Oscillator

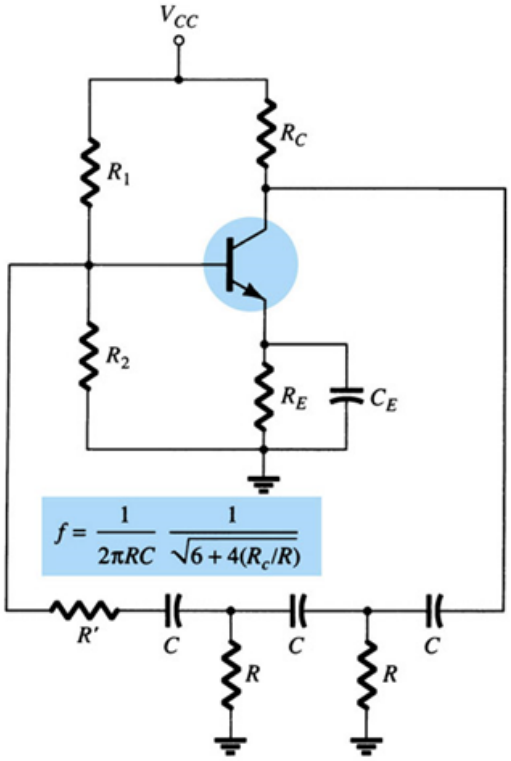


Figure 1.5.5: BJT phase-shift oscillator.

In Figure 1.5.5 above:

$$R' = R - R_i = R - R_1||R_2||h_{ie}$$

.

For the loop-gain to be greater than unity, the requirement on the current gain of the transistor is found to be

$$h_{fe} > 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}. \tag{1.5.8}$$

1.5.2.3 Opamp Phase-Shift Oscillator

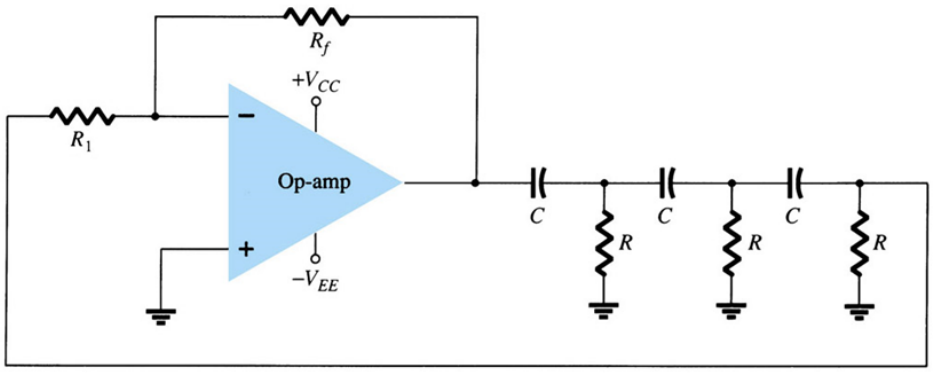


Figure 1.5.6: Op-amp phase-shift oscillator.

In Figure 1.5.6 above, in order to sustain oscillation, i.e., $\beta(\omega_0)A(\omega_0) \geq 1$ we need to have

$$\frac{R_f}{R_1} \geq 29 \tag{1.5.9}$$

.

1.5.3 Wien-Bridge Oscillator

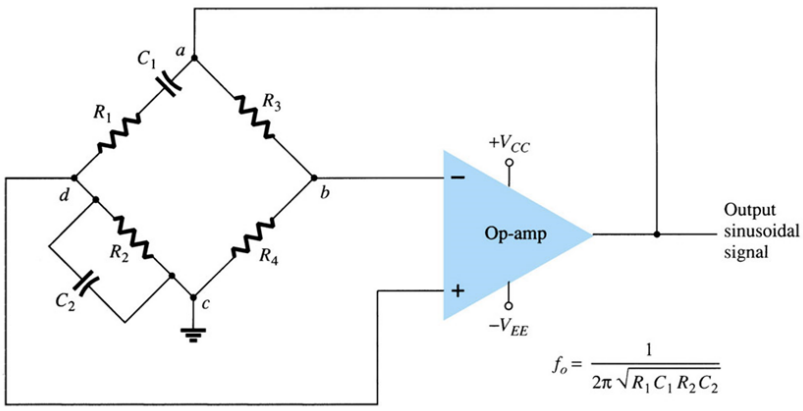


Figure 1.5.7: Wien-bridge oscillator circuit using op-amp amplifier.

Let us first define $Z_1 = R_1 + Z_{C_1}$ and $Z_2 = R_2 || Z_{C_2}$.

- Then, the positive feedback loop-gain is given as

$$\beta(\omega)A(\omega) = \underbrace{\frac{Z_2}{Z_1 + Z_2}}_{\beta(\omega)} \underbrace{\left(1 + \frac{R_3}{R_4}\right)}_{A(\omega)} = \frac{1}{1 + Z_1/Z_2}\left(1 + \frac{R_3}{R_4}\right) \tag{1.5.10}$$

In order to have the loop-gain to be 1, the Z_1/Z_2 needs to have **zero phase**, i.e., imaginary part needs to be zero. Thus, the oscillation frequency f_0 is found to be

$$\boxed{f_0 = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}} \tag{1.5.11}$$

- Hence, the positive feedback loop-gain at the oscillation frequency f_0 becomes

$$\beta(\omega_0)A(\omega_0) = \frac{1}{1 + \left(\frac{R_1}{R_2} + \frac{C_2}{C_1}\right)}\left(1 + \frac{R_3}{R_4}\right) \tag{1.5.12}$$

In order to sustain the oscillation, i.e., $\beta(\omega_0)A(\omega_0) \geq 1$,

$$\boxed{\frac{R_3}{R_4} \geq \frac{R_1}{R_2} + \frac{C_2}{C_1}} \tag{1.5.13}$$

- Thus, when $R_1 = R_2 = R$ and $C_1 = C_2 = C$, then

$$f_0 = \frac{1}{2\pi RC} \tag{1.5.14}$$

$$\frac{R_3}{R_4} \geq 2. \tag{1.5.15}$$

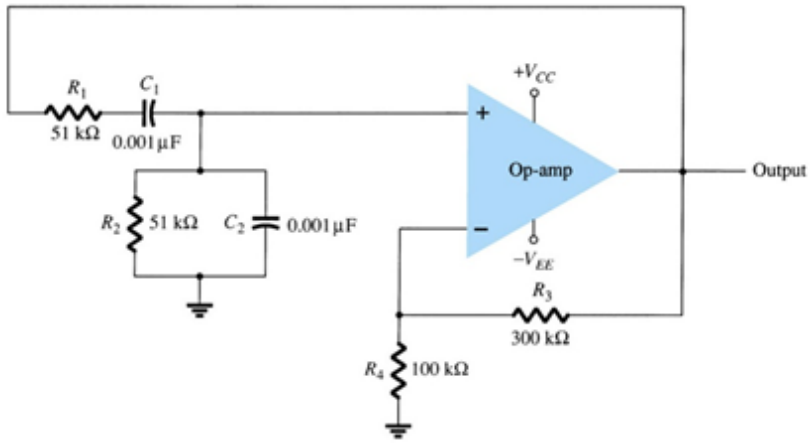


Figure 1.5.8: Wien-bridge oscillator circuit for Example 1.16.

Example 1.17: Calculate the resonant frequency of the Wien bridge oscillator shown in Figure 1.5.8 above.

Solution: Oscillation frequency is given by

$$f_0 = \frac{1}{2\pi RC} = \frac{1}{2\pi(51k)(1n)} = 3120.7\,\text{Hz}.$$

Example 1.18: Design the RC elements of a Wien bridge oscillatoras in Figure 1.5.7 for operation at $f_0 = 10\,\text{kHz}$.

Solution: Using equal values of R and C, we can select $R = 100\,\text{k}\Omega$ and calculate the required value of C as

$$C = \frac{1}{2\pi f_0 R} = \frac{1}{2\pi(10k)(100k)} = 159\,\text{pF}.$$

We can use $R_3 = 300\,\text{k}\Omega$ and $R_4 = 100\,\text{k}\Omega$ to provide a ratio R_3/R_4 greater than 2 for oscillation to take place.

1.5.4 Tuned Oscillator Circuits

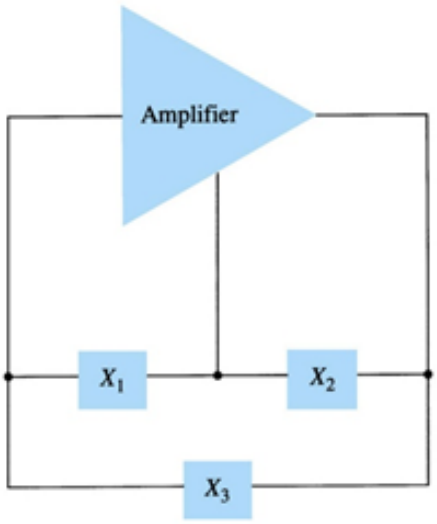


Figure 1.5.9: Basic configuration of tuned (or resonant) circuit oscillator.

	Reactance Element		
Oscillator Type	X_1	X_2	X_3
Colpitts oscillator	C	C	L
Hartley oscillator	L	L	C
Tuned input, tuned output	LC	LC	—

Figure 1.5.10: Resonant element selection for a tuned oscillator

Tuned Oscillators use a parallel LC resonant circuit (LC-tank) to provide the oscillations.

There are two common types:

- **Colpitts:** The resonant circuit is an inductor and two capacitors.
- **Hartley:** The resonant circuit is a tapped inductor or two inductors and one capacitor.

1.5.4.1 Colpitts Oscillator Circuits

FET Colpitts Oscillator

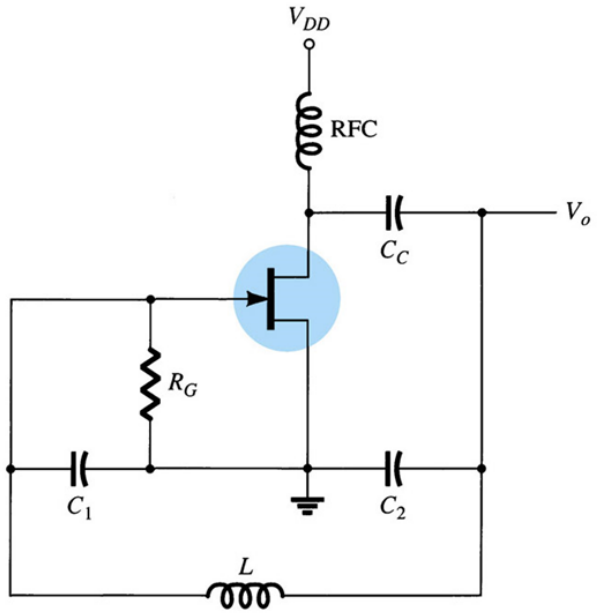


Figure 1.5.11: FET Colpitts Oscillator.

Oscillator frequency

$$\boxed{f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}} \tag{1.5.16}$$

where $C_{eq} = \dfrac{C_1 C_2}{C_1 + C_2}$.

BJT Colpitts Oscillator

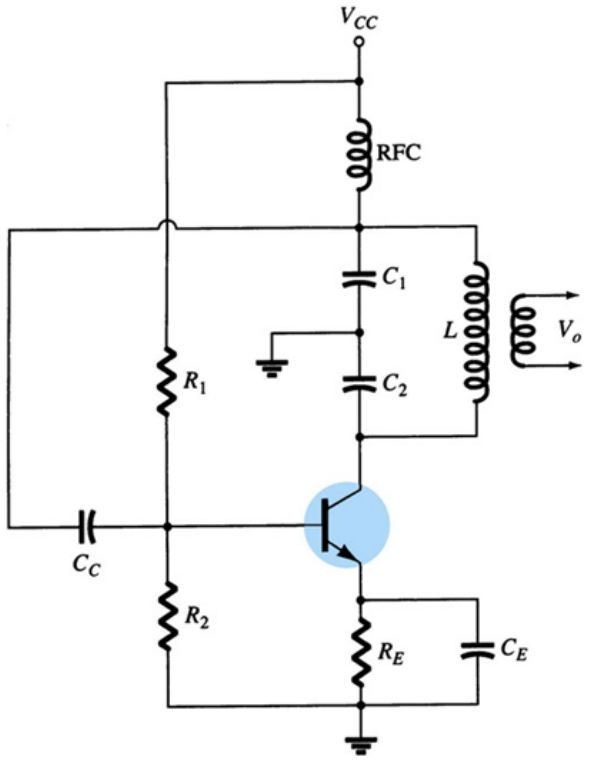


Figure 1.5.12: BJT Colpitts Oscillator.

Opamp Colpitts Oscillator

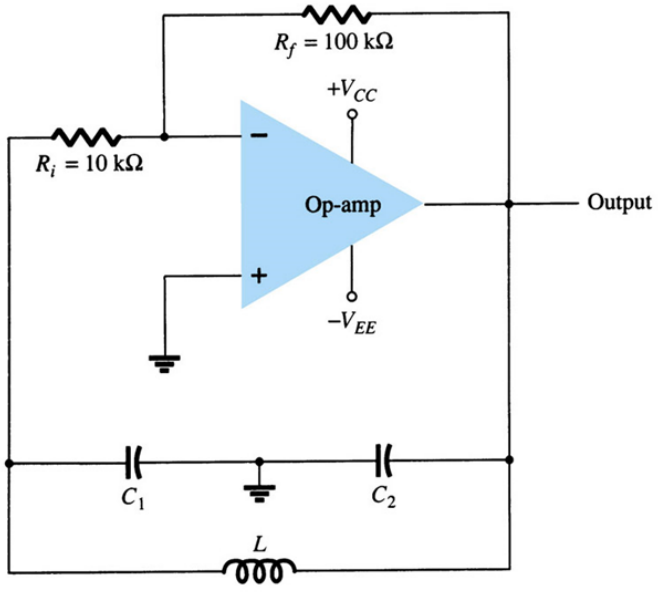


Figure 1.5.13: Op-amp Colpitts Oscillator.

1.5.4.2 Hartley Oscillator Circuits

FET Hartley Oscillator

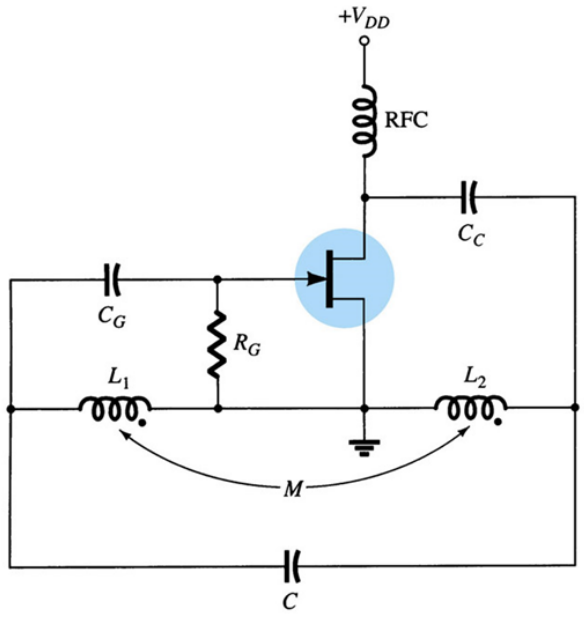


Figure 1.5.14: FET Hartley Oscillator.

Oscillator frequency

$$\boxed{f_0 = \frac{1}{2\pi\sqrt{L_{eq}C}}} \tag{1.5.17}$$

where $L_{eq} = L_1 + L_2 + 2M$ with M denoting the mutual inductance.

BJT Hartley Oscillator

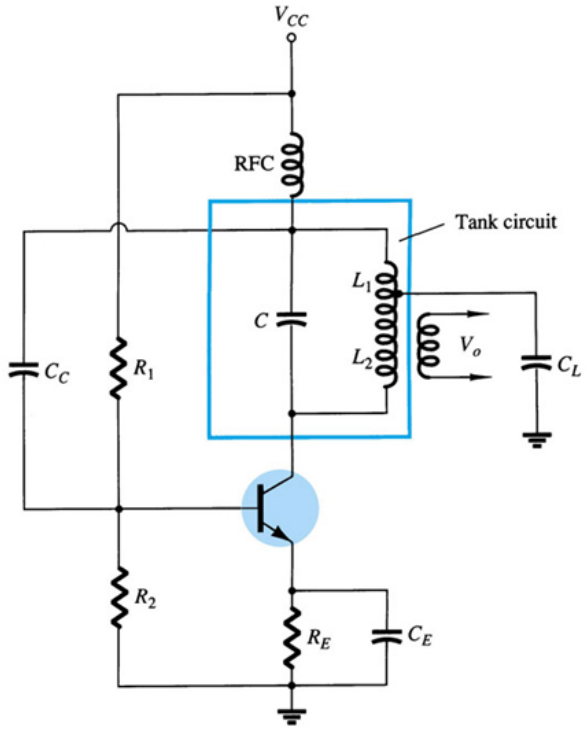


Figure 1.5.15: BJT Hartley Oscillator.

1.5.5 Crystal Oscillator

A crystal oscillator is basically a tuned-circuit oscillator using a piezoelectric crystal as a resonant tank circuit. The crystal (usually quartz) has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate. Crystal oscillators are used whenever great stability is required, such as in communication transmitters and receivers.

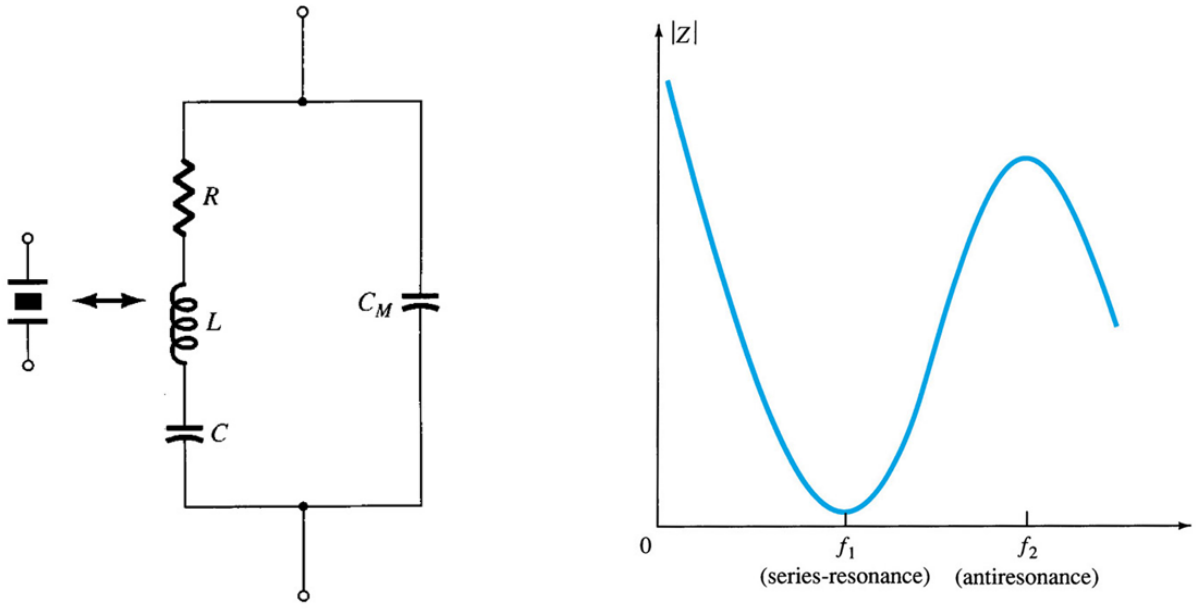
A **quartz** crystal (one of a number of crystal types) exhibits the property that when mechanical stress is applied across the faces of the crystal, a difference of potential develops across opposite faces of the crystal. This property of a crystal is called the **piezoelectric effect**. Similarly, a voltage applied across one set of faces of the crystal causes mechanical distortion in the crystal shape.

When alternating voltage is applied to a crystal, mechanical vibrations are set up. These vibrations having a natural resonant frequency dependent on the crystal. Although the crystal has electromechanical resonance, we can represent the crystal action by an equivalent **electrical resonant circuit**as shown in Figure 1.5.16(a). The inductor L and capacitor C represent electrical equivalents of crystal mass and compliance, while resistance R is an electrical equivalent of the crystal structure's internal friction. The shunt capacitance C_M represents the capacitance due to mechanical mounting of the crystal. Because the crystal losses, represented by R, are small, the equivalent crystal Q-value (quality factor) is high (typically 20000). Values of Q up to almost 10^6 can be achieved by using crystals.

The crystal has two resonant frequencies as shown in Figure 1.5.16(b):

- **Series resonant:** RLC determine the resonant frequency. The crystal has a low impedance.
- **Parallel resonant:** RL and C_M determine the resonant frequency. The crystal has a high impedance.

The series and parallel resonant frequencies are very close, within 1% of each other.



(a) (b)

Figure 1.5.16: Crystal operation: (a) electrical equivalent circuit, (b) crystal impedance versus frequency.

Series-Resonant Crystal FET Oscillator

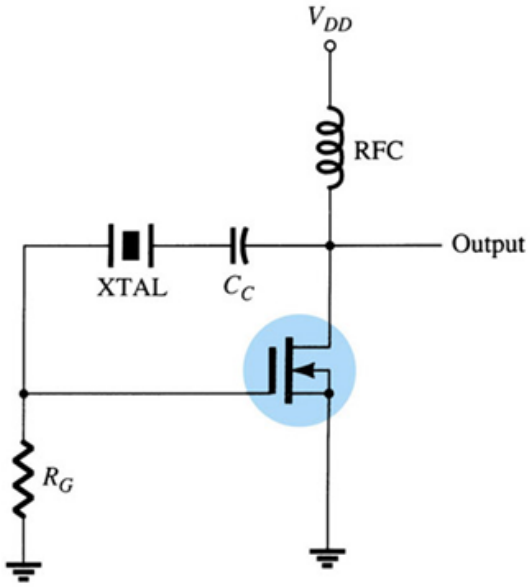


Figure 1.5.17: Crystal-controlled FET oscillator circuit using crystal in series-feedback path.

Series-Resonant Crystal Opamp Oscillator

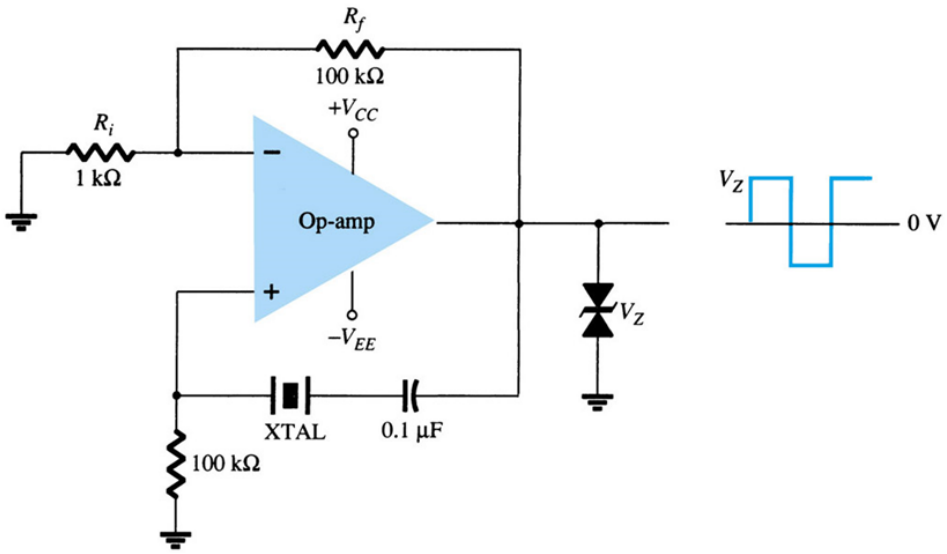


Figure 1.5.18: Crystal-controlled Opamp oscillator circuit using crystal in series-feedback path.

Parallel-Resonant Crystal BJT Oscillator

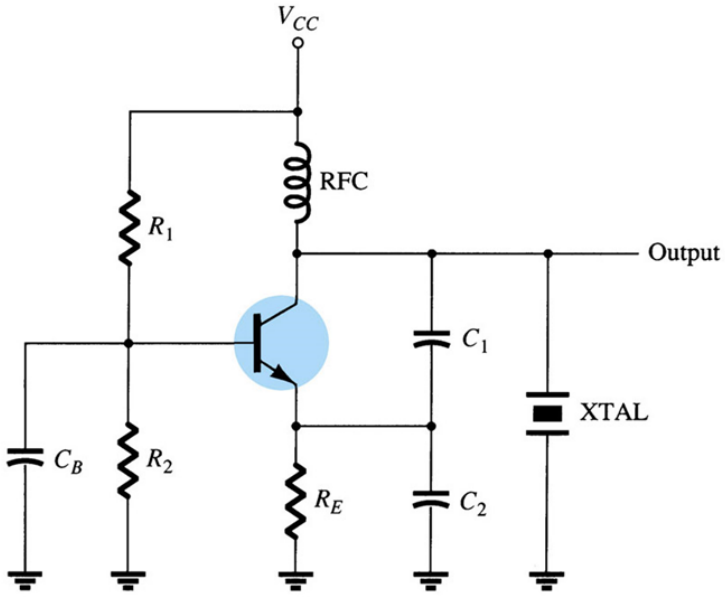


Figure 1.5.19: Crystal-controlled BJT oscillator operating in parallel-resonant mode.

1.5.6 Unijunction Oscillator

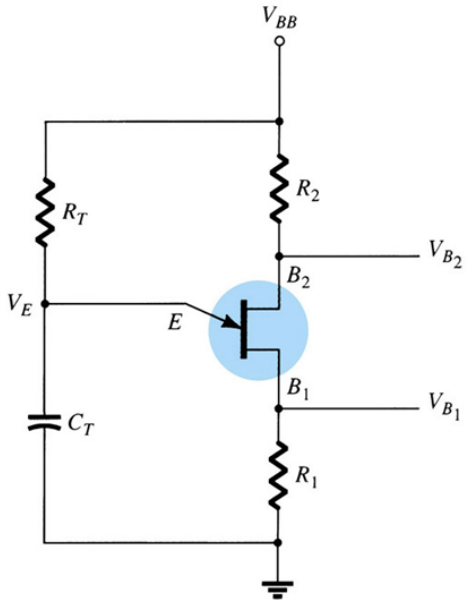


Figure 1.5.20: Basic unijunction oscillator circuit.

Unijunction transistor (UJT) can be used in a single-stage oscillator circuit to provide a **pulse signal** suitable for digital-circuit applications.

The unijunction transistor can be used in what is called a **relaxation oscillator** as shown by the basic circuit in Figure 1.5.20 above. Resistor R_T and capacitor C_T are the timing components that set the circuit oscillating rate.

The oscillating frequency may be calculated as

$$f_0 = \frac{1}{R_T C_T \ln\left(\frac{1}{1-\eta}\right)} \tag{1.5.18}$$

where η is the unijunction transistor intrinsic stand-off ratio.

Typically, a unijunction transistor has a stand-off ratio from 0.4 to 0.6, i.e., $0.4 \leq \eta \leq 0.6$. Using a value of $\eta = 0.5$ gives us

$$f_0 \cong \frac{1.5}{R_T C_T} \tag{1.5.19}$$

Capacitor C_T is charged through resistor R_T toward supply voltage V_{BB}. As long as the capacitor voltage V_E is below a stand-off voltage (V_P) given by

$$V_P = \eta\left(V_{B_2} - V_{B_1}\right) + V_{B_1} + V_{D(ON)} \cong \eta V_{BB} + V_{D(ON)} \tag{1.5.20}$$

the unijunction emitter lead appears as an open circuit. When the emitter voltage across capacitor C_T exceeds this value (V_P), the unijunction circuit fires, discharging the capacitor, after which a new charge cycle begins.

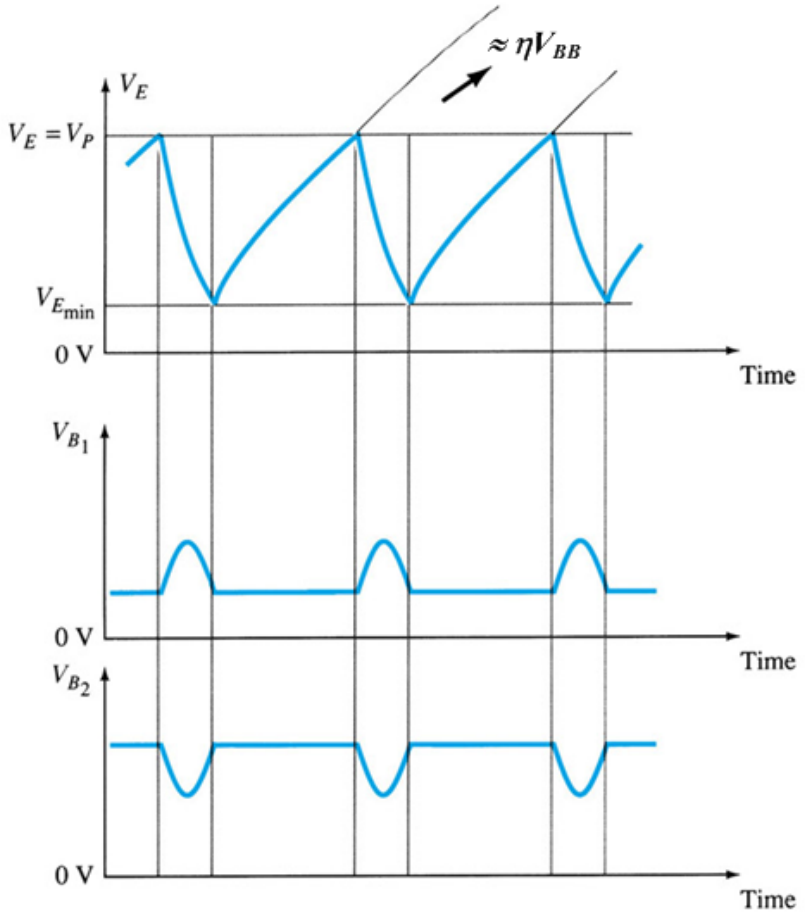


Figure 1.5.21: Unijunction oscillator waveforms.

When the unijunction fires, a voltage rise is developed across R_1 and a voltage drop is developed across R_2 as shown in Figure 1.5.21 above. The signal at the emitter is a **sawtooth voltage** waveform that at B_1 is a **positive-going pulse** and at B_2 is a **negative-going pulse**.

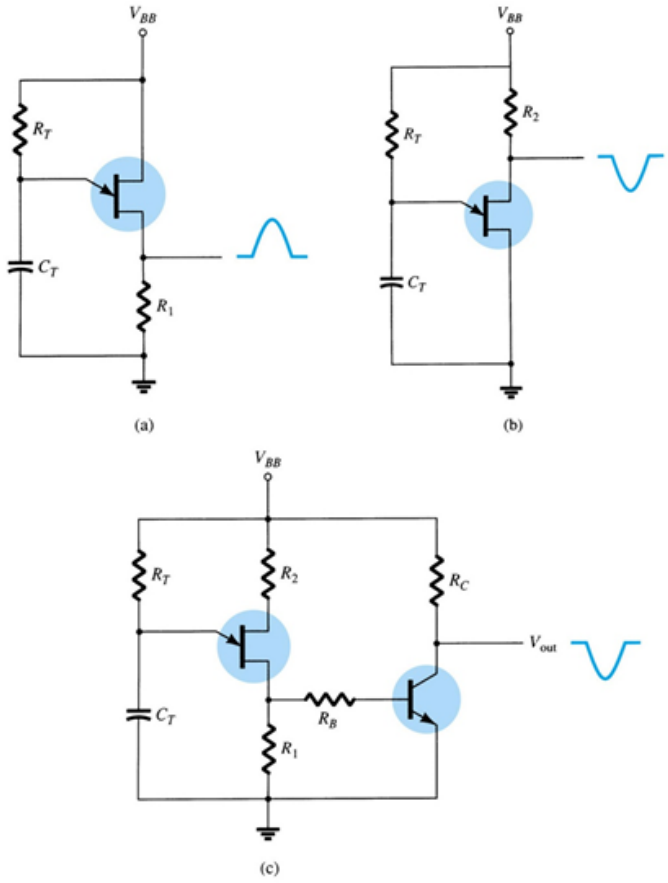


Figure 1.5.22: Some unijunction oscillator circuit configurations.

A few circuit variations of the unijunction oscillator are provided in Figure 1.5.22 above.

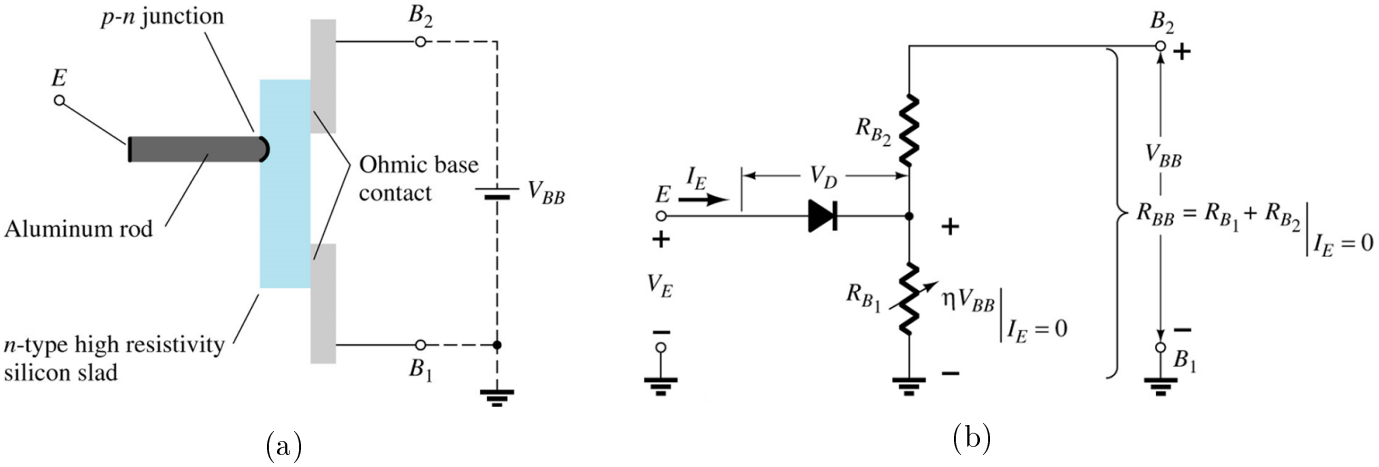


Figure 1.5.23: Unijunction transistor(UJT): (a) basic construction, (b) equivalent circuit.

Basic construction and equivalent circuit representation of the UJT is given in Figure 1.5.23 above.

Chapter 2

Digital Electronics

2.1 Properties of Digital Integrated Circuits

We are going to introduce the general properties and definitions common to all digital integrated circuit families. These properties and definitions include **voltage transfer characteristic (output voltage vs. input voltage)**, **Fan-in**, **Fan-out**, **power dissipation** and **propagation delay**.

Five basic logic operations, namely NOT, AND, OR, NAND and NOR, are used to investigate the properties of digital circuits, because any complex logical operation can be implemented by these five logic operations. The electronic circuit which performs one of these logic functions is called as a **gate**. The logic gates that perform one or more of the basic operations are called combinational gates.In this part of the course, we are mostly investigate the properties of such combinational gates.

The voltages (or currents) in digital logic circuits have two possible states corresponding to two binary variables: **0** and **1**. We usually define the **LOW** voltage to correspond to a binary **0** and the **HIGH** voltage to correspond to a binary **1**.

As we can obtain an **inverter** (or **non-inverter**) from NOR and NAND (or from OR and AND gates), we are going to analyze the properties of digital circuit families mostly by starting with the analysis of the inverter or non-inverter gate.

2.1.1 Inverter and Non-Inverter Gates

Figure 2.1.1(a) and Figure 2.1.1(b) below show the circuit symbols for the **inverter** gate. The small circle denotes logical inversion (it makes no difference whether the inverting circle is at the input or output). That is, if the input voltage is **low**, the output voltage will be **high** and vice versa. This gate is also referred to as a NOT gate, since it performs the logical NOT operation.

(a) (b)

Figure 2.1.1: Inverter symbols: (a) inverter symbol, (b) alternate inverter symbol.

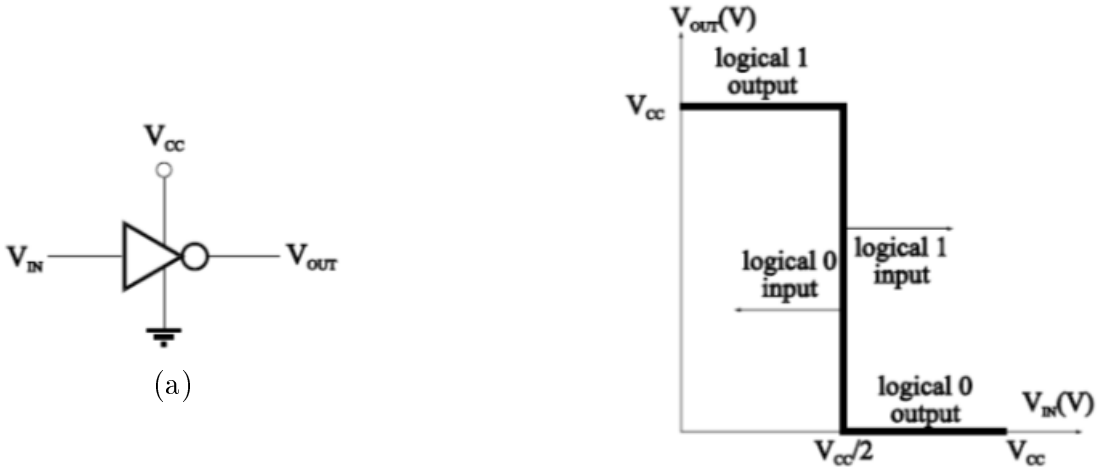
Figure 2.1.2(a) and Figure 2.1.2(b) below show the circuit symbols for the **non-inverter** gate, or sometimes referred to as a **buffer**.

(a) (b)

Figure 2.1.2: Non-inverter symbols: (a) non-inverter symbol, (b) alternate non-inverter symbol.

2.1.2 Ideal Inverter

Figure 2.1.3(a) below shows an ideal inverter gate operating with a single power supply, V_{CC}.



(a) (b)

Figure 2.1.3: Ideal inverter: (a) operates from a single power supply, (b) voltage transfer characteristic.

Figure 2.1.3(b) above shows the voltage transfer characteristic (VTC) of the ideal inverter gate, where the logical **1** is ideally at the power supply voltage V_{CC} and the logical **0** is ideally at ground (0 V). Logic gates with output voltage transitions from ground to the power supply voltage are called to operate **rail-to-rail**.

The transition between output logic states ideally occurs abruptly at an input value of $V_{CC}/2$. Thus, logical input **0** (or **input LOW**) is represented by the voltage range $0 \leq V_{IN} < V_{CC}/2$, since an input in this range generates a logical **1** output (or **output HIGH**) state.

Similarly, logical input **1** (or **input HIGH**) is represented by the voltage range $V_{CC}/2 < V_{IN} \leq V_{CC}$.

The input voltage $V_{IN} = V_{CC}/2$ has an undefined output and will cause unpredictable results, and is therefore avoided.

2.1.3 Inverter Voltage Transfer Characteristic

Figure 2.1.4 below shows the linearized form of the voltage transfer characteristic (VTC) of an inverter.

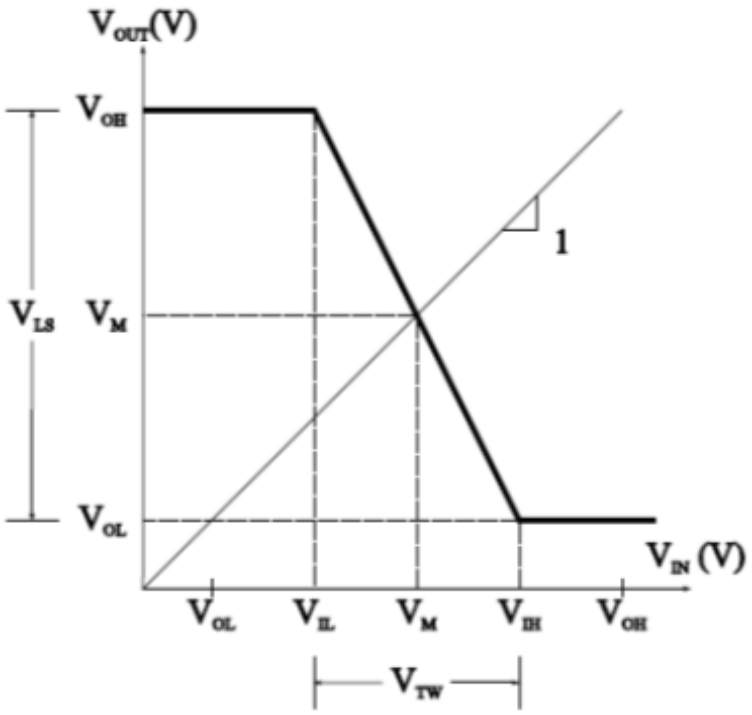


Figure 2.1.4: Linearized voltage transfer characteristic (VTC) of an inverter

Indicated on the output axis are the voltages V_{OH} and V_{OL} which correspond to the **output high** and **output low** voltage levels, respectively.

On the input axis, V_{IL} is the maximum input voltage that is considered as a LOW input (i.e., that provides a HIGH output), and V_{IH} is the minimum input voltage that is considered as a HIGH input (i.e., that provides a LOW output),i.e.,

$$V_{IN} = \begin{cases} \textbf{LOW}, & \text{if } V_{IN} \leq V_{IL} \\ \textbf{HIGH}, & \text{if } V_{IN} \geq V_{IH} \\ \text{undefined}, & \text{if } V_{IL} < V_{IN} < V_{IH} \end{cases} \tag{2.1.1}$$

It is customary to indicate output voltages V_{OL} and V_{OH} also on the input axis. Because output voltages V_{OL} and V_{OH} for the current inverter will be the **inputs** for the **next inverter**. If we want these outputs V_{OL} and V_{OH} to be considered LOW and HIGH, respectively, for the next inverter, then we must always have

$$V_{OL} < V_{IL} \tag{2.1.2}$$

$$V_{OH} > V_{IH}. \tag{2.1.3}$$

One of the critical points labelled on the VTC graph is the midpoint voltage, V_M, which is defined as the point on the transfer characteristic where $V_{OUT} = V_{IN}$ and ideally should appear at the center of the transition region. V_M can be found graphically by drawing the $V_{OUT} = V_{IN}$ line (the unity slope line) on the VTC and finding its intersection with the VTC.

Logic swing, V_{LS}, is defined as the magnitude of the voltage difference between the output high and low voltage levels, i.e.,

$$V_{LS} = V_{OH} - V_{OL} \tag{2.1.4}$$

Transition width, V_{TW}, is defined as the magnitude of the voltage difference between V_{IH} and V_{IL} voltage levels, i.e.,

$$V_{TW} = V_{IH} - V_{IL} \tag{2.1.5}$$

The low and high voltage **noise margins**, V_{NML} and V_{NMH}, represent a safety margin for low and high voltage levels, respectively.

$$V_{NML} = V_{IL} - V_{OL} \tag{2.1.6}$$
$$V_{NMH} = V_{OH} - V_{IH} \tag{2.1.7}$$

Extraneous noise voltages must have magnitudes less than the voltage noise margins.

The effects of input variations are also quantified in terms of the **noise sensitivities**. The low and high noise sensitivities are defined as the difference between the input and midpoint voltage for V_{IN} at V_{OL} and V_{OH}, respectively, i.e.,

$$V_{NSL} = V_M - V_{OL} \tag{2.1.8}$$
$$V_{NSH} = V_{OH} - V_M \tag{2.1.9}$$

The quantity **noise immunity** is the ability of a gate to reject noise, and defined as the ratio of noise sensitivities and the logical swing, i.e.,

$$V_{NIL} = \frac{V_{NSL}}{V_{LS}} \tag{2.1.10}$$
$$V_{NIH} = \frac{V_{NSH}}{V_{LS}} \tag{2.1.11}$$

Example 2.1: For the circuit in Figure 2.1.5 below, determine V_{OL}, V_{OH}, V_{IL}, V_{IH}, V_M, V_{TW}, V_{LS}, V_{NML}, V_{NMH}, V_{NSL}, V_{NSH}, V_{NIL} and V_{NIH}.

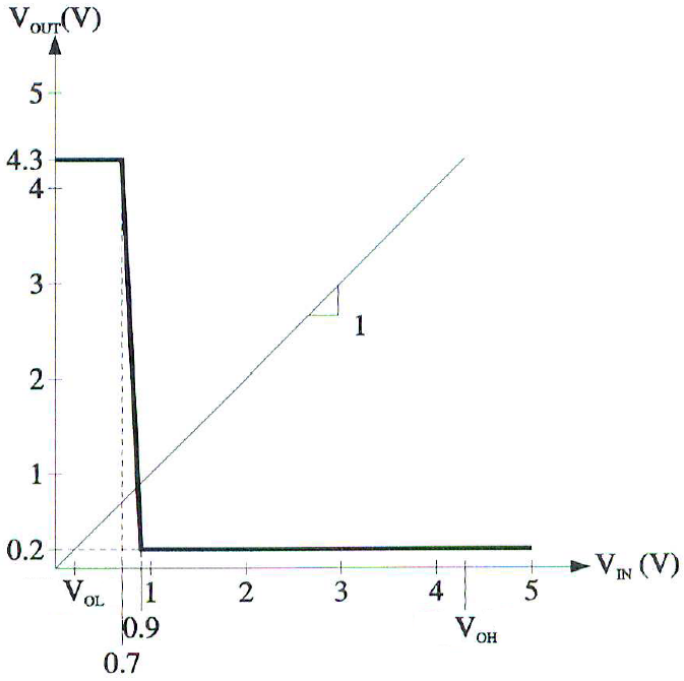


Figure 2.1.5: A VTC example

2.1.4 Fan-In and Fan-Out

A general logic gate has multiple inputs and multiple outputs. By multiple outputs, we mean the output of a given gate is connected to (i.e., driving) the inputs of several load gates.

The term **fan-in** is used to describe the number of inputs of a gate, as shown in Figure 2.1.6(b) below. Similarly, the term **fan-out** is used to describe the number of outputs of a gate, as shown in Figure 2.1.6(a) below.

(a) (b)

Figure 2.1.6: Fan-in and fan-out: (a) Fan-in (b) Fan-out

Figure 2.1.7 below shows the input and output impedance model of an inverter.

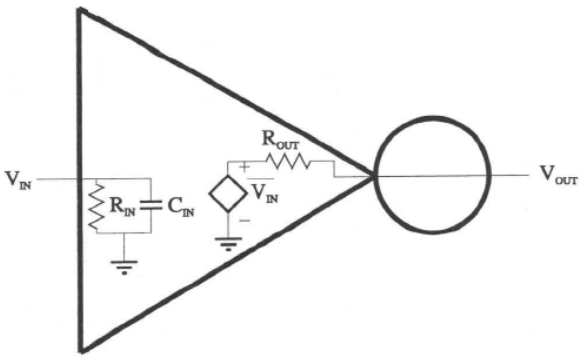


Figure 2.1.7: Input and output impedance model of an inverter.

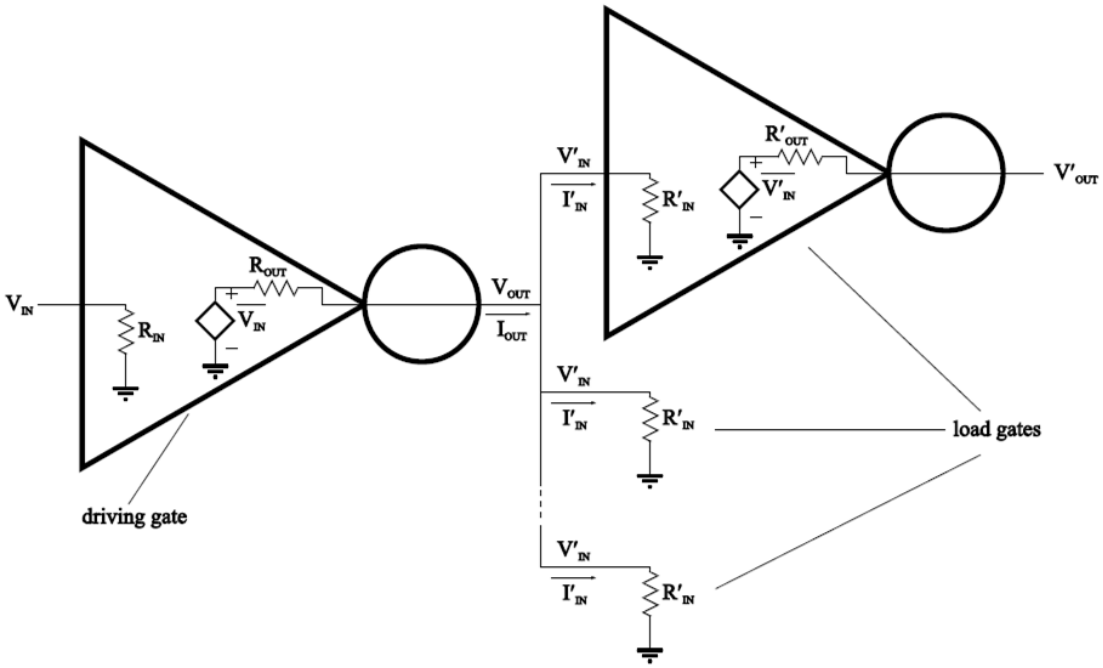


Figure 2.1.8: Static driving of multiple (identical) inverters.

Maximum fan-out of a digital logic circuit is the maximum number of load gates that can be connected to the output of a gate in parallel as shown in Figure 2.1.8 above. From the static behaviour point of view, it is restricted by its input and output currents,

$$N_{\max} = \min\left(N_{OL(\max)}, N_{OH(\max)}\right) \tag{2.1.12}$$

where

$$N_{OL(\max)} = \left\lfloor \frac{I_{OL(\max)}}{I'_{IL}} \right\rfloor \tag{2.1.13}$$

$$N_{OH(\max)} = \left\lfloor \frac{I_{OH(\max)}}{I'_{IH}} \right\rfloor \tag{2.1.14}$$

and $\lfloor \cdot \rfloor$ denotes the floor function.

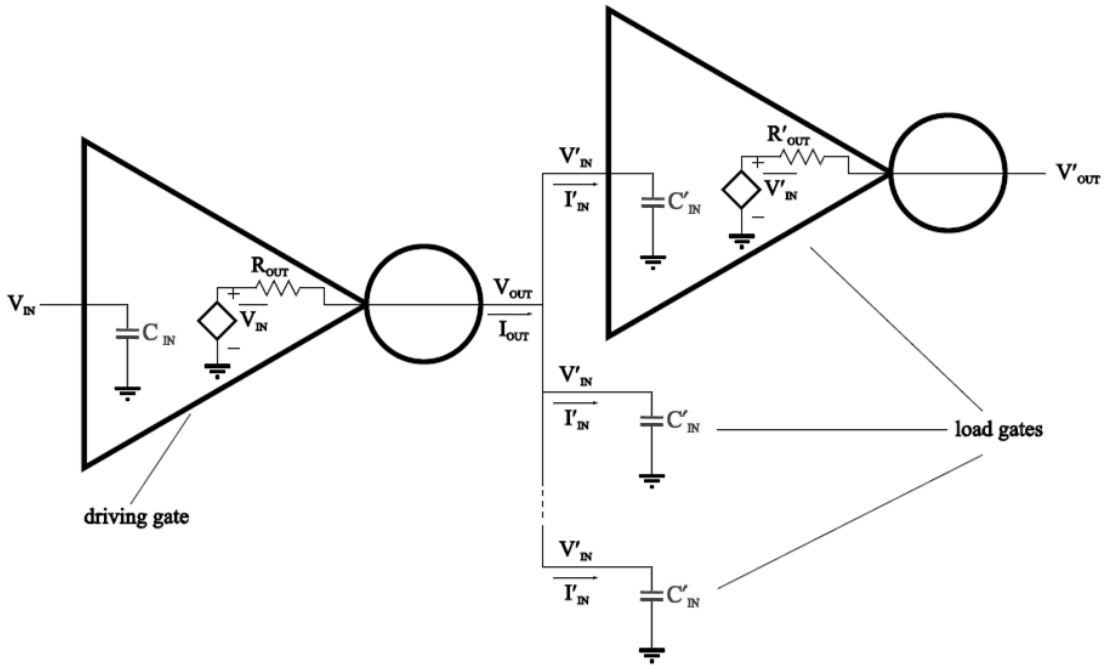


Figure 2.1.9: Dynamic driving of multiple (identical) inverters.

As input current of MOSFET's is the infinitesimal gate current, this might suggest that logic circuits with MOSFETs will have an infinite fan-out. However, this is not the case. Fan-out of MOSFET digital circuits is limited by the input capacitance of the gate which is the gate oxide capacitance due to dynamic behaviour. As you see in Figure 2.1.9 above, equivalent load capacitance will be higher (parallel capacitances are added together) limiting the maximum operating frequency. In other words, maximum required operating frequency will limit the maximum number of load gates.

Example 2.2: For the circuit in Figure 2.1.10 below, calculate the maximum fan-out.

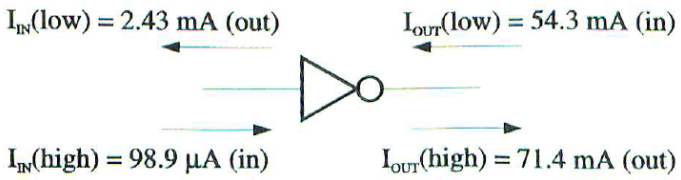


Figure 2.1.10: Inverter with input and output currents shown.

2.1.5 Transient Characteristics

Digital circuits have finite **switching speeds**, i.e., switching a voltage from high to low (or low to high) requires a finite amount of time called **turn-on** t_{ON} and **turn-off** t_{OFF} time.

Additionally, when the input voltage changes from one level to another, the output voltage is delayed in time, which is referred to as **propagation delay**.

For digital circuits employing BJTs, these time limitations are caused by the time required to store and remove charge from the base region.

Similarly, transient characteristics of digital circuits employing MOSFETs are limited by the gate oxide capacitance.

Ideally, turn-on, turn-off and propagation delay times are zero, as shown in the ideal transient response of the inverter in Figure 2.1.11 below.

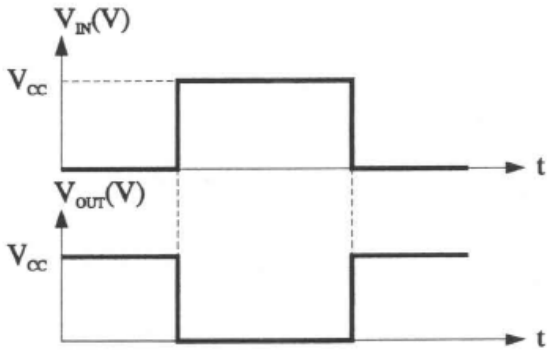


Figure 2.1.11: Ideal transient response of an inverter.

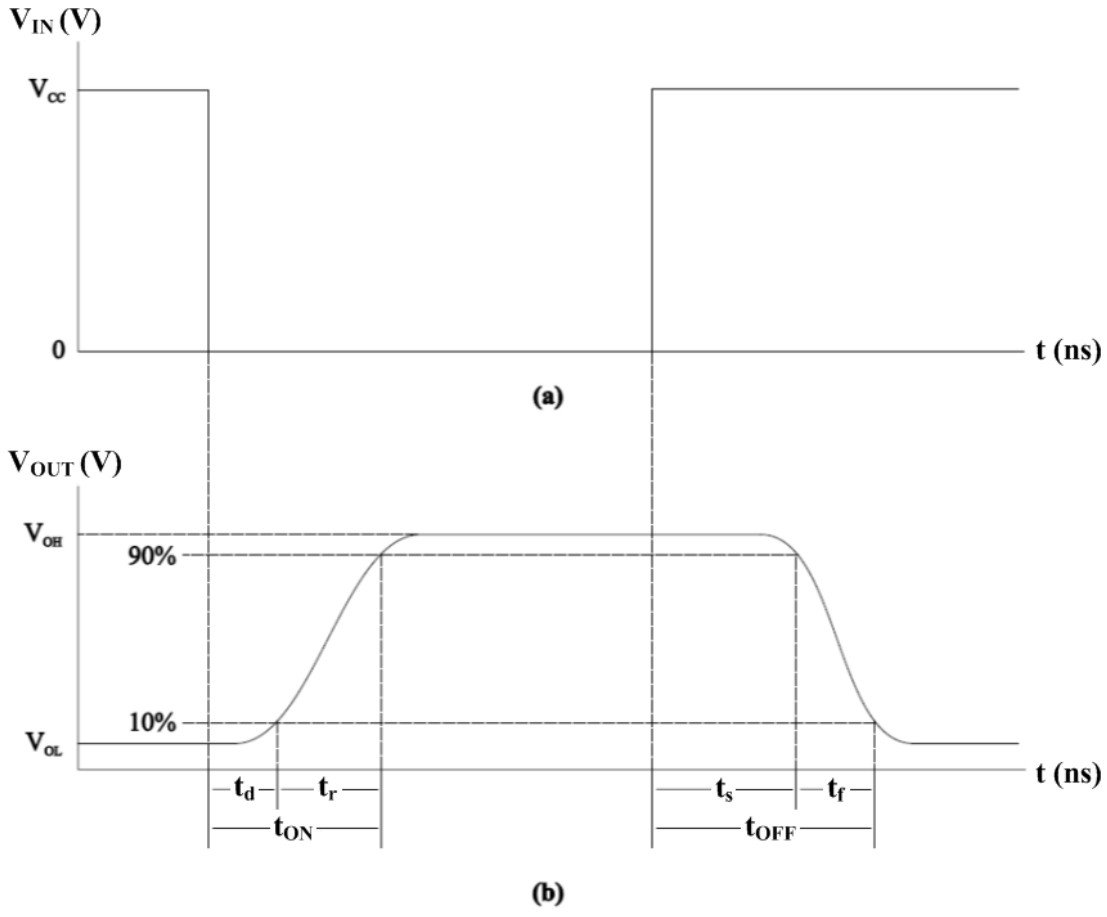


Figure 2.1.12: Switching speed definitions: (a) input pulse (b) output pulse.

Figure 2.1.12 above shows an input pulse and output response of an inverter. Here, t_d is the delay time, t_r is the rise time, t_s is the storage time, t_f is the fall time, $t_{ON} = t_d + t_r$ is the turn-on time and $t_{OFF} = t_s + t_f$ is the turn-off time.

The 10% V_{OH} and 90% V_{OH} points are marked on both the rising and falling edges of the output voltage. The rise time t_r and fall time t_f are the times associates with charging and discharging load capacitances.

The delay time t_d and storage time t_s are associated with the storage charge of PN junctions.

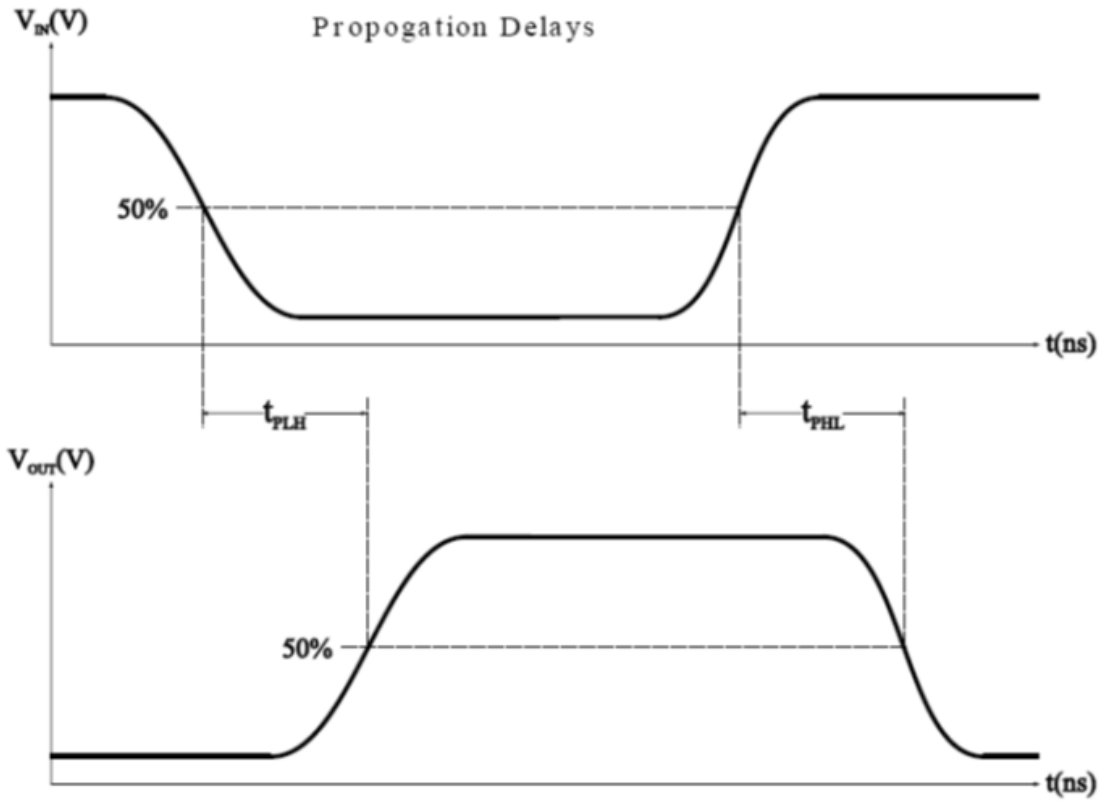


Figure 2.1.13: Propagation delay definitions: (a) input waveform (b) output response.

Figure 2.1.13 above shows an input waveform and output response of an inverter. Here, t_{PLH} is the low-to-high propagation delay timereferring to the low-to-high transition of the output and t_{PHL} is the high-to-low propagation delay timereferring to the high-to-low transition of the output.

The 50% points are labelled on the rising and falling edges of both the input and output waveforms.The 50% points are used to defined the time required for the output to respond to the input.

The overall propagation delay time $t_{p(avg)}$ is defined as the average of low-to-high and high-to-low propagation delay times, i.e.,

$$t_{p(avg)} = \frac{t_{PLH} + t_{PHL}}{2}. \tag{2.1.15}$$

2.1.6 Average Power Dissipation

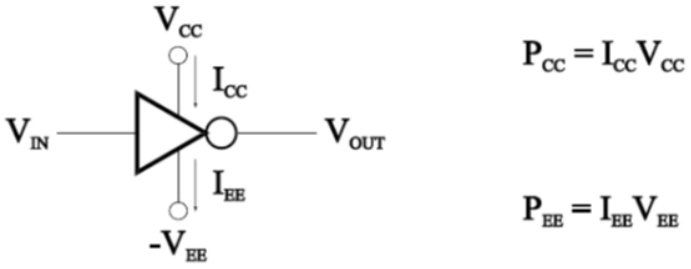


Figure 2.1.14: Power dissipation in a logic gate with two power supplies.

A logic circuit with two power supplies is shown in Figure 2.1.14 above. As the power dissipated in this gate for the output high and output low states are different, the **average power dissipation** $P_{D(avg)}$ for this gate with two possible states are given as

$$P_{D(avg)} = P_{CC(avg)} + P_{EE(avg)} \tag{2.1.16}$$

$$= \frac{P_{CC(OH)} + P_{CC(OL)}}{2} + \frac{P_{EE(OH)} + P_{EE(OL)}}{2} \tag{2.1.17}$$

$$= \frac{I_{CC(OH)} + I_{CC(OL)}}{2} V_{CC} + \frac{I_{EE(OH)} + I_{EE(OL)}}{2} V_{EE} \tag{2.1.18}$$

As we will see later, static power dissipation will be zero in CMOS circuits. Hence, we have to consider the dynamic power dissipation as given below

$$P_{D(dynamic)} = C_L f V_{LS}^2. \tag{2.1.19}$$

[]where C_L is the load capacitance, f is the frequency of switching and V_{LS} is the voltage swing over the load. In CMOS circuits operate rail-to-rail, so $V_{LS} = V_{DD}$, where V_{DD} is value of the DC power supply.

2.1.7 Power-Delay Product

Low power dissipation and short propagation delay times are both desirable for digital logic circuits. However, faster propagation times are achieved at the cost of increased power dissipation. Conversely, lower power dissipation results in longer propagation delays

A practical figure of merit used for digital logic gates is the **power-delay product** or speed-power product given by

$$PD = P_{D(avg)} \times t_{p(avg)} \tag{2.1.20}$$

The unit of power-delay product is in terms of joules and the lower the value of the power-delay product the better.

For a logic family, this power-delay product can be considered as constant. In other words, if you want to decrease power dissipation by increasing resistor values, the propagation delay will increase accordingly. You can change the power-delay product by redesigning the whole digital circuit (using different design and/or different components).

2.1.8 Logic Families

A summary of logic families are shown as a diagram in Figure 2.1.15 below.

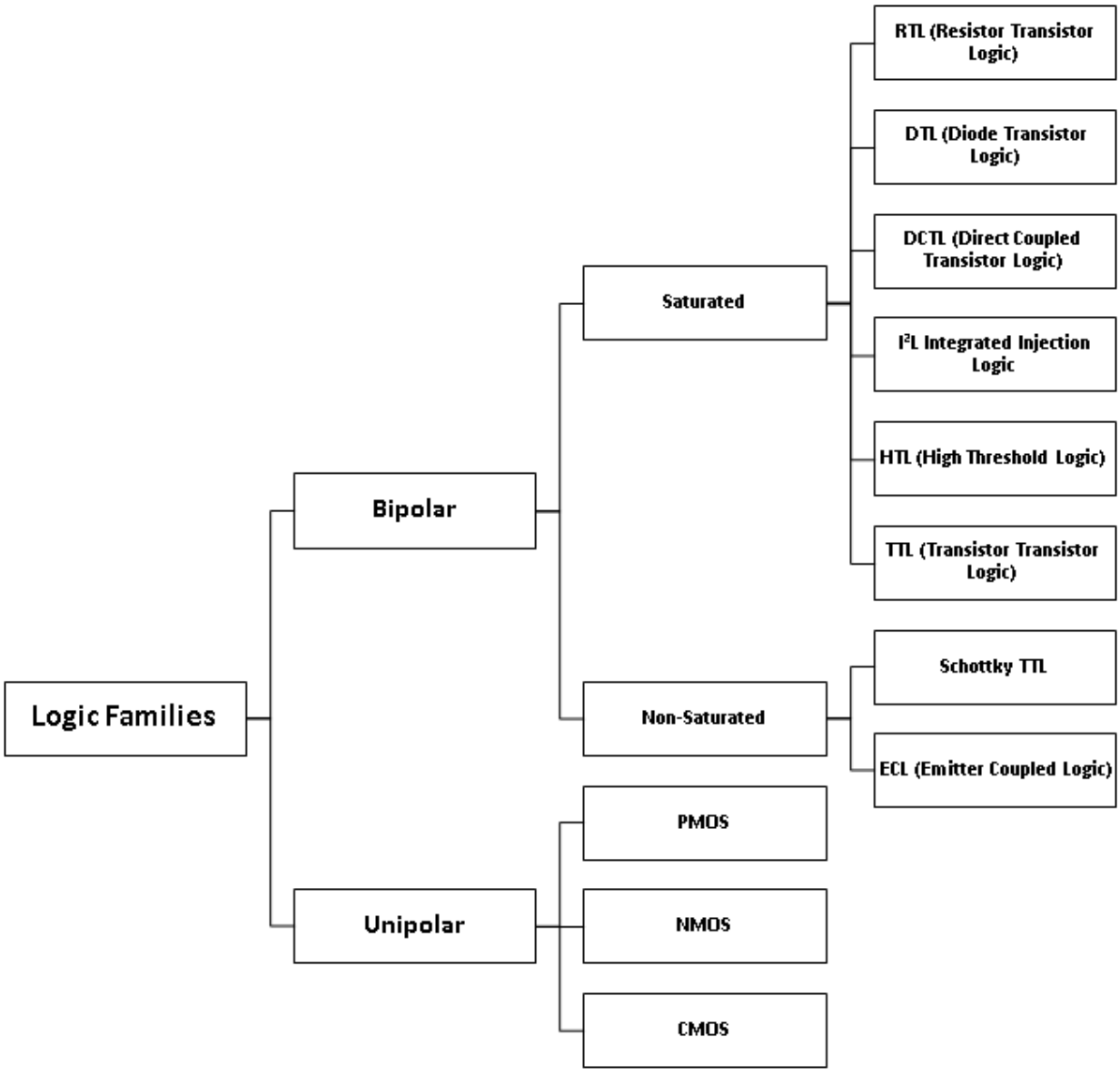


Figure 2.1.15: A diagram of logic families.

All logic families have different properties. For example, CMOS logic circuits have very low power dissipations.

For another example, propagation delay and power dissipation characteristics for TTL and STTL families are given in Table 2.1 below.

Table 2.1: Power dissipation and propagation delay characteristics of TTL and STTL families

Family	**Power**	**Prop. Delay**
TTL	10 mW	9 ns
STTL	20 mW	3 ns
LSTTL	2 mW	9 ns
ASTTL	10 mW	2 ns
ALSTTL	1 mW	4 ns
FAST	4 mW	2 ns

2.2 Diodes

2.2.1 Diode Model

Diodes are important elements in digital electronic circuits, as well as they are used to perform various logic operations, they are also used as variable capacitors, DC voltage level shifters and clamping diodes at logic circuit inputs.

Symbols for PN junction diodes and MN junction diodes are shown in Figure 2.2.1(a) and Figure 2.2.1(b) below, respectively.

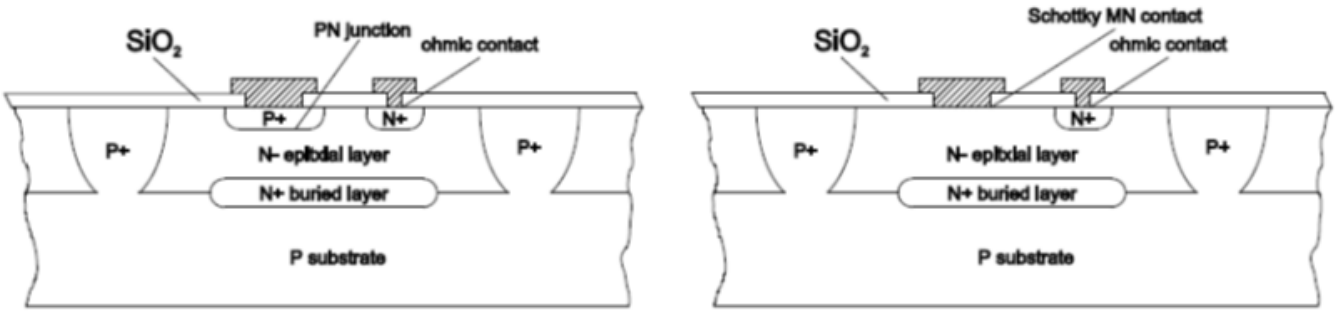
(a) (b)

Figure 2.2.1: Diode symbols: (a) PN junction diode, (b) MN Schottky barrier diode.

PN junction diodes are formed from the combination of P-type and N-type regions. Usually, PN junctions in integrated circuits (ICs) are usually formed by utilizing the two out of the three regions of a bipolar junction transistor, instead of a separate device structure. Turn-on voltage for a PN junction diode is $V_{D(ON)} = 0.7\,\mathrm{V}$.

MN junction (Schottky Barrier) diodes are formed from the combination of a metal and an N^--type semiconductor. Metal used in MN junction diodes is mostly platinum silicide (Pt_5Si_2). As there are no holes present, MN junction diodes are much faster than PN junction diodes. Turn-on voltage for a Schottky Barrier (MN junction) diode is $V_{SBD(ON)} = 0.3\,\mathrm{V}$.

Cross sections of some example PN and MN junction diodes as shown in Figure 2.2.2(a) and Figure 2.2.2(b) below, respectively, in order to highlight some of the fabrication properties.



(a) (b)

Figure 2.2.2: Diode cross sections: (a) PN junction diode, (b) MN Schottky barrier diode.

Diode current-voltage (IV) characteristics are normally governed by the well-known Shockley's diode equation,

$$I_D = I_S \left(e^{V_D/\gamma} - 1\right) \tag{2.2.1}$$

where I_S is the reverse saturation current (typically pA for PN junction diodes and μA for MN junction diodes) and $\gamma = \phi_T = kT/q$ is the thermal voltage (typically $\gamma = 26\,\text{mV}$ at $300\,\text{K}$) with k representing the Boltzman constant, T representing the temperature in kelvins and q representing the elementary charge.

In the analysis of digital circuits, we are going to use the **simplified diode model** as shown in Figure 2.2.3 and summarized in Table 2.2 below

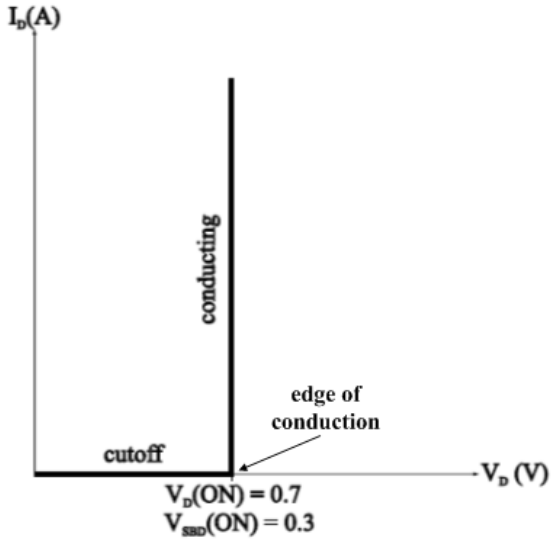


Figure 2.2.3: IV characteristics of the simplified diode model.

The transition point from cutoff mode to conduction mode (i.e., when the current is not yet flowing) is called as **edge of conduction** (EOC).

Table 2.2: Diode modes of operation

Junction Bias	**Mode of Operation**
Reverse	Cutoff (OFF)
Forward	Conducting (ON)

The large signal diode model used in SPICE in shown in Figure 2.2.4 below.

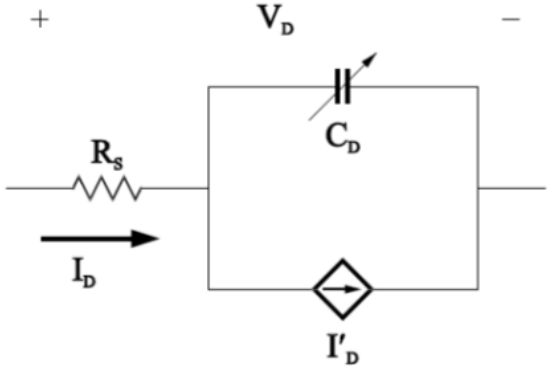


Figure 2.2.4: SPICE diode model.

PN Junction capacitance can be utilized in ICs by applying a negative bias to a diode. Diodes used for this purpose are referred to as **varactor** diodes and have the modified circuit symbol presented in Figure 2.2.5 below.

Figure 2.2.5: Varactor diode (voltage dependent capacitor for $V_D < 0$).

2.2.2 Clamping Diodes

When the input to a gate is switched from high-to-low, the input voltage sometimes swings well beyond 0 V. This is called as ringing and may cause physical damage to the gate.

Connecting **clamping** diodes to each input of a gate, as shown in Figure 2.2.6 below, eliminates this problem by preventing inputs from falling below -0.7 V. The diodes will not affect the operation of the gate, as the diodes are open circuit for positive inputs.

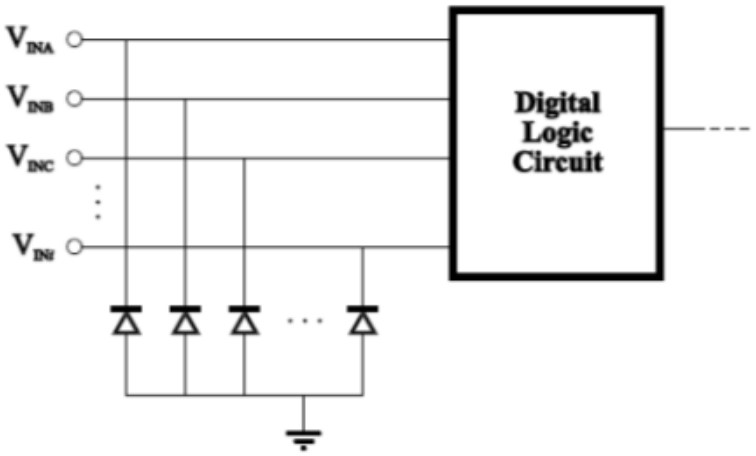


Figure 2.2.6: Input clamping diodes.

Clamping diodes can be also connected to the output(s) of a gate.

Most TTL/STTL families employ clamping diodes at their inputs and sometimes also at their outputs.

2.2.3 Level-Shifting Diodes

It is often required to change the voltage level across particular portions of digital circuits, e.g., to level shift the output voltage.

Another use of the diode forward voltage is to ensure that sub-circuits with complementary objectives are not conducting simultaneously. For example, TTL circuits employ two output drivers. Only one driver should be working for the output-low state, while only the other driver should be working for the output-high state. Placement of a voltage level-shifting device between the two drivers ensures the desired operation by allowing only one driver to be on at a time.

Example 2.3: For the circuit in Figure 2.2.7 below, determine the level-shifting voltage V_{shift}.

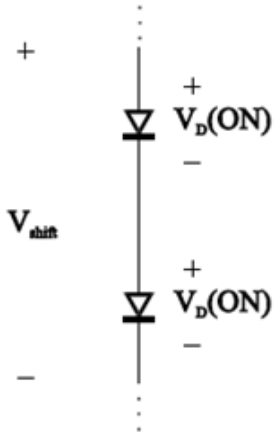


Figure 2.2.7: A level-shifting diodes example.

2.3 BJT Transistors

Bipolar junction transistors (BJTs) are very important in digital circuits, e.g., TTL circuits are based on BJTs. Figure 2.3.1 below shows a 3D cross-section (without metallization) of an NPN BJT fabricated with the junction isolated technology.

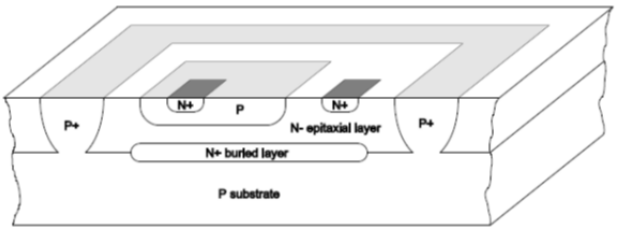
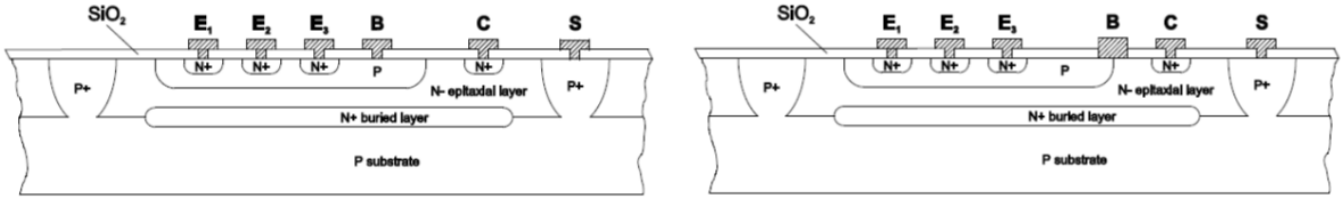


Figure 2.3.1: Three-dimensional cross-section (without metallization).

In some BJT logic families (e.g., TTL), multiple inputs are achieved by using multi-emitter BJTs as shown in Figure 2.3.2(a) below.



(a) (b)

Figure 2.3.2: Multi-emitter NPN transistor cross-sections with junction isolation technology: (a) BJT, (b) Schottky-clamped BJT.

A multi-emitter **Schottky-clamped BJT** (SBJT) is shown in Figure 2.3.2(b) above. The base contact is extended over the N collector region, thus placing a Schottky Barrier (MN) diode in parallel with the base-collector PN junction. This device operates much faster than a normal BJT, and an SBJT does not go into saturation mode.

The most frequently used notation and symbols for BJT transistors are shown in Figure 2.3.3 below for the NPN and PNP transistors.

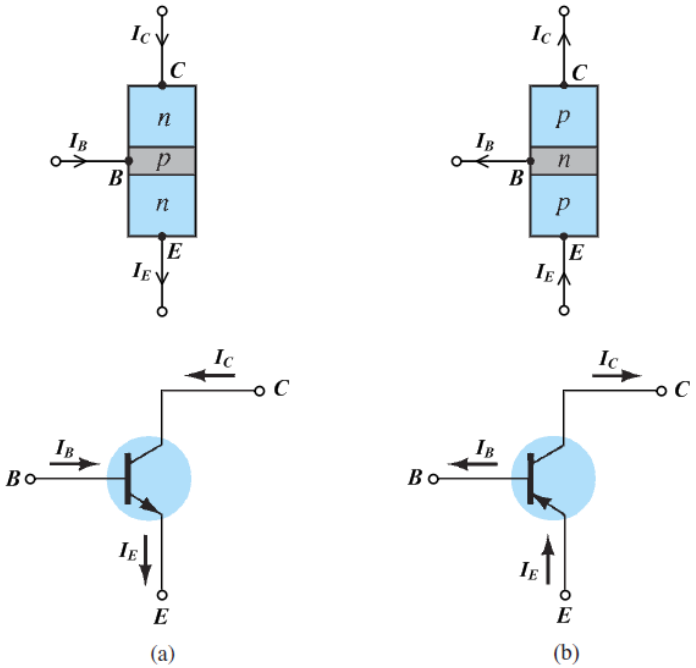
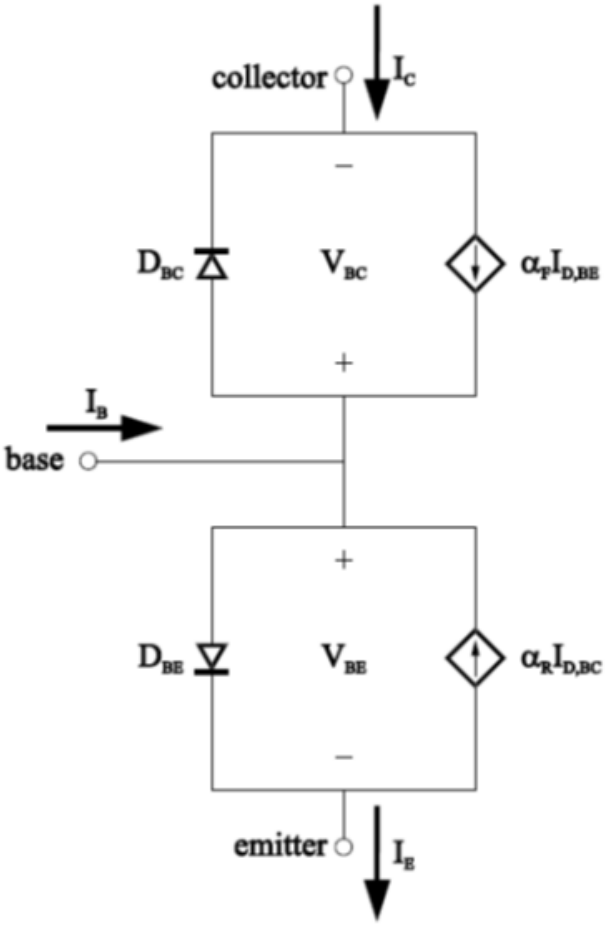


Figure 2.3.3: Notation and symbols used for BJT transistors: (a) NPN transistor, (b) PNP transistor.

2.3.1 Ebers-Moll BJT Model

Ebers-Moll model is a well-known BJT model, shown for an NPN BJT in Figure 2.3.4, can be used to calculate the terminal currents for all modes of operation.



$$I_{D,BE} = I_{ES}\left(e^{V_{BE}/\gamma} - 1\right) \tag{2.3.1}$$

$$I_{D,BC} = I_{CS}\left(e^{V_{BC}/\gamma} - 1\right) \tag{2.3.2}$$

I_{ES} is the base-emitter reverse saturation current,

I_{CS} is the base-collector reverse saturation current,

γ is the thermal voltage ($kT/q = 26\,\text{mV}$ at $300\,\text{K}$).

$$\boxed{I_E = I_{D,BE} - \alpha_R I_{D,BC}} \tag{2.3.3}$$

$$\boxed{I_C = \alpha_F I_{D,BE} - I_{D,BC}} \tag{2.3.4}$$

$$\boxed{I_B = I_E - I_C} \tag{2.3.5}$$

α_F and α_R are the common base **forward** and **reverse** amplification factors. (typically $\alpha_F \approx 1$ and $0.2 \leq \alpha_R \leq 0.6$)

Reciprocity theorem:

$$I_S = \boxed{\alpha_F I_{ES} = \alpha_R I_{CS}} \tag{2.3.6}$$

I_S is known as the transport saturation current.

Figure 2.3.4: Ebers-Moll NPN BJT model.

2.3.2 BJT Modes of Operation

A BJT transistor has two PN junctions: the base-emitter PN junction (BE junction) and the base-collector PN junction (BC junction), as depicted in Figure 2.3.3 and Figure 2.3.4 above. As either junction can be forward or reverse biased, there are four modes of operation (or four transistor states) as shown in Table 2.3 below.

Table 2.3: BJT modes of operation

BE Junction Bias	**BC Junction Bias**	**Mode of Operation**
Reverse	Reverse	Cutoff (OFF)
Forward	Reverse	Forward Active (FA)
Reverse	Forward	Reverse Active (RA)
Forward	Forward	Saturation (SAT)
		(Forward Saturation (FSAT) or Reverse Saturation (RSAT) in reality)

In all modes of operation, Kirchoff's Current Law (KCL) must be satisfied, i.e.,

$$\boxed{I_E = I_C + I_B} \tag{2.3.7}$$

2.3.2.1 Cutoff (OFF)

In the **cutoff** (OFF) mode, both PN junctions (BE and BC) of the BJT are reverse-biased. If we assume simplified diode model for the PN junctions in the Ebers-Moll model, both $I_{D,BE}$ and $I_{D,BC}$ are zero. Consequently,

$$I_{E(OFF)} = 0 \tag{2.3.8}$$

$$I_{C(OFF)} = 0 \qquad \text{and} \qquad I_{B(OFF)} = 0 \tag{2.3.9}$$

2.3.2.2 Forward Active (FA)

In the **forward active** (FA) mode, the base-emitter PN junction (BE) is forward biased and the base-collector PN junction is reverse biased. In the Ebers-Moll model, $I_{D,BC}$ becomes zero. Consequently,

$$V_{BE(FA)} = 0.7\,\text{V} \tag{2.3.10}$$

$$I_{C(FA)} = \beta_F I_{B(FA)} \qquad \text{or} \qquad I_{C(FA)} = \alpha_F I_{E(FA)} \tag{2.3.11}$$

where β_F is the common-emitter current amplification factor given by

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \tag{2.3.12}$$

Similarly, α_F can also be expressed in terms of β_F as

$$\alpha_F = \frac{\beta_F}{\beta_F + 1} \tag{2.3.13}$$

2.3.2.3 Reverse Active (RA)

In the **reverse active** (RA) mode, the base-emitter PN junction (BE) is reverse biased and the base-collector PN junction is forward biased. In the Ebers-Moll model, $I_{D,BE}$ becomes zero. Consequently,

$$V_{BC(RA)} = 0.7\,\mathrm{V} \tag{2.3.14}$$

$$-I_{C(RA)} = (\beta_R + 1)\, I_{B(RA)} \qquad (I_{C(RA)} < 0) \tag{2.3.15}$$

or

$$I_{E(RA)} = \alpha_R I_{C(RA)} = -\beta_R I_{B(RA)} \qquad (I_{E(RA)} < 0) \tag{2.3.16}$$

where β_R is the reverse active current amplification factor (typically $0.1 \leq \beta_R \leq 2.0$) given by

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R} \tag{2.3.17}$$

Similarly, α_R can also be expressed in terms of β_R as

$$\alpha_R = \frac{\beta_R}{\beta_R + 1} \tag{2.3.18}$$

Note that, negative values for currents mean that currents flow in the reverse directions than the directions shown in Figure 2.3.3. In other words, negative I_E and I_C mean that the current is flowing into the emitter and out of the collector for an NPN transistor, and into the collector and out of the emitter for a PNP transistor.

2.3.2.4 Saturation (SAT)

In the **saturation** (SAT) mode, both PN junctions (BE and BC) are forward biased. Normally, we only consider the case called **forward saturation** where base-emitter junction has a stronger bias (i.e., $V_{BE} \geq V_{BC}$ for NPN transistors). The opposite case ($V_{BC} > V_{BE}$ for NPN transistors) is called **reverse saturation** and rarely occurs in digital circuits.

Forward Saturation (FSAT): In this mode, base current is large and collector and emitter currents are saturated such that $I_C < \beta_F I_B$. Note that, in this mode I_C and I_E are **positive**.

$$I_{C(FSAT)} < \beta_F I_{B(FSAT)} \tag{2.3.19}$$

$$V_{BE(FSAT)} = 0.8\,\mathrm{V} \tag{2.3.20}$$

$$V_{BC(FSAT)} = 0.6\,\mathrm{V} \tag{2.3.21}$$

$$V_{CE(FSAT)} = 0.2\,\mathrm{V} \tag{2.3.22}$$

A saturation parameter σ is defined to indicate the relationship between I_C and I_B as

$$\sigma = \frac{I_C}{\beta_F I_B} \tag{2.3.23}$$

where $\sigma \leq 1$. Note that σ is not constant, it changes according to the operating point, and $\sigma = 1$ denotes forward active operation and/or edge of saturation operation. If it is not given, you may assume $\sigma_{\max} = 1$.

Reverse Saturation (RSAT): In this mode, base-collector junction has a stronger bias, i.e., $V_{BC} > V_{BE}$ for NPN transistors, and collector and emitter currents are saturated such that $-I_E < \beta_R I_B$. Note that, in this mode I_C and I_E are **negative**.

$$-I_{E(RSAT)} < \beta_R I_{B(RSAT)} \tag{2.3.24}$$

$$-I_{C(RSAT)} < (\beta_R + 1)\, I_{B(RSAT)} \tag{2.3.25}$$

$$V_{CE(RSAT)} < 0 \qquad \text{(for NPN transistors)} \tag{2.3.26}$$

In this course, we are going to refer forward saturation (FSAT) mode as the only **saturation** (SAT) mode, i.e.,

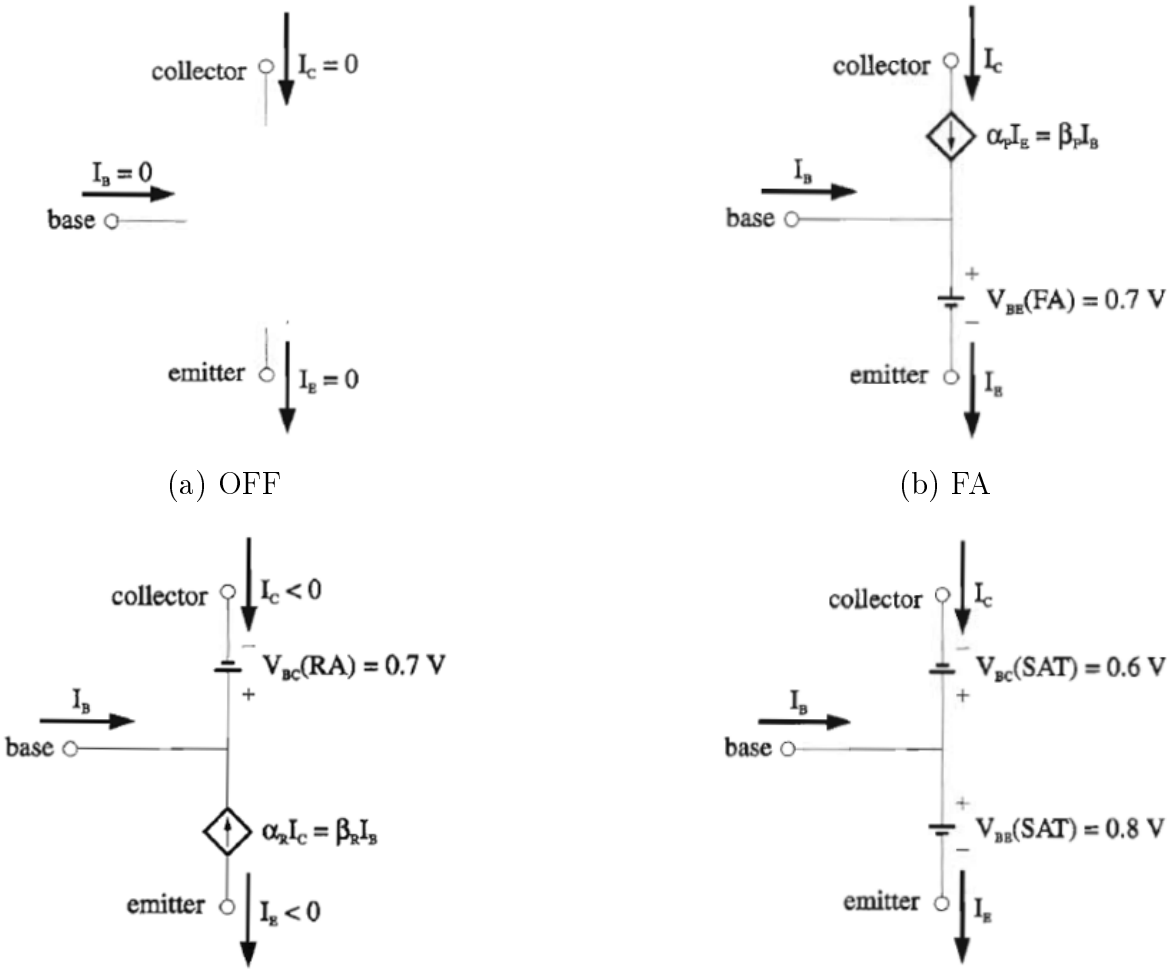
$$SAT = FSAT. \tag{2.3.27}$$

In **all** operation modes (FSAT, RSAT etc.) the following must hold:

1. I_C and I_E always have the same sign, i.e., always in the same direction,
2. Base current is always nonnegative, i.e., $I_B \geq 0$,
3. KCL is satisfied, i.e., $I_E = I_C + I_B$,
4. KVL is satisfied, i.e., $V_{CE} = V_{BE} - V_{BC}$.

2.3.2.5 Simplified NPN BJT Model

We can show the simplified models for the four modes—namely cutoff (OFF), forward active (FA), reverse active (RA) and saturation (SAT)—of operation of NPN transistors in Figure 2.3.5 below.



(a) OFF (b) FA

(c) RA (d) SAT

Figure 2.3.5: Reduced NPN BJT models for the four modes of operation: (a) Cutoff (OFF), (b) Forward Active (FA), (b) Reverse Active (RA), (d) Saturation (SAT).

We can summarize the simplified NPN BJT model with its state and circuit behaviour with Table 2.4 below.

Table 2.4: Simplified NPN BJT models for the all modes of operation

Simplified NPN BJT Model		
State	**Circuit Behaviour**	**Test Condition**
Cutoff (OFF)	$I_C = 0$, $I_E = 0$, $I_B = 0$	$V_{BE} < V_{BE(FA)}$, $V_{BC} < V_{BC(RA)}$
Forward Active (FA)	$V_{BE} = V_{BE(FA)}$, $I_C = \beta_F I_B$	$V_{BC} < V_{BC(RA)}$, $V_{CE} > V_{CE(FSAT)} > 0$
Reverse Active (RA)	$V_{BC} = V_{BC(RA)}$, $I_C = -(\beta_R + 1) I_B$	$V_{BE} < V_{BE(FA)}$, $V_{CE} < V_{CE(RSAT)} < 0$
Forward Saturation (FSAT) [Saturation (SAT)]	$V_{CE} = V_{CE(FSAT)}$, $V_{BE} = V_{BE(FSAT)}$ $V_{BC} = V_{BC(FSAT)}$	$I_C < \beta_F I_B$, $I_C > 0$, $I_E > 0$, $V_{CE} > 0$, $I_B > 0$.
Reverse Saturation (RSAT)	$V_{CE} = V_{CE(RSAT)}$, $V_{BE} = V_{BE(RSAT)}$ $V_{BC} = V_{BC(RSAT)}$	$-I_C < (\beta_R + 1) I_B$, $I_C < 0$, $I_E < 0$, $V_{CE} < 0$, $I_B > 0$.

2.3.2.6 IV Characteristics

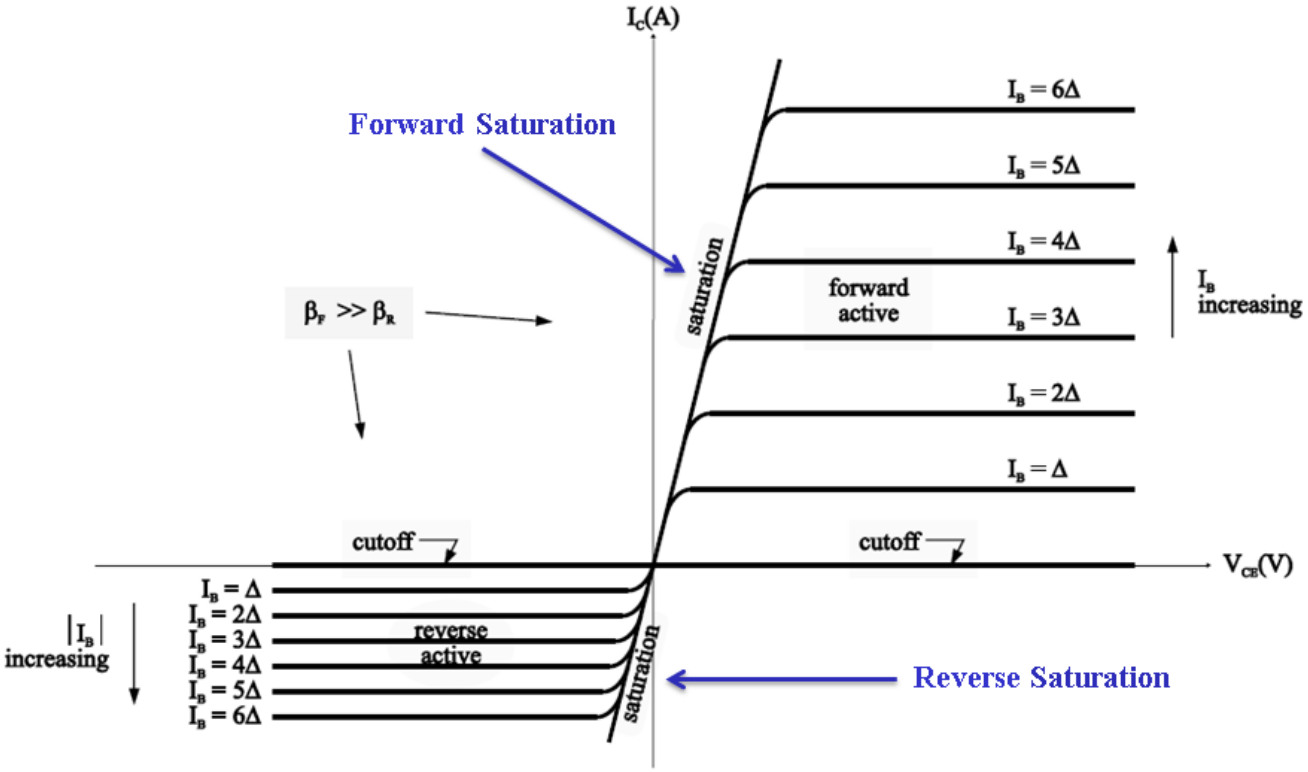


Figure 2.3.6: Output IV characteristics (I_C vs. V_{CE}) of a common-emitter NPN BJT transistor with I_B as a parameter.

Figure 2.3.6 above shows a set of I_C versus V_{CE} characteristics for changes in I_B (of amount Δ) as predicted by the Ebers-Moll model. For equal increments in I_B, the curves in the active regions are approximately evenly spaced, although the curves in the reverse active region are much closer than those in the forward active region.

Example 2.4: For the circuit in Figure 2.3.7 below, determine the state of the transistor and find currents I_B, I_C and I_E, given $\beta_F = 65$.

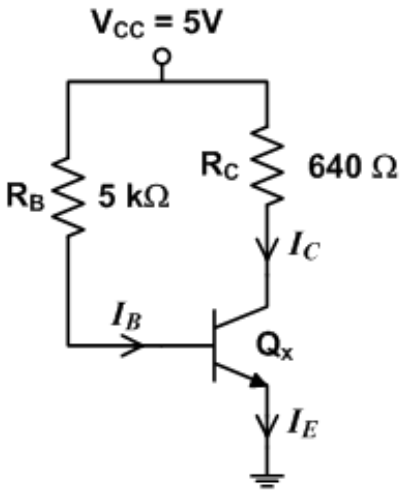


Figure 2.3.7: A simple circuit for unknown BJT state example.

Example 2.5: For the circuit in Figure 2.3.8 below, determine the voltages at the base and emitter of each BJT.

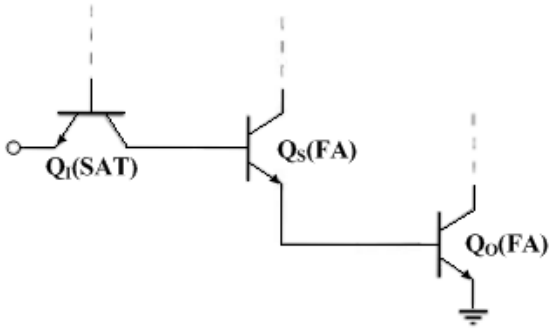


Figure 2.3.8: A digital sub-circuit for known BJT states example.

Example 2.6: For the circuit in Figure 2.3.9 below, determine I and V_B. Assume the BJT base current is negligible.

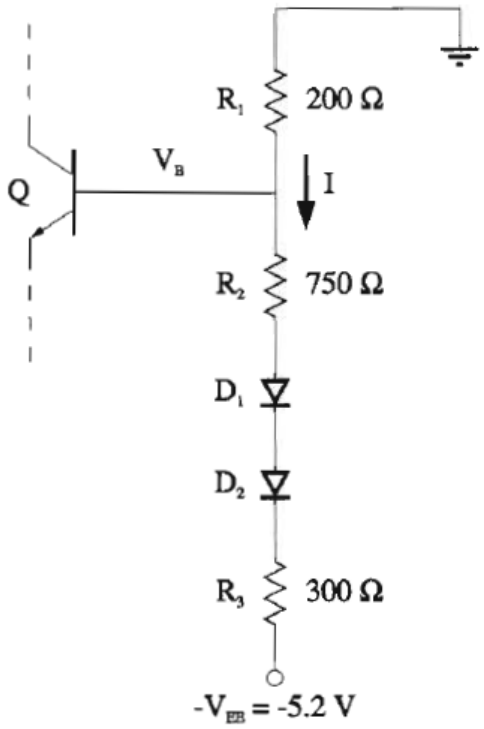


Figure 2.3.9: A saturated BJT example.

2.3.3 BJT Sub-Circuits

In order to provide a preview to succeeding chapters, this subsection introduces sub-circuits common to all TTL families summarized by the NAND block diagram in Figure 2.3.10 below.

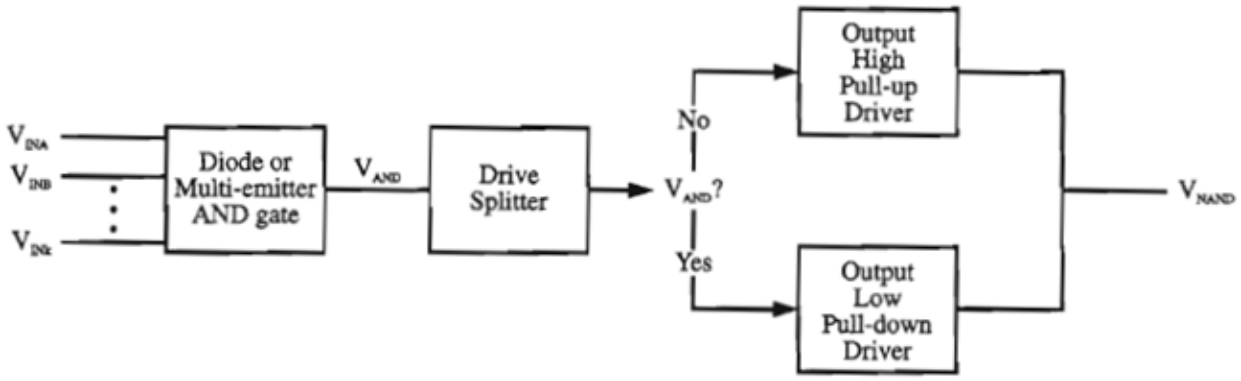


Figure 2.3.10: TTL family NAND super-circuitry block diagram.

2.3.3.1 Input Section

For this NAND diagram, input section consists of ANDing of all inputs either with a parallel diode configuration or with a multi-emitter BJT.

2.3.3.2 Drive Splitter

Depending on the result of ANDing, the **drive splitter** turns on one of the two output sections, namely output low and output high driver sections. A typical drive splitter is a BJT acting as a switch, when it is cutoff mode it activate the output-high driver and when it is in saturation mode it activates the output-low driver. Driver splitter section also provides an inversion operation.

2.3.3.3 Output-High Pull-Up Driver

As the output goes low-to-high, current is required to charge the equivalent input-capacitance of the load gates. Output-high pull-up driver provides the current for this charging. Some example pull-up driver sub-circuits are shown in Figure 2.3.11 below.

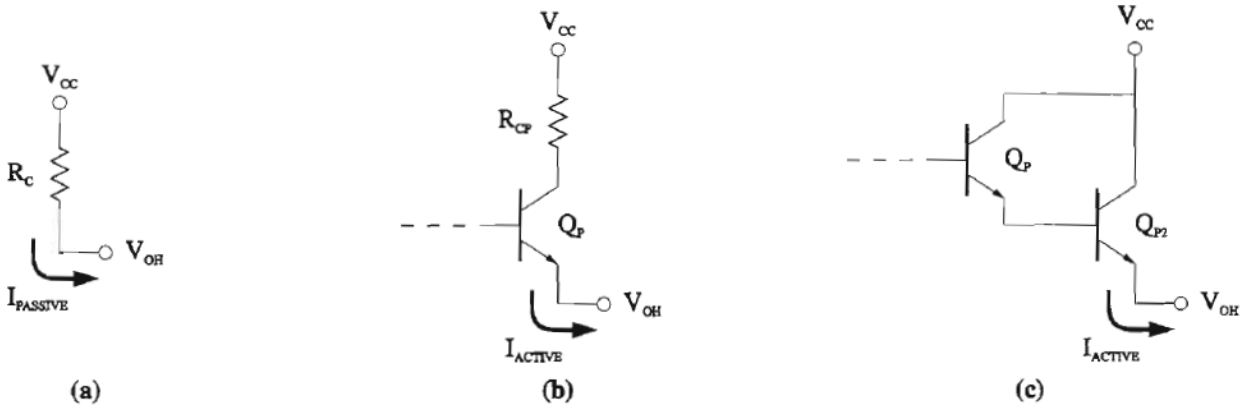


Figure 2.3.11: Pull-up driver sub-circuits: (a) Passive pull-up, (b) Active pull-up, (c) Darlington pair active pull-up.

A simple voltage driven resistor, also known as **passive pull-up**, would serve the purpose as shown in Figure 2.3.11(a) above.

An emitter-follower shown in Figure 2.3.11(b) above is an **active** solution which provides a higher output current and hence provides faster switching time for the load gates. For even more sourcing current, a Darlington pair can be used as shown in Figure 2.3.11(c) above.

Active pull-up circuitry also provides greater fan-out.

2.3.3.4 Output-Low Pull-Down Driver

There are two purposes of output-low pull-down circuits: one is to discharge the capacitive load by providing a large sinking current, and another is to provide larger fan-out by sinking currents I_{IL} from all the load gates as shown in Figure 2.3.12 below.

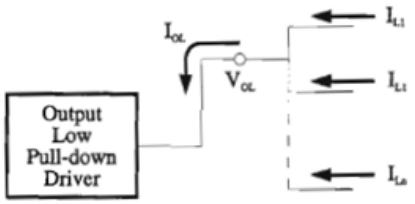


Figure 2.3.12: Fan-out current sinking for output-low pull-down driver.

Some example pull-down driver sub-circuits are shown in Figure 2.3.13 below.

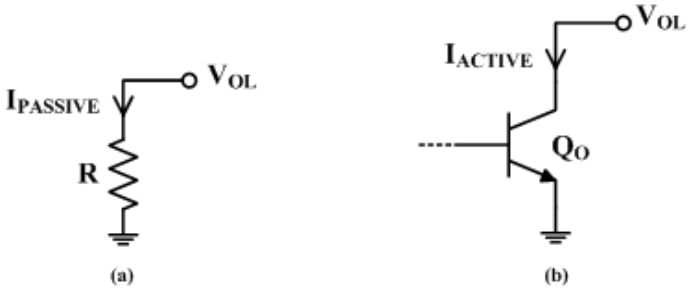


Figure 2.3.13: Pull-down driver sub-circuits: (a) Passive pull-down, (b) Active pull-down.

A simple resistor connected to a negative power supply (or ground), also known as **passive pull-down**, would serve the purpose as shown in Figure 2.3.13(a) above.

A BJT, as shown in Figure 2.3.13(b) above, will server as an **active pull-down** in **saturation** mode.

Another advantage of active pull-down or pull-up circuits is that they can be activated and/or deactivated, apart from increasing fan-out.

2.3.3.5 Discharge Paths

In order to turn off a saturated BJT, all of the stored charges in the base region must be removed. A path must therefore be available for base discharge. Some example discharge sub-circuits are shown in Figure 2.3.14 below.

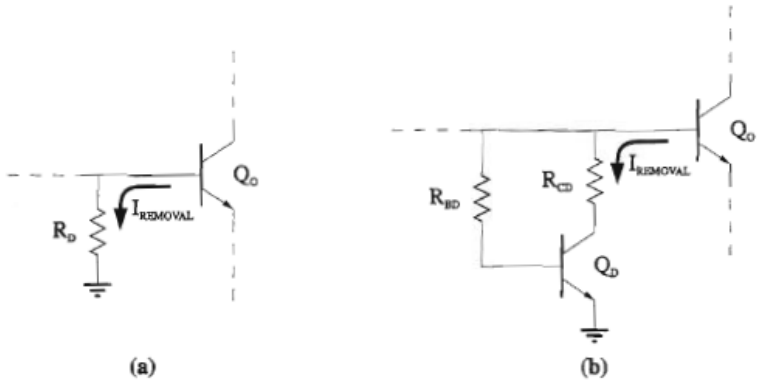


Figure 2.3.14: Discharge (or stored charge removal) sub-circuits: (a) Passive, (b) Active.

Figure 2.3.14(a) above displays a circuit with an additional resistor R_D that provides passive charge removal.

Figure 2.3.14(b) above shows an active configuration for stored charge removal, which provides a much faster discharge (i.e., higher discharge current) than R_D itself.

2.3.3.6 Base Driving Circuitry

On the other hand, the turn-on time of a BJT is dependent on the time required to charge the base of the BJT. Active base driving current is often supplied to BJTs to ensure a shorter turn-on time.

An emitter-follower BJT configuration, as shown in Figure 2.3.15 below where Q_S drives base driving current to Q_O, usually supplies this driving current.

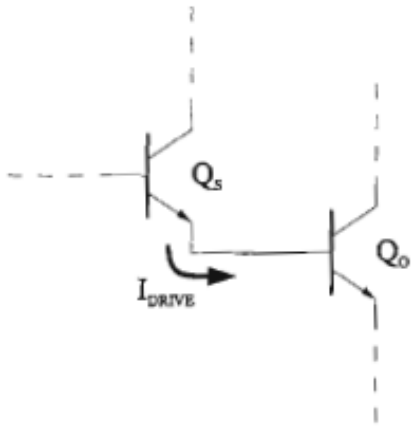


Figure 2.3.15: Active base driving circuitry.

2.3.3.7 Power Dissipation of BJT Logic Circuits

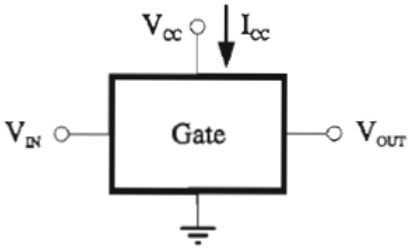


Figure 2.3.16: .

When BJT logic circuits have a single power supply, as shown in Figure 2.3.16 above, the power dissipation for a particular gate in a particular state is taken as the power supplied given by

$$P_{CC} = I_{CC} V_{CC} \tag{2.3.28}$$

where I_{CC} is the current drawn from V_{CC} and is obtained by **summing all** the currents leaving the supply voltage source.

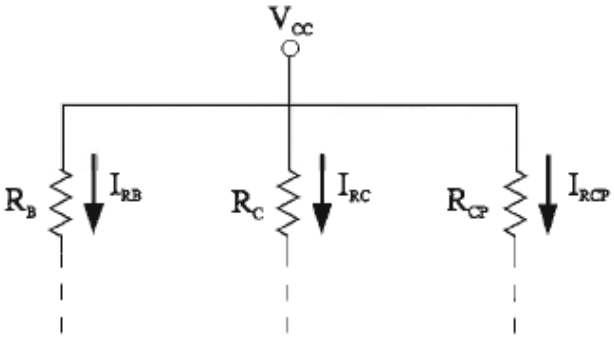


Figure 2.3.17: Currents leaving the power supply.

For example, for Figure 2.3.17 above, the current supplied by V_{CC} is

$$I_{CC} = I_{RB} + I_{RC} + I_{RCP}. \tag{2.3.29}$$

Consequently, the average power dissipated in a logic circuit with two output states (output-low and output-high) is defined as

$$P_{CC(avg)} = \frac{I_{CC(OL)} + I_{CC(OH)}}{2} V_{CC} \tag{2.3.30}$$

Example 2.7: For the circuit in Figure 2.3.18 below, calculate the average power dissipation for this gate, if $I_{RB(OH)} = 1.55\,\text{mA}$, $I_{RC(OH)} = 24.7\,\mu\text{A}$, $I_{RCP(OH)} = 1.21\,\text{mA}$, $I_{RB(OL)} = 1.14\,\text{mA}$, $I_{RC(OL)} = 4.48\,\text{mA}$ and $I_{RCP(OL)} = 104\,\mu\text{A}$.

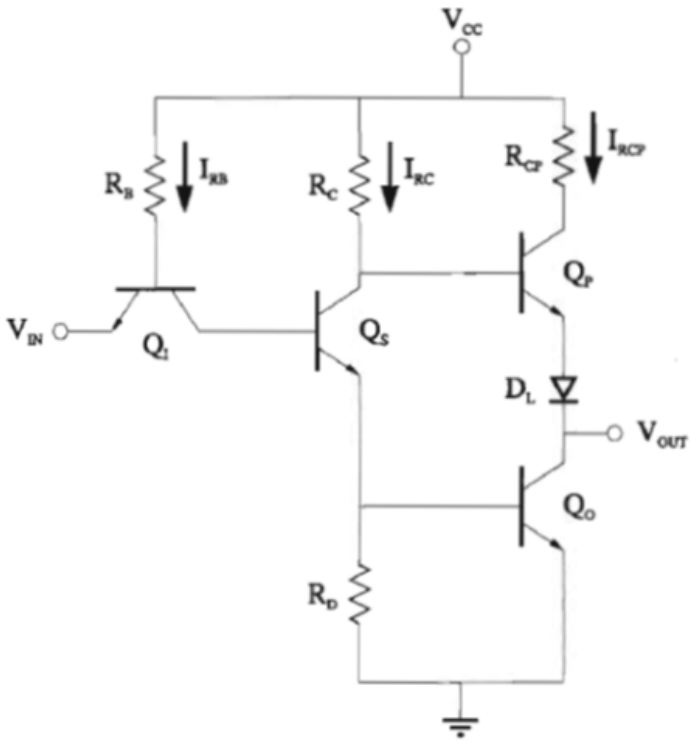


Figure 2.3.18: BJT logic gate for a power dissipation example.

2.4 Resistor-Transistor Logic (RTL)

2.4.1 Basic RTL Inverter

Resistor-Transistor Logic (RTL) which is introduced in 1962, is constructed from resistors and BJTs as shown in Figure 2.4.1(a) below.

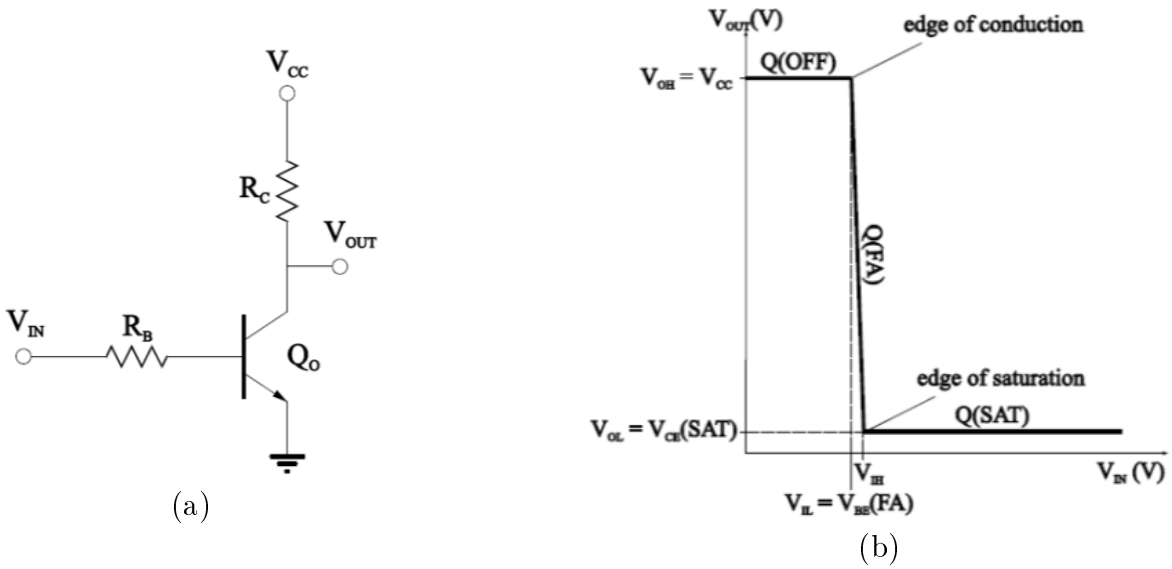


Figure 2.4.1: Basic RTL inverter: (a) Circuit, (b) Voltage transfer characteristics.

A basic RTL inverter and its VTC are shown in Figure 2.4.1(a) and Figure 2.4.1(b) above, respectively.

Here, Q_O is in cutoff (OFF) state when the input voltage is zero, i.e., $V_{IN} = 0$, consequently output is HIGH as $V_{OUT} = V_{CC}$ (because $I_C = 0$).

When the input voltage is enough, i.e., $V_{IN} = V_{BE(FA)}$, to turn on Q_O into the forward active (FA) mode, then current I_C will start to flow.

Hence, V_{OUT} starts to drop with increasing V_{IN} as $V_{OUT} = V_{CC} - I_C R_C$, $I_C = \beta_F I_B$ and $I_B = \frac{V_{IN} - V_{BE,O(FA)}}{R_B}$.

If we increase V_{IN} further, at some point (i.e., when $V_{IN} = V_{IH}$) Q_O goes into saturation. Consequently, output becomes LOW and remains constant at $V_{OUT} = V_{CE(SAT)}$.

We can summarize the state of the BJT transistor Q_O for output-high and output-low states as indicated in Table 2.5 below.

Table 2.5: State of active elements for output-high and output-low states in a basic RTL inverter.

Element	V_{OH}	V_{OL}
Q_O	Cutoff (OFF)	Saturated (SAT)

Thus,

$$V_{OH} = V_{CC} \tag{2.4.1}$$
$$V_{OL} = V_{CE(SAT)} \tag{2.4.2}$$
$$V_{IL} = V_{BE(FA)} \tag{2.4.3}$$
$$V_{IH} = I_{B(EOS)}R_B + V_{BE(EOS)} \tag{2.4.4}$$
$$= \frac{I_{C(EOS)}}{\beta_F}R_B + V_{BE(EOS)} \tag{2.4.5}$$
$$= \frac{V_{CC} - V_{CE(EOS)}}{\beta_F R_C}R_B + V_{BE(EOS)} \tag{2.4.6}$$

where EOS is **edge of saturation**, and hence $V_{BE(EOS)} = V_{BE(SAT)}$ and $V_{CE(EOS)} = V_{CE(SAT)}$.

2.4.2 Basic RTL NOR and NAND Gates

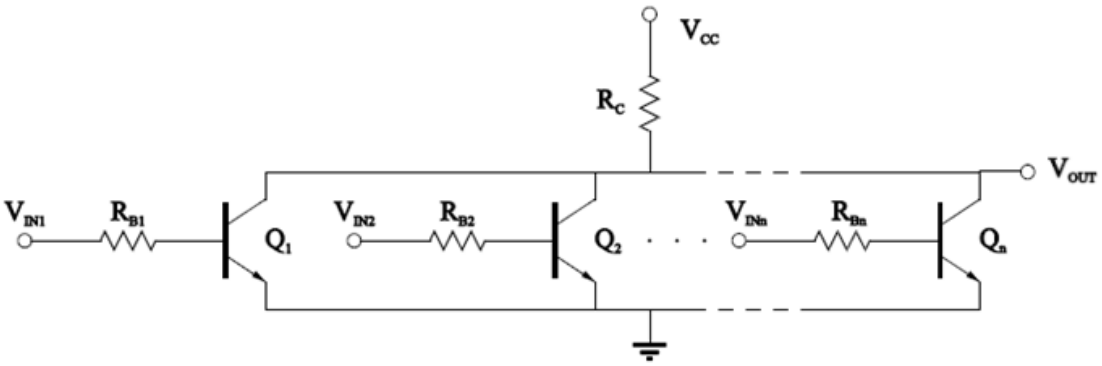


Figure 2.4.2: Basic RTL NOR gate.

Figure 2.4.2 above shows a basic RTL NOR gate.

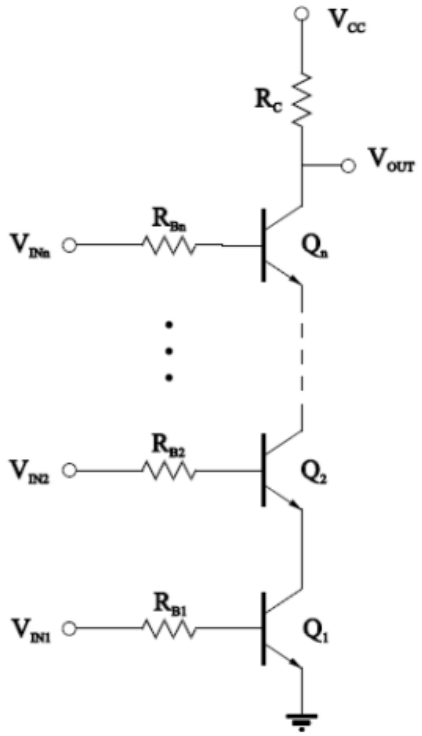


Figure 2.4.3: Basic RTL NAND gate.

Figure 2.4.3 above shows a basic RTL NAND gate.

Example 2.8: For the basic RTL NAND gate in Figure 2.4.3 above, determine the maximum fan-in if all stack BJTs have $V_{CE(SAT)} = 0.17\,\text{V}$ and all load gates have $V_{BE(FA)} = 0.7\,\text{V}$.

2.4.3 Basic RTL Fan-Out

When a basic RTL inverter is in **output-low** state, any load gate would be in cutoff mode and draw no input current.

Thus, maximum fan-out will be determined by the **output-high** state as shown in Figure 2.4.4 below.

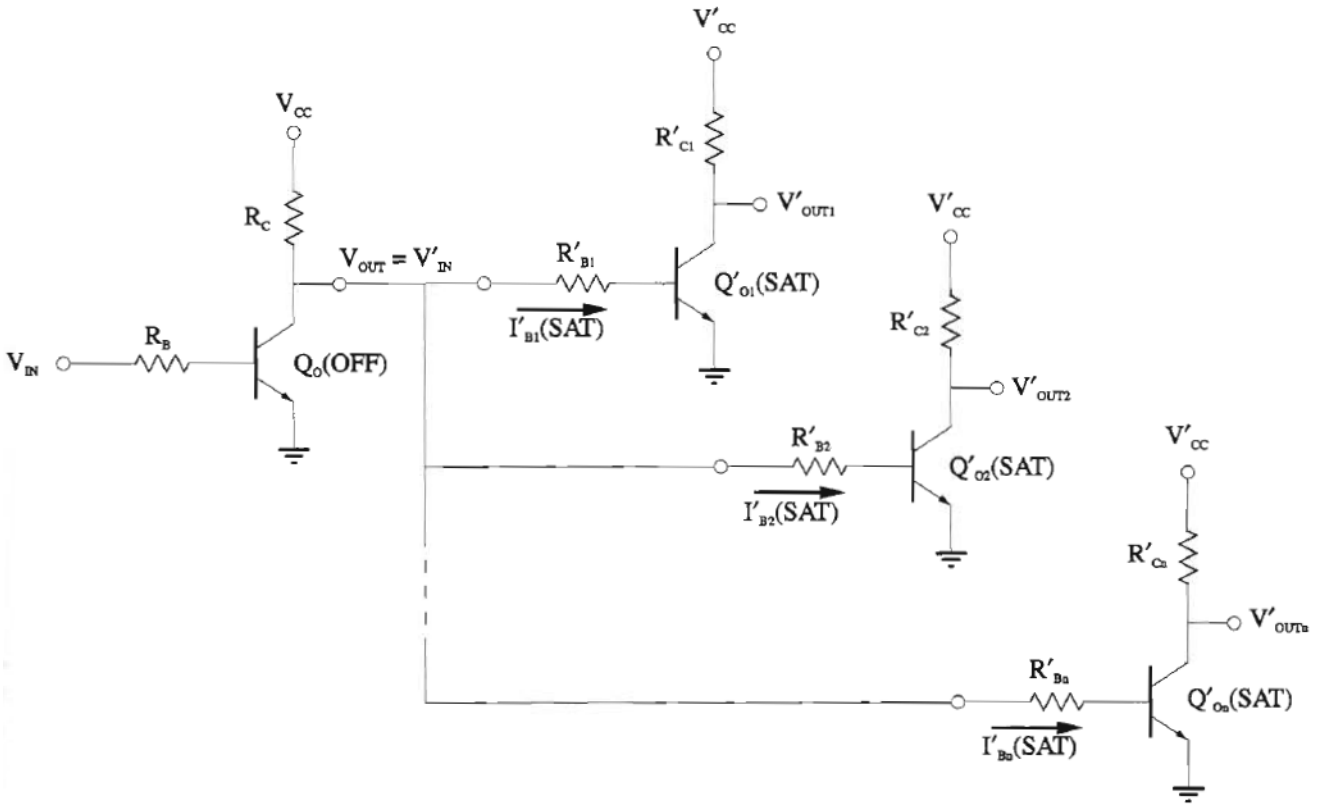


Figure 2.4.4: RTL Inverter in output high state with n identical load gates.

Output voltage is given by $V_{OH} = V_{CC} - I_{OH}R_C$ where $I_{OH} = I_{RC}$ and $V_{OUT} = V_{OH}$. So, $\boldsymbol{V_{OH}}$ is **not constant** and decreases with each added load gates, as the output current I_{OH} increases by each added load gate.

Thus, output current I_{OH} which is the sum of the identical input currents I'_{IH} of N load gates, is given by

$$I_{OH} = \frac{V_{CC} - V_{OH}}{R_C} = NI'_{IH} \tag{2.4.7}$$

where I'_{IH} is given by

$$I'_{IH} = \frac{V_{OH} - V'_{BE(SAT)}}{R'_B}. \tag{2.4.8}$$

Then, number of load gates, i.e., fan-out, (dropping the prime signs) is given by

$$N = \frac{V_{CC} - V_{OH}}{V_{OH} - V_{BE(SAT)}} \frac{R_B}{R_C} \tag{2.4.9}$$

Consequently, **maximum fan-out** is given by

$$N_{\max} = \left\lfloor \frac{V_{CC} - V_{OH(\min)}}{V_{OH(\min)} - V_{BE(SAT)}} \frac{R_B}{R_C} \right\rfloor \tag{2.4.10}$$

As $V_{OH(\min)} = V_{IH}$,

$$\boxed{N_{\max} = \left\lfloor \frac{V_{CC} - V_{IH}}{V_{IH} - V_{BE(SAT)}} \frac{R_B}{R_C} \right\rfloor} \tag{2.4.11}$$

Example 2.9: Determine the maximum fan-out for a basic RTL inverter with $V_{CC} = 5\,\text{V}$, $R_B = 10\,\text{k}\Omega$, $R_C = 1\,\text{k}\Omega$, $\beta_F = 25$, $V_{BE(SAT)} = 0.8\,\text{V}$ and $V_{CE(SAT)} = 0.2\,\text{V}$.

2.4.4 Basic RTL Power Dissipation

As $V_{OL} = V_{CE(SAT)}$ all load gates will be in cutoff mode. So, **output-low current supplied** is independent of load gates and given by

$$I_{CC(OL)} = \frac{V_{CC} - V_{CE,O(SAT)}}{R_C} \tag{2.4.12}$$

However, **output-high current supplied** depends on the number of load gates connected and given by

$$I_{CC(OH)} = \frac{V_{CC} - V'_{BE(SAT)}}{R_C + R'B/N} \tag{2.4.13}$$

If there is no load, $I_{CC(OH)} = 0$.

Consequently, **average power dissipation** is given by

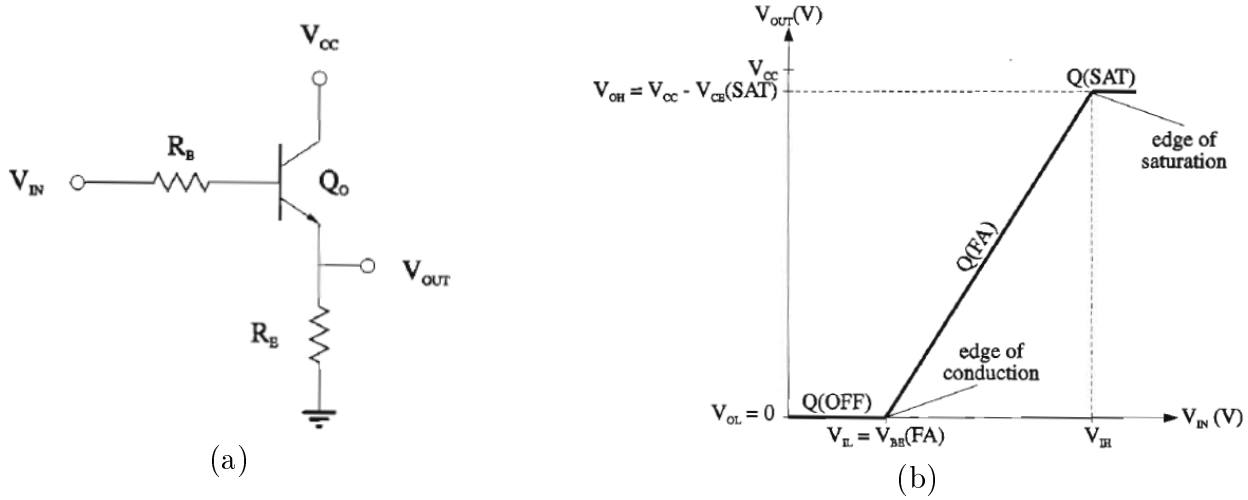
$$P_{CC(\text{avg})} = \frac{I_{CC(OL)} + I_{CC(OH)}}{2} V_{CC} \tag{2.4.14}$$

Example 2.10: Consider a basic RTL inverter with $V_{CC} = 5\,\text{V}$, $R_B = 10\,\text{k}\Omega$, $R_C = 1\,\text{k}\Omega$, $\beta_F = 25$, $V_{BE(SAT)} = 0.8\,\text{V}$ and $V_{CE(SAT)} = 0.2\,\text{V}$. Find the average power dissipated

a) no load

b) a fan-out of 1.

2.4.5 Basic RTL Non-Inverter



(a) (b)

Figure 2.4.5: Basic RTL non-inverter: (a) Circuit, (b) Voltage transfer characteristics.

For the basic RTL non-inverter shown in Figure 2.4.5 above

$$V_{OH} = V_{CC} - V_{CE(SAT)} \tag{2.4.15}$$
$$V_{OL} = 0\,\mathrm{V} \tag{2.4.16}$$
$$V_{IL} = V_{BE(FA)} \tag{2.4.17}$$
$$V_{IH} = I_{B(EOS)} R_B + V_{BC(EOS)} + V_{CC} \tag{2.4.18}$$
$$= \frac{I_{E(EOS)}}{\beta_F + 1} R_B + V_{BC(EOS)} + V_{CC} \tag{2.4.19}$$
$$= \frac{V_{CC} - V_{CE(EOS)}}{\beta_F + 1} \frac{R_B}{R_E} + V_{BC(EOS)} + V_{CC} \tag{2.4.20}$$

where EOS is **edge of saturation**, and hence $V_{BC(EOS)} = V_{BC(SAT)}$ and $V_{CE(EOS)} = V_{CE(SAT)}$.

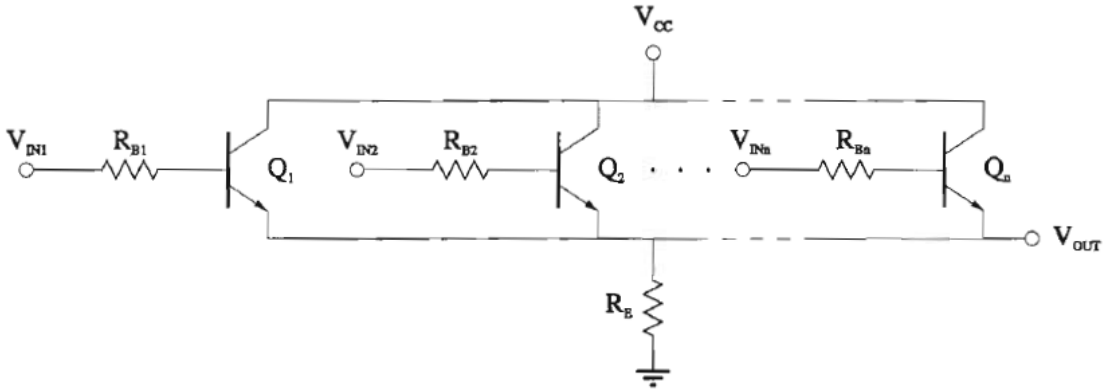


Figure 2.4.6: Basic RTL OR gate.

Figure 2.4.6 above shows a basic RTL OR gate.

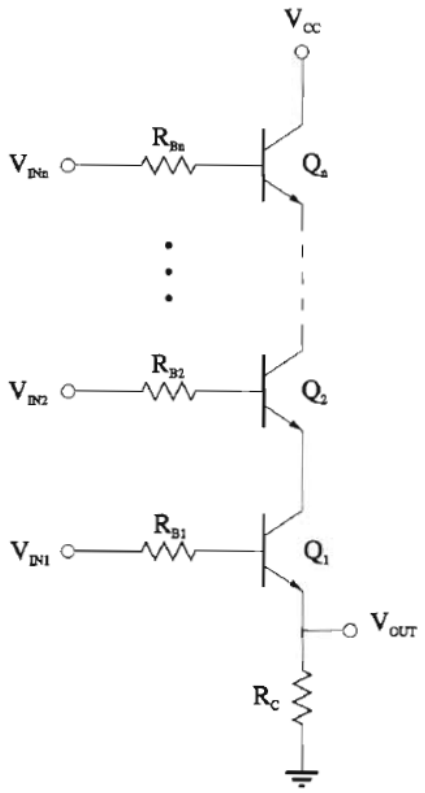


Figure 2.4.7: Basic RTL NAND gate.

Figure 2.4.7 above shows a basic RTL AND gate.

2.4.6 RTL with Active Pull-Up

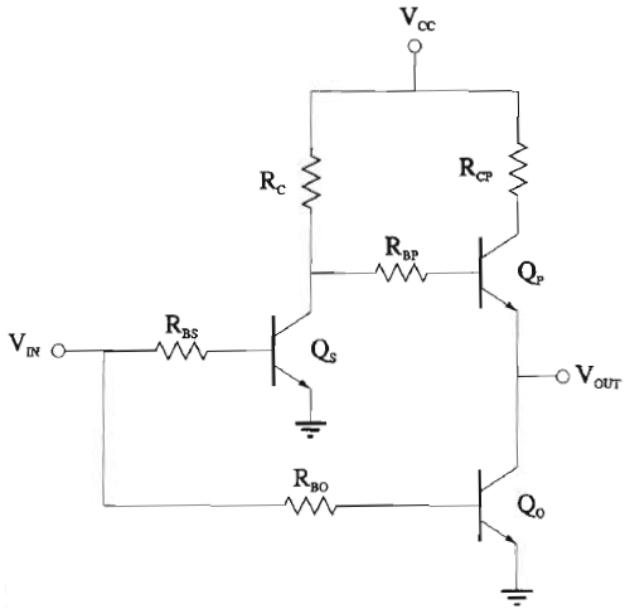


Figure 2.4.8: RTL inverter with active pull-up.

A method to increase the fan-out of RTL gates is to have an active pull-up configuration as shown in Figure 2.4.8 above, where the purpose of each element in the circuit is listed in Table 2.6 below.

Table 2.6: Purpose of each element for an RTL inverter with active pull-up

Element	Purpose
R_{BS},R_{BO}	Matched input resistors
Q_S	Drive splitter and pull-down of Q_P
R_C	Along with Q_S provides logic-inversion to output-high driver
R_{BP}	Limits base current to Q_P
Q_O	Output inverting BJT and active pull-down for output-low driver
Q_P	Provides active pull-up for output-high driver
R_{CP}	Part of active pull-up

The states of active elements are given in Table 2.7 below.

Table 2.7: State of active elements for output-high and output-low states in an RTL inverter with active pull-up.

Element	V_{OH}	V_{OL}
Q_O	Cutoff (OFF)	Saturated (SAT)
Q_S	Cutoff (OFF)	Saturated (SAT)
Q_P	Saturated (SAT) (for fan-out ≥ 1)	Cutoff (OFF)
	Edge of conduction (EOC) (for no load)	

2.4.7 RTL with Active Pull-Up Fan-Out

Maximum fan-out will be determined by the **output-high** state.

Output current $I_{OH} = I_{E,P(SAT)} = I_{C,P(SAT)} + I_{B,P(SAT)}$ which is the sum of the identical input currents I'_{IH} of N load gates, is given by

$$I_{OH} = \frac{V_{CC} - V_{CE,P(SAT)} - V_{OH}}{R_{CP}} + \frac{V_{CC} - V_{BE,P(SAT)} - V_{OH}}{R_C + R_{BP}} = NI'_{IH} \tag{2.4.21}$$

where I'_{IH} is

$$I'_{IH} = \frac{V_{OH} - V'_{BE(SAT)}}{R'_B/2}. \tag{2.4.22}$$

Then, number of load gates, i.e., fan-out, (dropping the prime signs) is given by

$$N = \frac{V_{CC} - V_{CE(SAT)} - V_{OH}}{V_{OH} - V_{BE(SAT)}} \frac{R_B}{2R_{CP}} + \frac{V_{CC} - V_{BE(SAT)} - V_{OH}}{V_{OH} - V_{BE(SAT)}} \frac{R_B}{2\left(R_C + R_{BP}\right)} \tag{2.4.23}$$

As $V_{OH(\min)} = V_{IH}$, **maximum fan-out** is given by

$$N_{\max} = \left\lfloor \frac{V_{CC} - V_{CE(SAT)} - V_{IH}}{V_{IH} - V_{BE(SAT)}} \frac{R_B}{2R_{CP}} + \frac{V_{CC} - V_{BE(SAT)} - V_{IH}}{V_{IH} - V_{BE(SAT)}} \frac{R_B}{2\left(R_C + R_{BP}\right)} \right\rfloor \tag{2.4.24}$$

If we ignore $I_{B,P(SAT)}$ (i.e., $(R_C + R_{BP}) \gg R_{CP}$), **maximum fan-out** simplifies to

$$\boxed{N_{\max} \approx \left\lfloor \frac{V_{CC} - V_{CE(SAT)} - V_{IH}}{V_{IH} - V_{BE(SAT)}} \frac{R_B}{2R_{CP}} \right\rfloor} \tag{2.4.25}$$

Example 2.11: Compare the maximum fan-out for the RTL inverter with active pull-up with that of basic RTL inverter where $V_{CC} = 5\,\text{V}$, $R_{BP} = R_{BS} = R_{BO} = 10\,\text{k}\Omega$, $R_C = 1\,\text{k}\Omega$, $R_{CP} = 100\,\Omega$, $V_{BE(SAT)} = 0.8\,\text{V}$, $V_{CE(SAT)} = 0.2\,\text{V}$ and $\beta_F = 25$.

2.5 Diode-Transistor Logic (DTL)

2.5.1 Basic DTL Inverter

Diode-Transistor Logic (DTL) which is introduced in 1964 in order to overcome the low fan-out of RTL, is constructed from diodes and BJTs as shown in Figure 2.5.1(a) below.

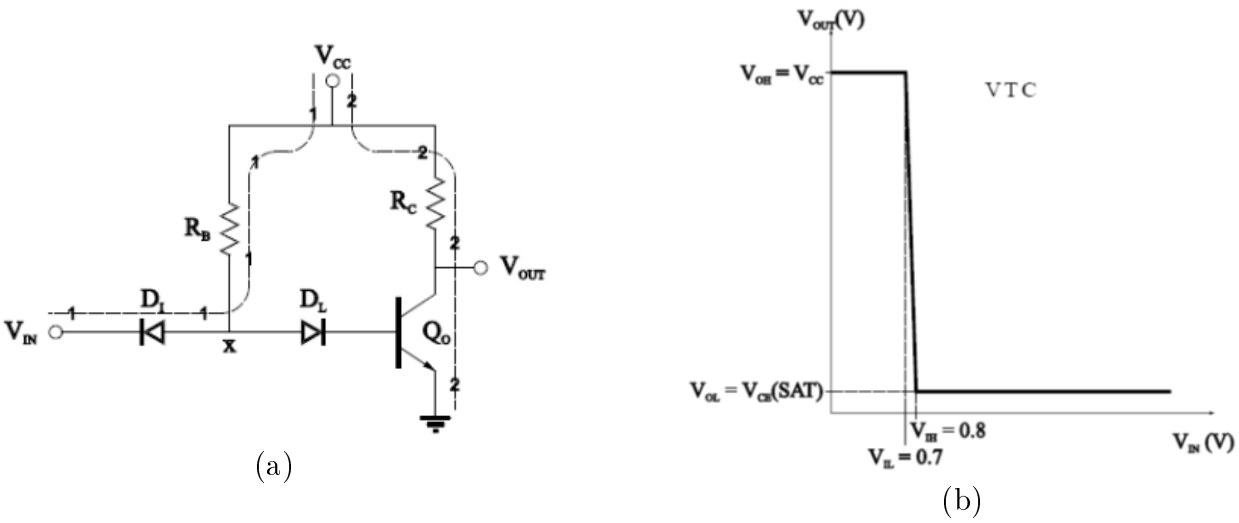


Figure 2.5.1: Basic DTL inverter: (a) Circuit, (b) Voltage transfer characteristics.

A basic DTL inverter and its VTC are shown in Figure 2.5.1(a) and Figure 2.5.1(b) above, respectively.

When the input is low, e.g., $V_{IN} = 0\,\text{V}$, input diode D_I is forward biased so the voltage V_x between the diodes will be $V_x = V_{IN} + V_{D,I(ON)}$ and thus as $V_{BE,O} = V_x - V_{D,L(ON)} = V_{IN}$, output transistor Q_O will be in **cutoff** mode. Consequently, output is HIGH as $V_{OUT} = V_{CC}$ (because $I_C = 0$)

$$V_x = V_{IN} + V_{D,I(ON)} \qquad (\text{while } V_{IN} < V_{BE(SAT)}) \tag{2.5.1}$$

$$V_{BE,O} = V_x - V_{D,L(ON)} \tag{2.5.2}$$

$$V_{BE,O} = V_{IN} \tag{2.5.3}$$

When the input voltage is high enough, i.e., $V_{IN} = V_{BE(FA)}$, to turn on Q_O into the forward active (FA) mode, then current I_C will start to flow.

Hence, V_{OUT} starts to drop with increasing V_{IN} as $V_{OUT} = V_{CC} - I_C R_C$.

If we increase V_{IN} further, at some point (i.e., when $V_{IN} = V_{BE(SAT)}$), Q_O goes into saturation and D_I starts to turn off. As a result, V_{OUT} becomes LOW and remains constant at $V_{OUT} = V_{CE,O(SAT)}$.

We can summarize the state of the active elements for output-high and output-low states as indicated in Table 2.8 below.

Table 2.8: State of active elements for output-high and output-low states in a basic DTL inverter.

Element	V_{OH}	V_{OL}
Q_O	Cutoff (OFF)	Saturated (SAT)
D_L	Edge of Conduction (EOC)	Conducting (ON)
D_I	Conducting (ON)	Cutoff (OFF)

Thus,

$$V_{OH} = V_{CC} \tag{2.5.4}$$
$$V_{OL} = V_{CE(SAT)} \tag{2.5.5}$$
$$V_{IL} = V_{BE(FA)} \tag{2.5.6}$$
$$V_{IH} = V_{BE(SAT)} \tag{2.5.7}$$

2.5.2 Basic DTL NAND Gate

NAND function is inherently provided by the DTL logic family by adding diodes in parallel at the input pointing outward (i.e., towards the input) as shown in Figure 2.5.2 below for a two-input basic DTL NAND gate.

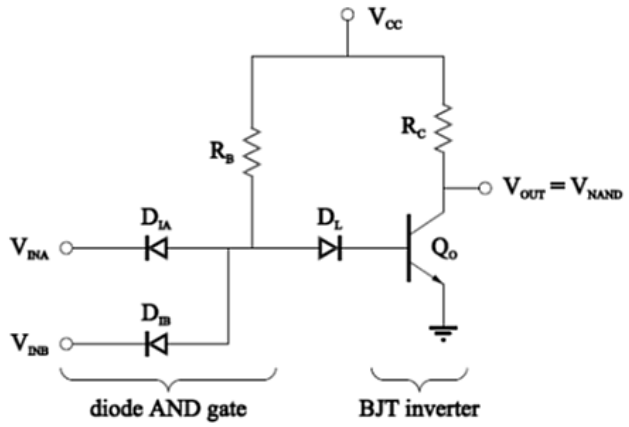


Figure 2.5.2: Basic DTL NAND gate.

Example 2.12: Consider the DTL NAND gate in Figure 2.5.2 above, and determine

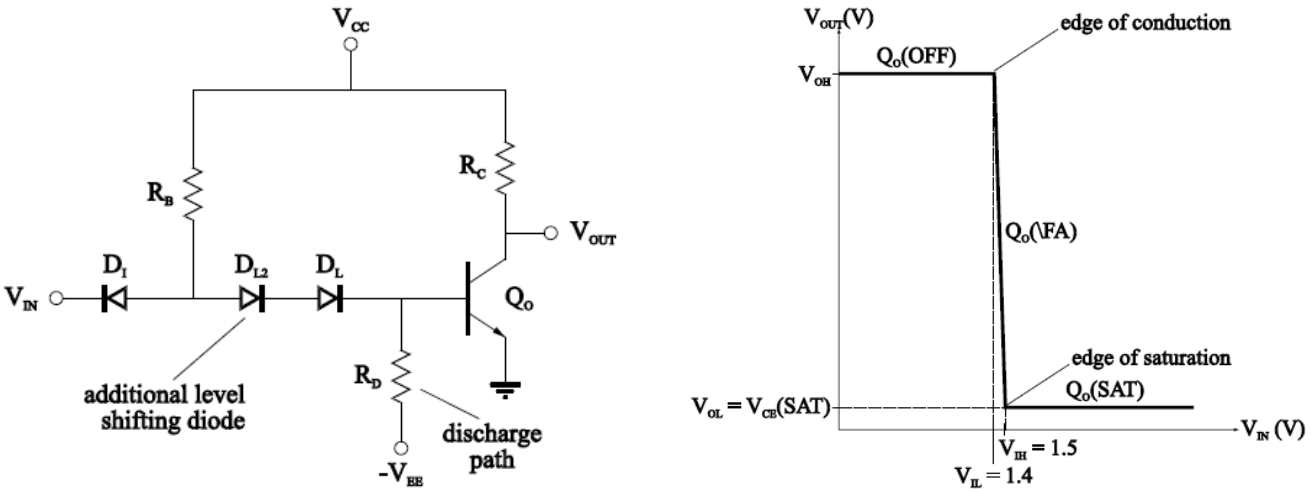
a) Truth table for V_{INA}, V_{INB} and V_{OUT} (using LOW-HIGH states),

b) States of D_{IA}, D_{IB} and Q_O when $V_{INA} = 0.4\,\text{V}$ and $V_{INB} = 0.7\,\text{V}$,

c) States of D_{IA}, D_{IB} and Q_O when $V_{INA} = 0.3\,\text{V}$ and $V_{INB} = 0.4\,\text{V}$,

d) States of D_{IA}, D_{IB} and Q_O when $V_{INA} = 0.53\,\text{V}$ and $V_{INB} = 0.55\,\text{V}$.

2.5.3 Diode Modified DTL



(a) (b)

Figure 2.5.3: Modified DTL inverter with additional level-shifting diode and discharge path: (a) Circuit, (b) Voltage transfer.

As shown in Figure 2.5.3(a) above, basic DTL inverter can be improved by

- by an additional diode D_{L2} to improve noise-margin-low V_{NML}.
- by an additional discharge path (consisting of R_D and $-V_{EE}$) to the base of Q_O to improve the switching time from saturation to cutoff (i.e., to increase the low-to-high switching speed).

2.5.4 Transistor Modified DTL

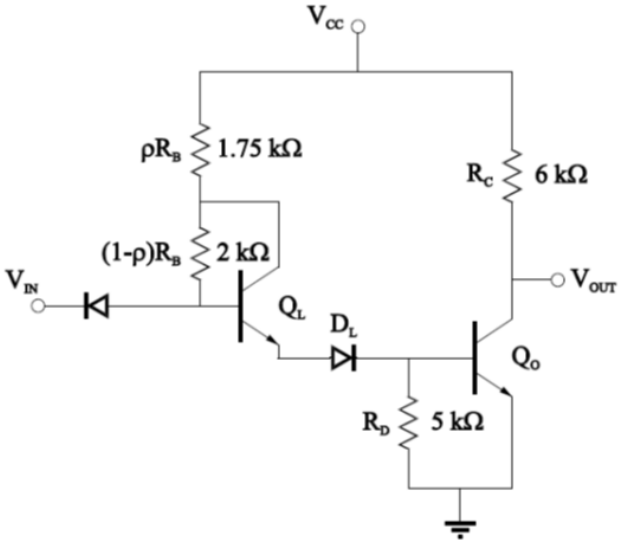


Figure 2.5.4: Transistor modified DTL inverter.

The fan-out of the modified DTL in Figure 2.5.3(a) can be further increased by replacing D_{L2} with a self-biased BJT Q_L (prevented from going into saturation mode by ensuring always

$V_{BC} < 0$) as shown in Figure 2.5.4 above, where the purpose of each element in the circuit is listed in Table 2.9 below.

Table 2.9: Purpose of each element for a transistor-modified DTL inverter

Element	**Purpose**
D_I	Input diode, provides ANDing and limits I_{IH}
ρR_B	Limits I_{IL}
$(1-\rho)R_B$	Self-biases Q_L and prevents Q_L from saturation
Q_L	Level shifting to improve V_{NML} and provides base driving current Q_O
D_L	Level-shifting diode for shifting transition width
R_D	Provides discharge path for saturation stored charge removal from base of Q_O
Q_O	Output inverting BJT and active pull-down for output-low driver
R_C	Part of passive pull-up

The states of active elements in a transistor modified DTL inverter are given in Table 2.10 below.

Table 2.10: State of active elements for output-high and output-low states in a transistor modified DTL inverter.

Element	$\boldsymbol{V_{OH}}$	$\boldsymbol{V_{OL}}$
Q_O	Cutoff (OFF)	Saturated (SAT)
D_L	Cutoff (OFF)	Conducting (ON)
Q_L	Cutoff (OFF)	Forward Active (FA)
D_I	Conducting (ON)	Cutoff (OFF)

Thus,

$$V_{OH} = V_{CC} \tag{2.5.8}$$
$$V_{OL} = V_{CE,O(SAT)} \tag{2.5.9}$$
$$V_{IL} = V_{BE,L(FA)} + V_{BE,O(FA)} \tag{2.5.10}$$
$$V_{IH} = V_{BE,L(FA)} + V_{BE,O(SAT)} \tag{2.5.11}$$

2.5.5 DTL NAND Gate

NAND function is inherently provided by the DTL logic family by adding diodes in parallel at the input pointing outward as shown in Figure 2.5.5 below.

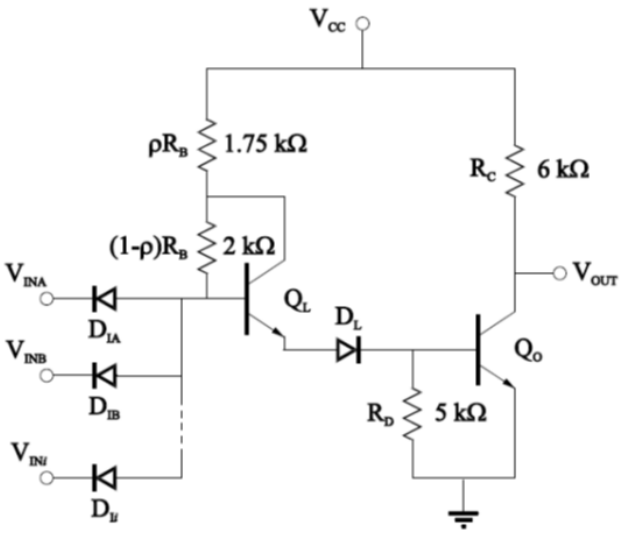


Figure 2.5.5: DTL NAND gate.

2.5.6 DTL Fan-Out

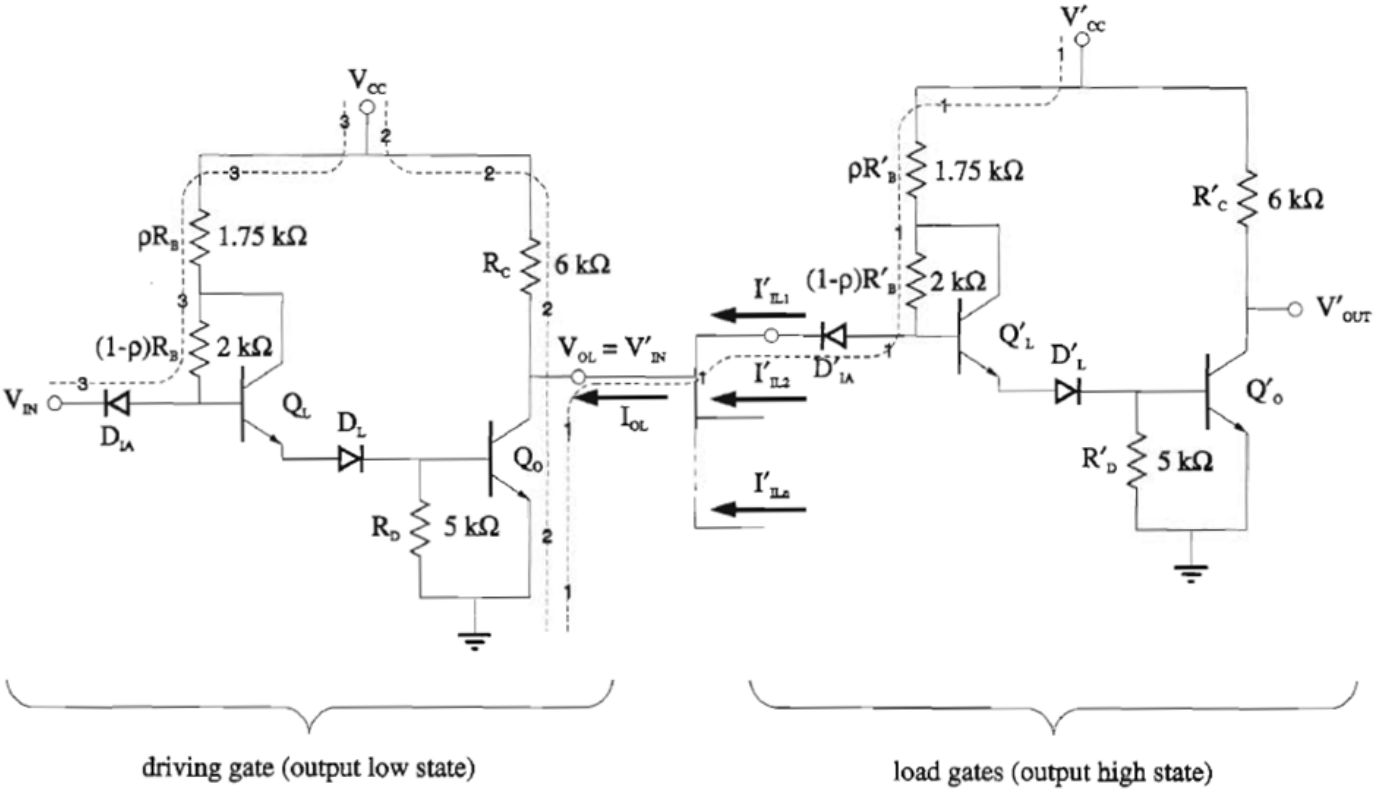


Figure 2.5.6: DTL NAND gate in output-low state driving N identical load gates.

Maximum fan-out will be determined by the **output-low** state, as when output is high input diode D'_I is cutoff (i.e., $I'_{IH} = 0$).

From Path 2 and Path 1,

$$I_{OL} = I_{C,O(SAT)} - I_{RC(OL)} \tag{2.5.12}$$

$$I_{RC(OL)} = \frac{V_{CC} - V_{CE,O(SAT)}}{R_C} \tag{2.5.13}$$

$$I_{C,O(SAT)} = \sigma\beta_F I_{B,O(SAT)} \tag{2.5.14}$$

Continuing,

$$I_{B,O(SAT)} = I_{E,L(FA)} - I_{RD(OL)} \tag{2.5.15}$$

$$I_{RD(OL)} = \frac{V_{BE,O(SAT)}}{R_D} \tag{2.5.16}$$

$$I_{E,L(FA)} = \frac{V_{CC} - V_{BE,L(FA)} - V_{D,L(ON)} - V_{BE,O(SAT)}}{\rho R_B + (1-\rho)\, R_B/\left(\beta_F + 1\right)} \tag{2.5.17}$$

$$\approx \frac{V_{CC} - V_{BE,L(FA)} - V_{D,L(ON)} - V_{BE,O(SAT)}}{\rho R_B} \tag{2.5.18}$$

From Path 1,

$$I'_{IL} = \frac{V_{CC} - V_{D,I(ON)} - V_{CE,O(SAT)}}{R_B} \tag{2.5.19}$$

Thus, the **maximum fan-out** is given by

$$N_{\max} = \left\lfloor \frac{I_{OL(\max)}}{I'_{IL}} \right\rfloor = \left\lfloor \frac{I_{C,O(SAT)(\max)} - I_{RC(OL)}}{I'_{IL}} \right\rfloor \tag{2.5.20}$$

$$= \left\lfloor \frac{\sigma_{\max}\beta_F I_{B,O(SAT)} - I_{RC(OL)}}{I'_{IL}} \right\rfloor \tag{2.5.21}$$

Example 2.13: For the DTL gate in Figure 2.5.4, determine the maximum fan-out for $\beta_F = 49$ and $\sigma_{\max} = 0.85$.

2.5.6.1 DTL Power Dissipation

Example 2.14: Calculate the average power dissipation for Example 2.13 above?

2.6 Transistor-Transistor Logic (TTL)

2.6.1 Basic TTL Inverter

Transistor-Transistor Logic (TTL) which is introduced in 1965 in order to provide increased fan-out, improved transient response and reduced chip area.

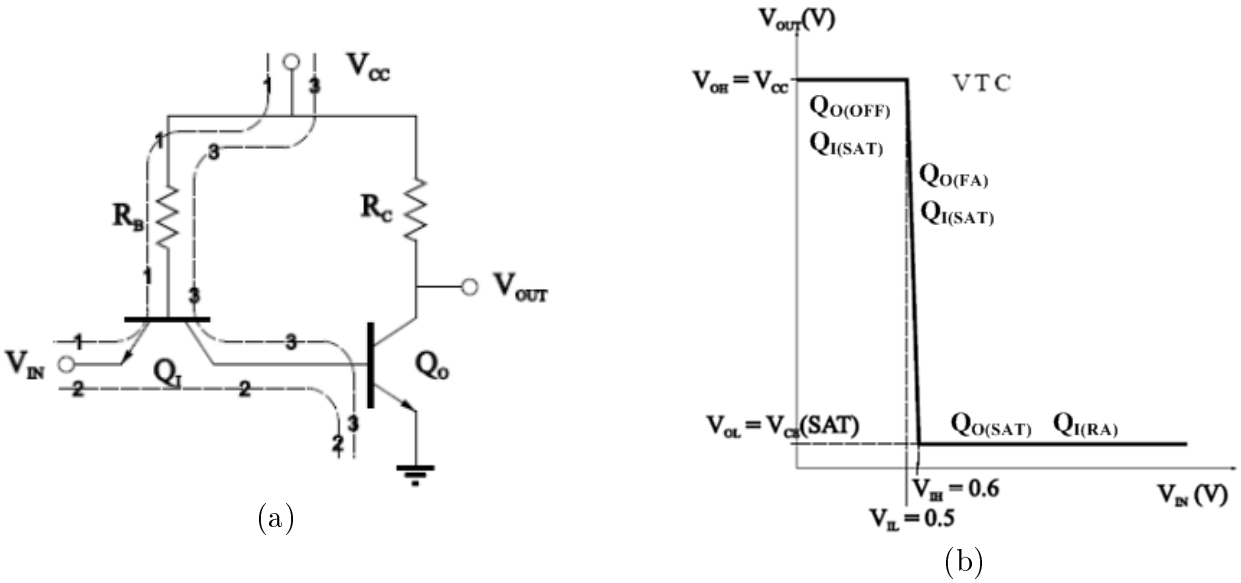


Figure 2.6.1: Basic TTL inverter: (a) Circuit, (b) Voltage transfer characteristics.

A basic TTL inverter and its VTC are shown in Figure 2.6.1(a) and Figure 2.6.1(b) above, respectively.

Compare the TTL inverter in Figure 2.6.1(a) with the DTL inverter in Figure 2.5.1(a) in order to see how diodes D_I and D_L are represented by the base-emitter and base-collector junctions of the input transistor Q_I which replaced these two diodes.

When the input is low, e.g., $V_{IN} = 0\,\text{V}$, base-emitter junction of Q_I is forward biased, however voltage at the base of Q_I is not enough to turn on both base-collector junction of Q_I and base-emitter junction of Q_O, so Q_O is **cutoff**. So, collector current of Q_I is zero, i.e., $I_{C,I} = 0$. Thus, Q_I is in **saturation** mode (as $I_C < \beta_F I_B$).

$$V_{BE,O} = V_{IN} + V_{CE,I(SAT)} \qquad (\text{while } V_{IN} < V_{IH}) \tag{2.6.1}$$

As Q_O is in **cutoff** mode when $V_{IN} = 0\,\text{V}$, the output is HIGH as $V_{OUT} = V_{CC}$.

When the input voltage is high enough, i.e., $V_{IN} = V_{BE(FA)} - V_{CE(SAT)}$, Q_O goes into the forward active (FA) mode and current I_{RC} will start to flow. Then, V_{OUT} starts to drop with increasing V_{IN} as $V_{OUT} = V_{CC} - I_{RC}R_C$.

If we increase V_{IN} further, at some point (i.e., when $V_{IN} = V_{BE(SAT)} - V_{CE(SAT)}$), Q_O goes into saturation and Q_I goes into reverse-active mode. As a result, V_{OUT} becomes LOW and remains constant at $V_{OUT} = V_{CE,O(SAT)}$.

We can summarize the state of the active elements for output-high and output-low states as indicated in Table 2.11 below.

Table 2.11: State of active elements for output-high and output-low states in a basic TTL inverter.

Element	V_{OH}	V_{OL}
Q_O	Cutoff (OFF)	Saturated (SAT)
Q_I	Saturated (SAT)	Reverse Active (RA)

Thus,

$$V_{OH} = V_{CC} \tag{2.6.2}$$
$$V_{OL} = V_{CE,O(SAT)} \tag{2.6.3}$$
$$V_{IL} = V_{BE,O(FA)} - V_{CE,I(SAT)} \tag{2.6.4}$$
$$V_{IH} = V_{BE,O(SAT)} - V_{CE,I(SAT)} \tag{2.6.5}$$

2.6.2 Basic TTL NAND Gate

NAND function is inherently provided by the TTL logic family by using a multiple-emitter BJT (ensuring a much-less chip area) as shown in Figure 2.6.2 below for a three-input basic TTL NAND gate.

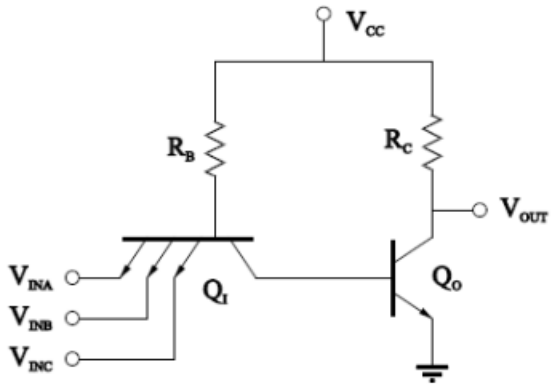


Figure 2.6.2: Basic TTL NAND gate.

2.6.3 Standard TTL NAND Gate

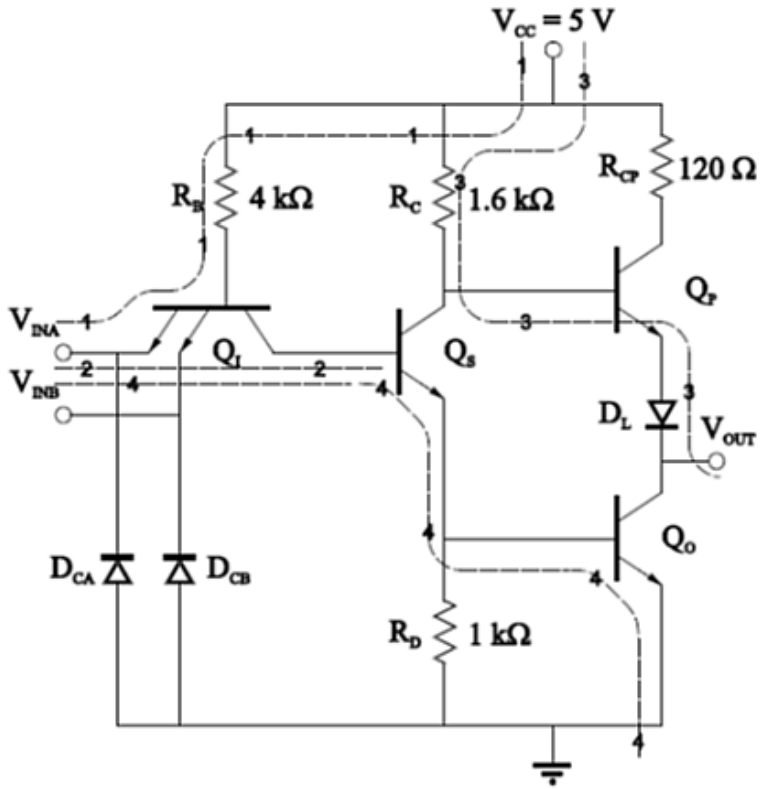


Figure 2.6.3: Standard TTL 5400/7400 series NAND gate with totem-pole output.

Basic TTL inverter can be improved by adding a **totem-pole output** (stacking of two BJTs, a resistor and diode in the output branch) to provide active pull-up and pull-down sections, a drive-splitter transistor Q_S, a discharge resistor R_D and clamping diodes at the inputs as shown in Figure 2.6.3 above. The purpose of each element in the circuit is listed in Table 2.12 below.

Table 2.12: Purpose of each element for a standard TTL NAND gate with totem-pole output

Element	**Purpose**
Q_I	Multi-emitter input BJT, level-shifting of transition width and pull-down of Q_S
R_B	Limits I_{IL}
Q_S	Drive splitter, provides base driving current Q_O, level-shifting of transition width and pull-down of Q_P
R_C	Along with Q_S provides logic inversion to output-high driver
Q_O	Output inverting BJT and active pull-down for output-low driver
D_L	Diode level shifting to output-high output and ensuring output high driver is off in the output-low state
R_D	Provides discharge path for saturation stored charge removal from base of Q_O
Q_P	Provides active pull-up for output-high driver
R_{CP}	Part of active pull-up and limits current-spikes during high-to-low transitions
D_{CA}, D_{CB}	Input clamping diodes to limit the negative voltage swing of the inputs

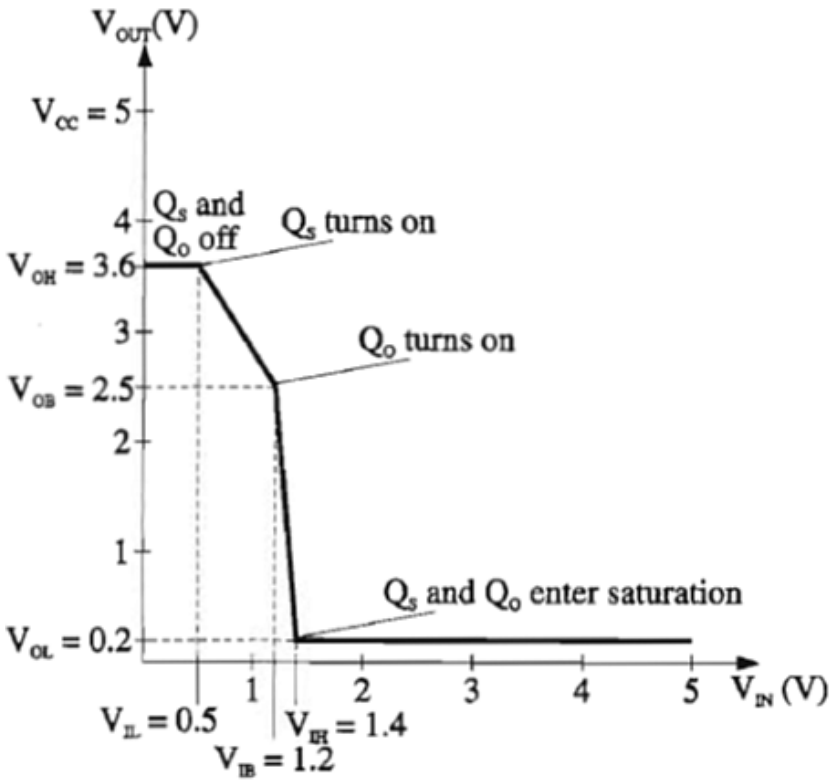


Figure 2.6.4: Voltage transfer characteristics of a standard TTL inverter given in Figure 2.6.3.

When the input is low, e.g., $V_{IN} = 0\,\text{V}$, base-emitter junction of Q_I is forward biased, however voltage at the base of Q_I is not enough to turn on both base-collector junction of Q_I and base-

emitter junction of Q_S, so Q_S and Q_O are **cutoff**. So, collector current of Q_I is zero and Q_I is in **saturation** mode.

When $V_{IN} = 0\,\text{V}$, Q_S and Q_O are in **cutoff** mode and Q_P is in edge-of-conduction (EOC) mode (i.e., no current flows as there is no-load). So, as $I_{RC(OH)} = I_{B,P(EOC)} = 0$, the output is HIGH and given as

$$V_{OUT} = V_{CC} - I_{RC(OH)}R_C - V_{BE,P(EOC)} - V_{D,L(EOC)} \tag{2.6.6}$$
$$= V_{CC} - V_{BE,P(FA)} - V_{D,L(ON)} \tag{2.6.7}$$

When the input voltage is high enough, i.e., $V_{IN} = V_{BE,S(FA)} - V_{CE,I(SAT)}$, Q_S goes into the forward active (FA) mode and current I_{RC} will start to flow. Then, V_{OUT} starts to drop with increasing V_{IN} as $V_{OUT} = V_{CC} - I_{RC}R_C - V_{BE,P(EOC)} - V_{D,L(EOC)}$.

If we increase V_{IN} further, then at some point (i.e., when $V_{IN} = V_{BE,O(FA)} + V_{BE,S(FA)} - V_{CE,I(SAT)}$), Q_O turns into forward active mode. As a result, V_{OUT} decreases more rapidly as $I_{C,O}$ also starts to flow and more current starts to flow from R_C. This point is called the **break point**. The input and output voltages at the break point are labelled as V_{IB} and V_{OB}, respectively.

If V_{IN} is kept increasing, then at some point (i.e., when $V_{IN} = V_{BE,O(SAT)} + V_{BE,S(SAT)} - V_{CE,I(SAT)}$), both Q_S and Q_O go into the saturation mode, Q_P goes into cutoff mode and Q_I goes into the reverse-active mode. As a result, V_{OUT} becomes LOW and remains constant at $V_{OUT} = V_{CE,O(SAT)}$.

The states of active elements in a standard TTL inverter are given in Table 2.13 below.

Table 2.13: State of active elements for output-high and output-low states in a standard TTL inverter.

Element	$\boldsymbol{V_{OH}}$	$\boldsymbol{V_{OB}}$	$\boldsymbol{V_{OL}}$
Q_O	Cutoff (OFF)	Edge of conduction (EOC)	Saturated (SAT)
Q_S	Cutoff (OFF)	Forward active (FA)	Saturated (SAT)
Q_I	Saturated (SAT)	Saturated (SAT)	Reverse active (RA)
Q_P	Edge of conduction (EOC)	Edge of conduction (EOC)	Cutoff (OFF)
D_L	Edge of conduction (EOC)	Edge of conduction (EOC)	Cutoff (OFF)

Thus,

$$V_{OH} = V_{CC} - V_{BE,P(FA)} - V_{D,L(ON)} \tag{2.6.8}$$

$$V_{OB} = V_{CC} - I_{C,S(FA)} R_C - V_{BE,P(FA)} - V_{D,L(ON)} \tag{2.6.9}$$

$$= V_{CC} - \frac{V_{BE,O(FA)}}{R_D} R_C - V_{BE,P(FA)} - V_{D,L(ON)} \tag{2.6.10}$$

$$V_{OL} = V_{CE,O(SAT)} \tag{2.6.11}$$

$$V_{IL} = V_{BE,S(FA)} - V_{CE,I(SAT)} \tag{2.6.12}$$

$$V_{IB} = V_{BE,O(FA)} + V_{BE,S(FA)} - V_{CE,I(SAT)} \tag{2.6.13}$$

$$V_{IH} = V_{BE,O(SAT)} + V_{BE,S(SAT)} - V_{CE,I(SAT)} \tag{2.6.14}$$

Example 2.15: For the TTL gate in Figure 2.6.3, determine the VTC critical points V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_{IB} and V_{OB} for $\beta_F = 100$ and $\sigma_{\max} = 0.85$.

2.6.4 TTL Fan-Out

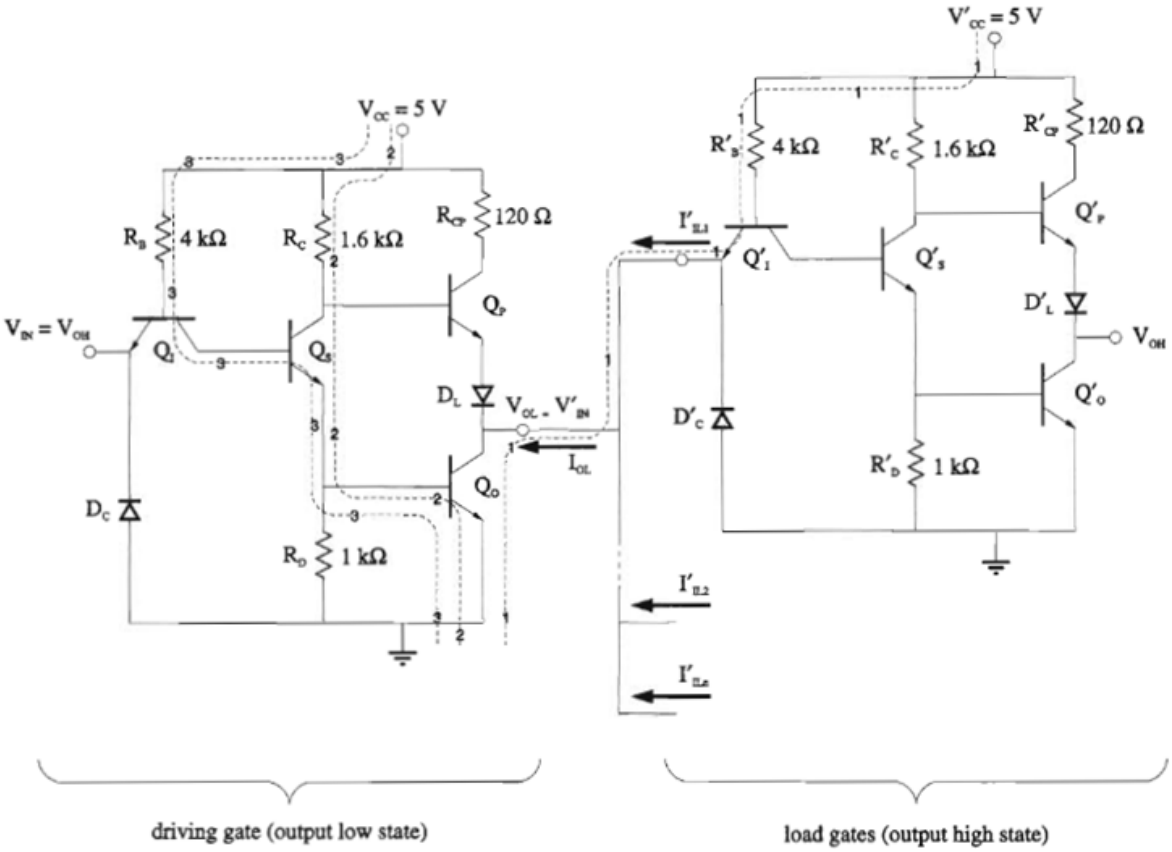


Figure 2.6.5: TTL NAND gate in output-low state driving N identical load gates.

Maximum fan-out will be determined by the **output-low** state, as when output is high input transistor Q'_I is in reverse active mode (i.e., $I'_{IH} = 0$).

From Path 1,

$$I_{OL} = I_{C,O(SAT)} - I_{D,L(EOC)} = I_{C,O(SAT)} \tag{2.6.15}$$

$$I_{C,O(SAT)} = \sigma\beta_F I_{B,O(SAT)} \tag{2.6.16}$$

Continuing

$$I_{B,O(SAT)} = I_{E,S(SAT)} - I_{RD(OL)} \tag{2.6.17}$$

$$I_{RD(OL)} = \frac{V_{BE,O(SAT)}}{R_D} \tag{2.6.18}$$

$$I_{E,S(SAT)} = I_{C,S(SAT)} + I_{B,S(SAT)} \tag{2.6.19}$$

$$I_{C,S(SAT)} = \frac{V_{CC} - V_{CE,S(SAT)} - V_{BE,O(SAT)}}{R_C} \qquad \text{(from Path 2)} \tag{2.6.20}$$

From Path 3,

$$I_{B,S(SAT)} = I_{C,I(RA)} \tag{2.6.21}$$

$$= (1 + \beta_R) I_{B,I(RA)} \tag{2.6.22}$$

$$I_{B,I(RA)} = \frac{V_{CC} - V_{BC,I(RA)} - V_{BE,S(SAT)} - V_{BE,O(SAT)}}{R_B} \tag{2.6.23}$$

From Path 1,

$$I'_{IL} = \frac{V_{CC} - V_{BE,I(SAT)} - V_{CE,O(SAT)}}{R_B} \tag{2.6.24}$$

Thus, the **maximum fan-out** is given by

$$N_{\max} = \left\lfloor \frac{I_{OL(\max)}}{I'_{IL}} \right\rfloor = \left\lfloor \frac{I_{C,O(SAT)(\max)}}{I'_{IL}} \right\rfloor \tag{2.6.25}$$

$$= \left\lfloor \frac{\sigma_{\max}\beta_F I_{B,O(SAT)}}{I'_{IL}} \right\rfloor \tag{2.6.26}$$

Example 2.16: For the TTL gate in Figure 2.6.3, determine the maximum fan-out for $\beta_F = 25$, $\beta_R = 0.1$ and $\sigma_{\max} = 0.85$.

2.6.4.1 TTL Power Dissipation

Example 2.17: Calculate the average power dissipation for Example 2.16 above?

2.6.5 Open-Collector TTL

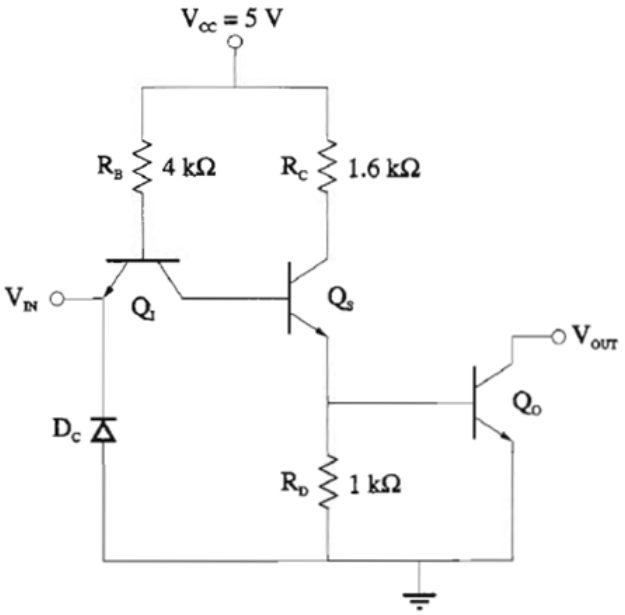


Figure 2.6.6: Open-collector TTL gate.

Open-collector TTL gates, one of which is shown in Figure 2.6.6 above, are often used in data busses where multiple gate outputs must be ANDed.

- This can be accomplished by using a single pull-up resistor with open-collector TTL gates.
- This type of connection is referred to as **wired-AND**.

2.6.6 Low Power TTL (LTTL)

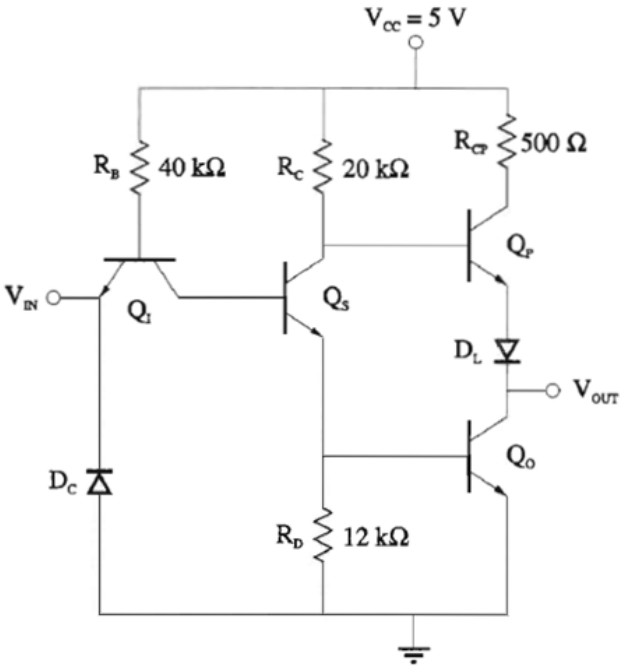


Figure 2.6.7: Low power TTL (LTTL) with increased resistances.

Power dissipation can be lowered by just **increasing** the **resistance** values as shown in Figure 2.6.7 above.

However, this results in:

- decreased fan-out,
- longer transient response times.

Example 2.18: Calculate the average power dissipation for LTTL in Figure 2.6.7 and compare it with that of TTL which was calculated in Example 2.17.

2.6.7 High Speed TTL (HTTL)

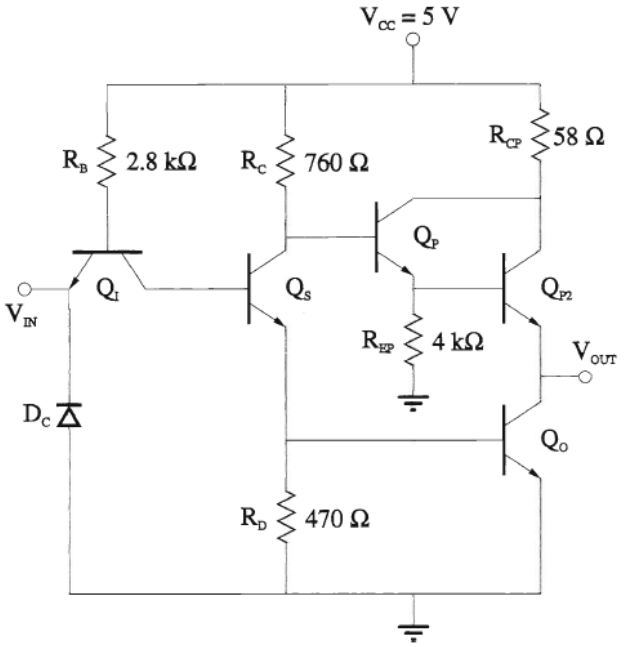


Figure 2.6.8: 54H00/74H00 high-speed TTL (LTTL) with smaller resistances and Darlington pair active pull-up driver.

Switching speed can be increased by just **decreasing** the **resistance** values as shown in Figure 2.6.8 above. An additional Darlington pair is also used to improve the low-to-high switching speed, together with R_{EP} resistor which provides a discharge path for Q_{P2} in order to improve the high-to-low switching speed.

However, this results in

- increased power dissipation.

2.7 Other TTL Gates

In this section, we are going to investigate the following TTL gates

- AND gates
- NOR gates
- OR gates
- AND-OR-INVERT (AOI) gates
- XOR gates
- Schmitt Trigger Inverters and NAND gates
- Tri-State buffers

2.7.1 AND Gate

NAND gate will become an AND date, if the output drivers are enabled in the inverse fashion. This is accomplished by using an **inverting driver splitter** as shown in the block diagram of Figure 2.7.1 below.

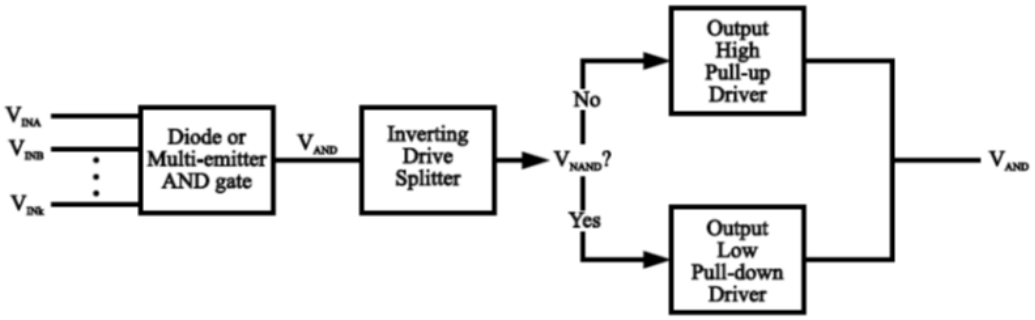


Figure 2.7.1: Block diagram of a TTL AND gate.

This second level inversion is accomplished by Q_{S2}, Q_{SD}, D_S, R_{SD} and R_{CS} which are enclosed in the shaded block in Figure 2.7.2 below. Circuit symbol and VTC for a TTL AND gate are also displayed in Figure 2.7.3 and Figure 2.7.4, respectively.

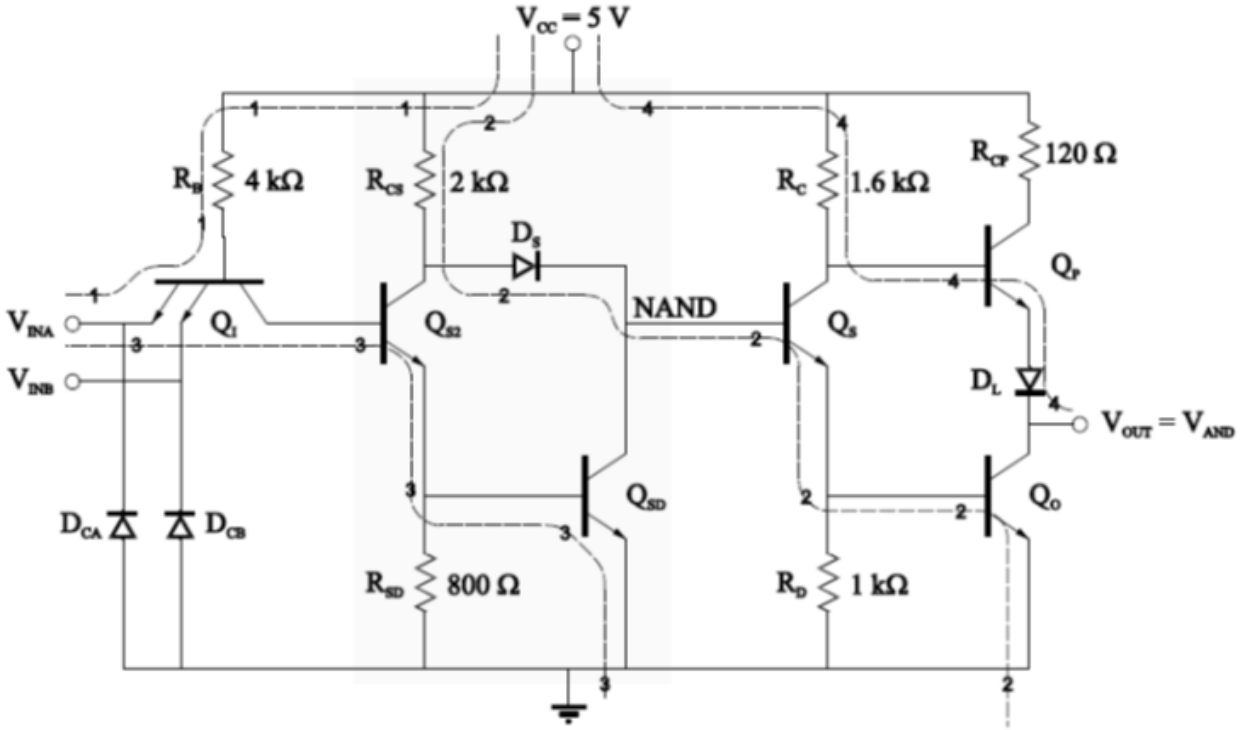


Figure 2.7.2: Circuit schematic of a standard 5408/7408 TTL AND gate.

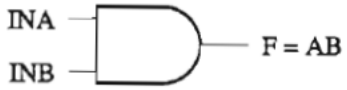


Figure 2.7.3: Circuit symbol of a TTL AND gate.

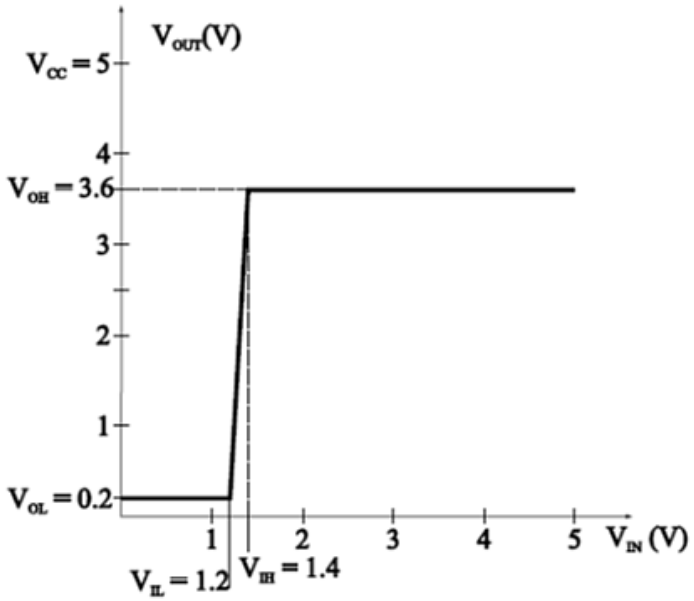


Figure 2.7.4: Voltage transfer characteristics of a standard TTL AND gate given in Figure 2.7.2.

When the input is low, e.g., $V_{IN} = 0\,\text{V}$, Q_I is saturated, Q_{S2} and Q_{SD} are cutoff. Consequently, Q_S and Q_O are saturated, and Q_P and D_L are cutoff. So, the output is LOW, i.e., $V_{OL} = V_{CE,O(SAT)}$.

The output will start increase when Q_O goes from saturation mode to forward active mode. Only Q_{S2} being in forward active mode is not enough to decrease the voltage at the base of Q_S below 1.6 V and change the state of Q_O. So, Q_{SD} needs to go into forward active mode as well. Thus, the value of the input to make the output rise is equal to $V_{IL} = V_{BE,SD(FA)} + V_{BE,S2(FA)} - V_{CE,I(SAT)}$.

Q_S will turn off when the voltage at its base goes below 0.7 V and this will occur suddenly when Q_{SD} and Q_{S2} go into saturation. Thus, the value of the input which makes the output high is given by $V_{IH} = V_{BE,SD(SAT)} + V_{BE,S2(SAT)} - V_{CE,I(SAT)}$. Then, Q_I goes into reverse active mode and the output stays high.

The states of active elements in a standard TTL noninverter are given in Table 2.14 below.

Table 2.14: State of active elements for output-high and output-low states in a standard TTL inverter.

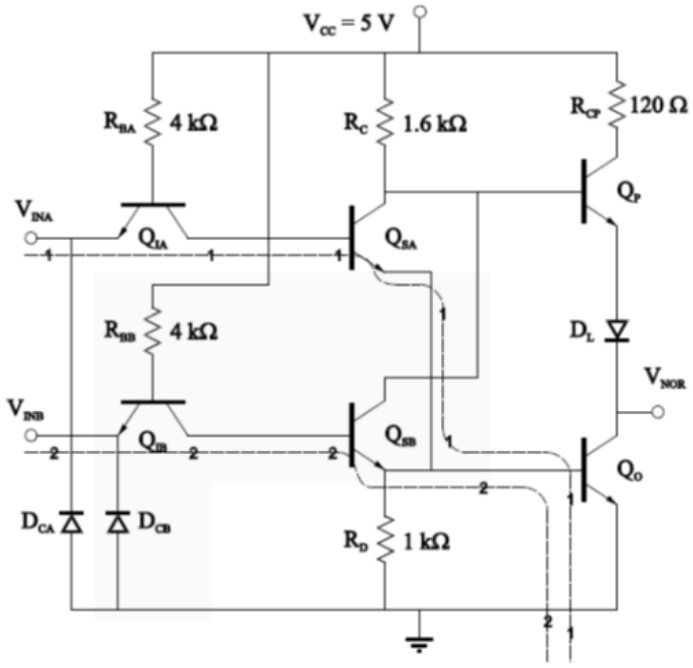
Element	V_{OL}	V_{OH}
Q_O	Saturated (SAT)	Cutoff (OFF)
Q_S	Saturated (SAT)	Cutoff (OFF)
Q_P	Cutoff (OFF)	Edge of conduction (EOC)
D_L	Cutoff (OFF)	Edge of conduction (EOC)
Q_{SD}	Cutoff (OFF)	Saturated (SAT)
Q_{S2}	Cutoff (OFF)	Saturated (SAT)
D_S	Conducting (ON)	Conducting (ON)
Q_I	Saturated (SAT)	Reverse active (RA)

A *knee* is not present in the VTC of the TTL AND gate in contrast to the VTC of the TTL NAND gate, and the transition region is more abrupt. Thus,

$$V_{OL} = V_{CE,O(SAT)} \tag{2.7.1}$$
$$V_{OH} = V_{CC} - V_{BE,P(FA)} - V_{D,L(ON)} \tag{2.7.2}$$
$$V_{IL} = V_{BE,SD(FA)} + V_{BE,S2(FA)} - V_{CE,I(SAT)} \tag{2.7.3}$$
$$V_{IH} = V_{BE,SD(SAT)} + V_{BE,S2(SAT)} - V_{CE,I(SAT)} \tag{2.7.4}$$

2.7.2 NOR Gate

NOR function is obtained by using separate input sections Q_I, R_B and Q_S for the inputs where drive splitter transistors are connected in parallel (i.e., their collectors and emitters are connected together) as shown in Figure 2.7.5(a) below. Circuit symbol for the NOR gate is also displayed in Figure 2.7.5(b) below.



(a)

(b)

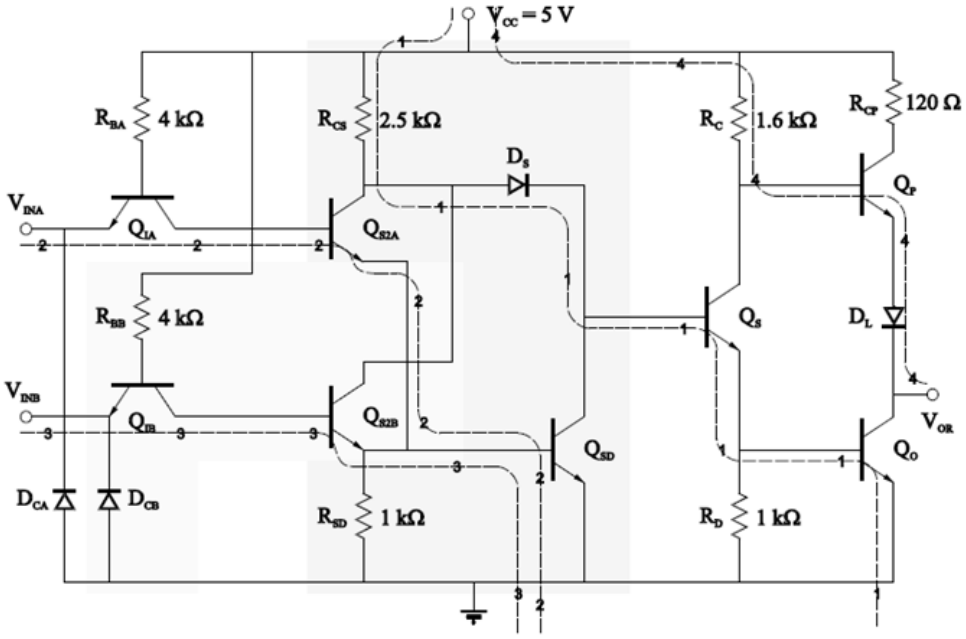
Figure 2.7.5: Standard 5402/7402 TTL NOR gate: (a) Circuit schematic, (b) Circuit symbol.

Example 2.19: For the two input TTL NOR gate in Figure 2.7.5(a), determine the average power dissipation and compare the result with that of a standard TTL inverter calculated in Example 2.17.

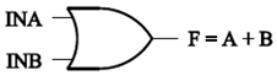
NOTE: You need to consider all four possible input states.

2.7.3 OR Gate

OR function is obtained by using separate input sections and parallel drive splitter transistors of the second lvel inversion circuitry as shown in Figure 2.7.6(a) below. Circuit symbol for the OR gate is also displayed in Figure 2.7.6(b) below.



(a)



(b)

Figure 2.7.6: Standard 5432/7432 TTL OR gate: (a) Circuit schematic, (b) Circuit symbol.

2.7.4 AND-OR-INVERT (AOI) Gates

TTL gates performing more complex logic functions can be designed using the following rules

1. ANDing of signals
   - Multi-emitter input BJT sections
2. ORing of signals
   - Multiple input sections (Q_I and R_B)
   - Multiple and parallel connected drive splitting BJTs (Q_S)
3. If non-inverting ORing is desired
   - Additional logic inversion circuitry with parallel connected drive splitting BJTs
4. Totem-pole output branch

Example 2.20: Design a four-input AOI TTL gate which performs $V_{OUT} = \overline{V_A V_B + V_C V_D}$.

Solution: Circuit schematic and circuit symbol for the solution are shown in Figure 2.7.7 and Figure 2.7.8 below.

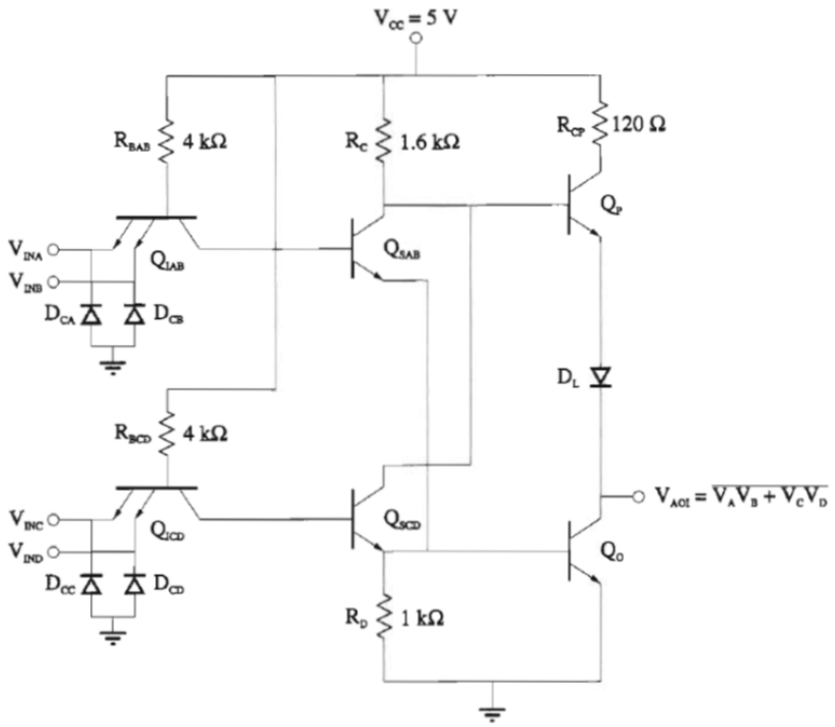


Figure 2.7.7: AOI TTL gate performing $V_{OUT} = \overline{V_A V_B + V_C V_D}$ in Example 2.20.

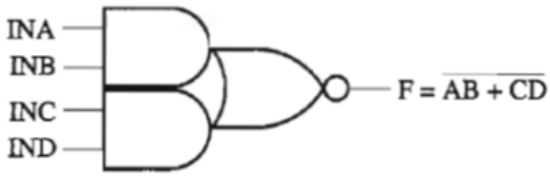


Figure 2.7.8: Circuit symbol for $V_{OUT} = \overline{V_A V_B + V_C V_D}$ in Example 2.20.

Example 2.21: Design a six-input AOI TTL gate which performs $V_{OUT} = V_A V_B + V_C + V_D V_E V_F$.

Solution: Solution is given in Figure 2.7.9 below.

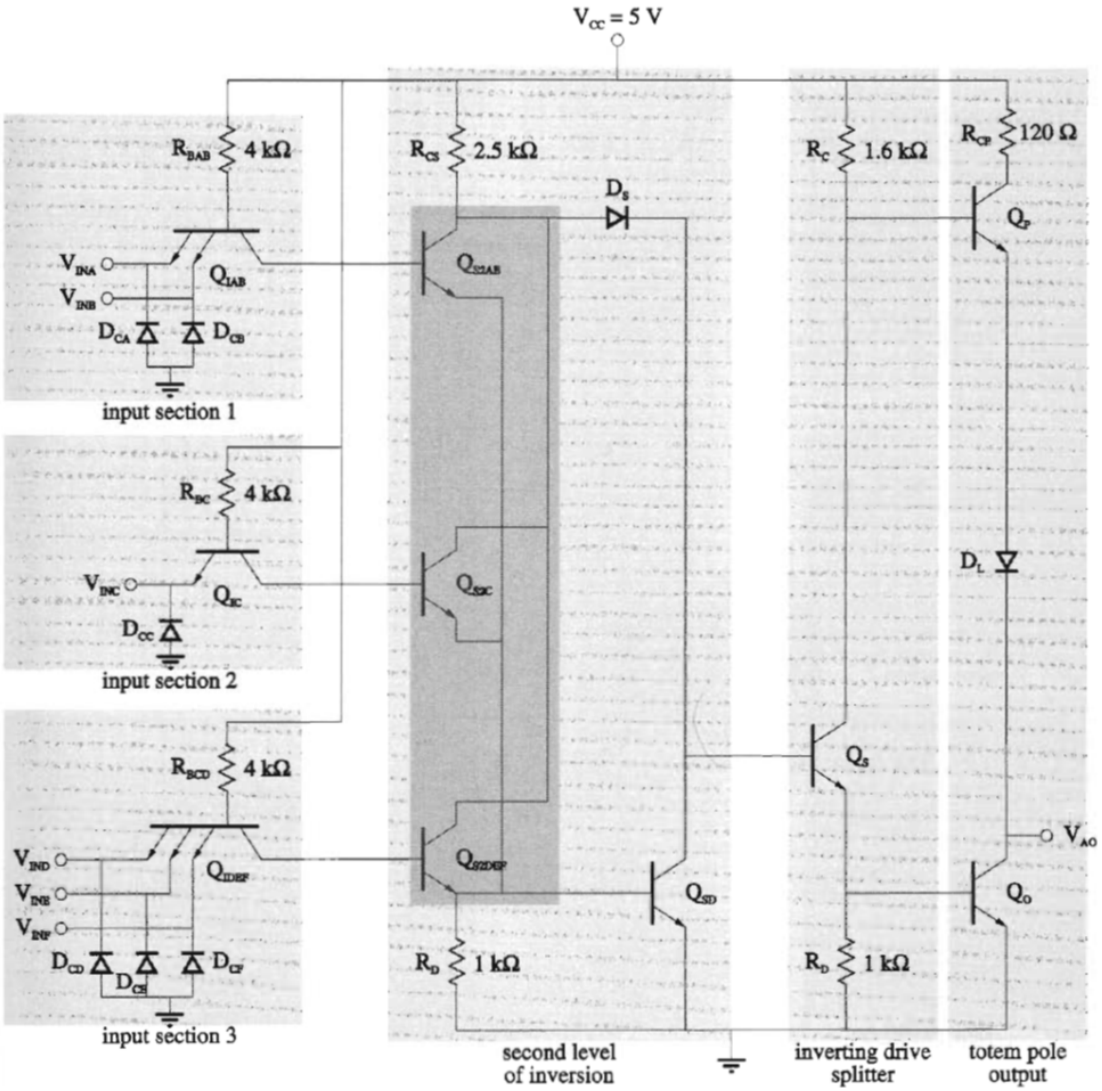


Figure 2.7.9: AOI TTL gate performing $V_{OUT} = V_A V_B + V_C + V_D V_E V_F$ in Example 2.21.

Example 2.22: Design a six-input AOI TTL gate which performs $V_{OUT} = \overline{V_A V_B + V_C + V_D V_E V_F}$.

Solution: Solution is given in Figure 2.7.10 below.

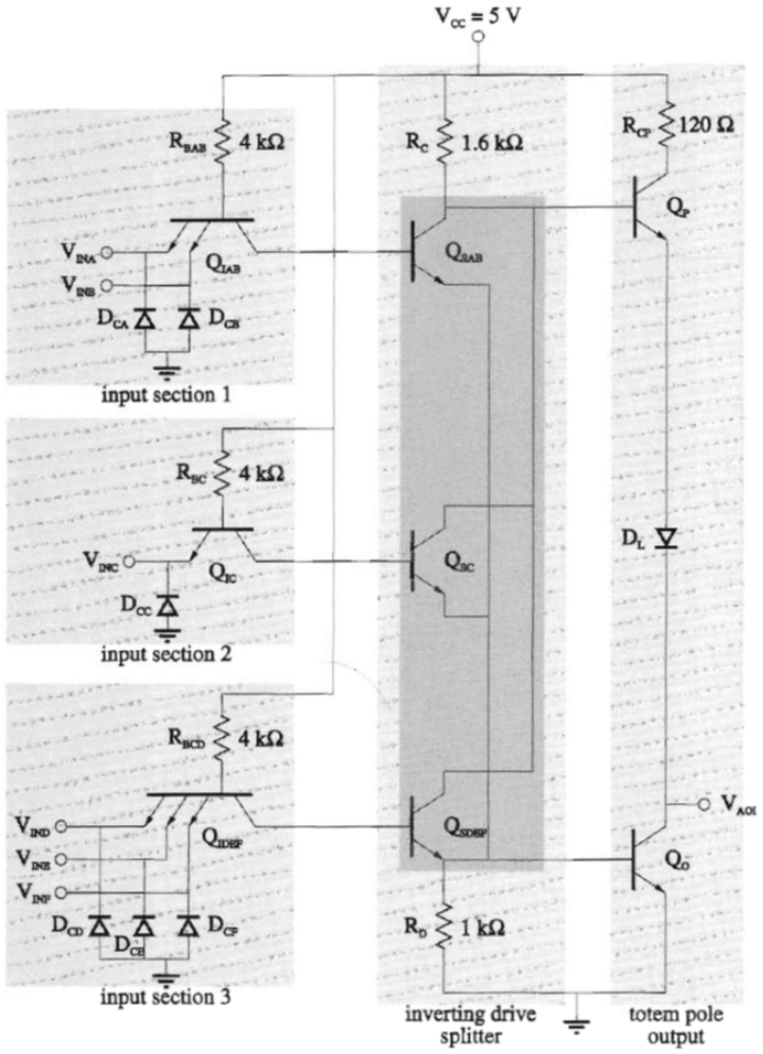


Figure 2.7.10: AOI TTL gate performing $V_{OUT} = \overline{V_A V_B + V_C + V_D V_E V_F}$ in Example 2.22.

2.7.5 XOR Gate

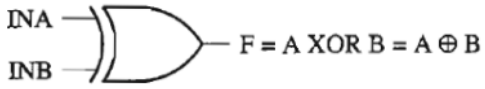


Figure 2.7.11: Circuit symbol for an XOR gate.

Circuit symbol and truth table for an XOR gate are given in Figure 2.7.11 above and Table 2.15 below, respectively.

Table 2.15: Truth table for an XOR gate.

V_{INA}	V_{INB}	V_{OUT}
LOW	LOW	LOW
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

As we notice, the output is LOW when the inputs are the same, and HIGH when the inputs are different.

Also, the outputs will be the same, even when the inputs are inverted, i.e,

$$F = A \oplus B = \overline{A} \oplus \overline{B} \tag{2.7.5}$$

We can form an **XORing logic pair** using two transistors: by connecting one input to the base of the first transistor and to the emitter of the second transistor, and connecting the other input to the base of the second transistor and to the emitter of the first transistor where the collectors of the transistors are connected together, as shown in Figure 2.7.12 as Q_{X1} and Q_{X2}

So, both transistors will be OFF when the inputs are the same. First transistor will be in saturation if the first input is HIGH and the second input is LOW, and similarly second transistor will be in saturation if the first input is LOW and the second input is HIGH. This is actually the XNOR operation, so we need to add an inverter section to the common collector of the transistors in order to obtain the XOR operation.

Also, in order to make sure the transistors will be in saturation when the inputs are different, we invert the inputs first to obtain fixed voltage levels for the inputs of the XORing logic pair which consists of Q_{X1} and Q_{X2}.

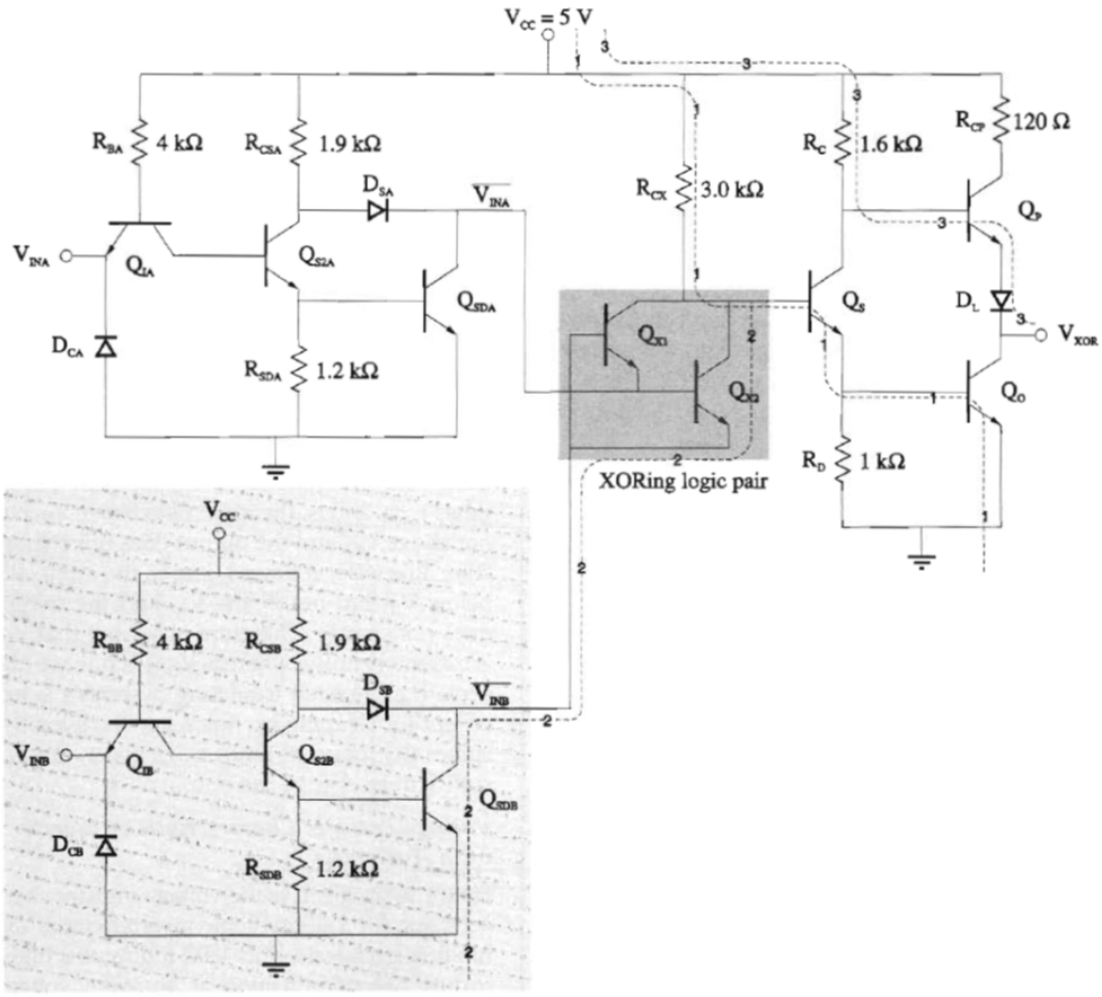


Figure 2.7.12: Standard 5486/7486 TTL XOR gate.

2.7.6 Schmitt Trigger Inverters and NAND Gates

Consider a noisy signal, shown at the top of Figure 2.7.13(a) below, as an input to an inverter gate. We need to produce a neat inverter output signal considering the input is LOW before t_2, HIGH between t_2 and t_3, LOW between t_5 and t_8 and HIGH after t_8, as shown at the bottom of Figure 2.7.13(a) below.

As we can see, a single threshold is not enough to determine the input voltage state. Two thresholds are needed one for low-to-high transition and another one for high-to-low transition.

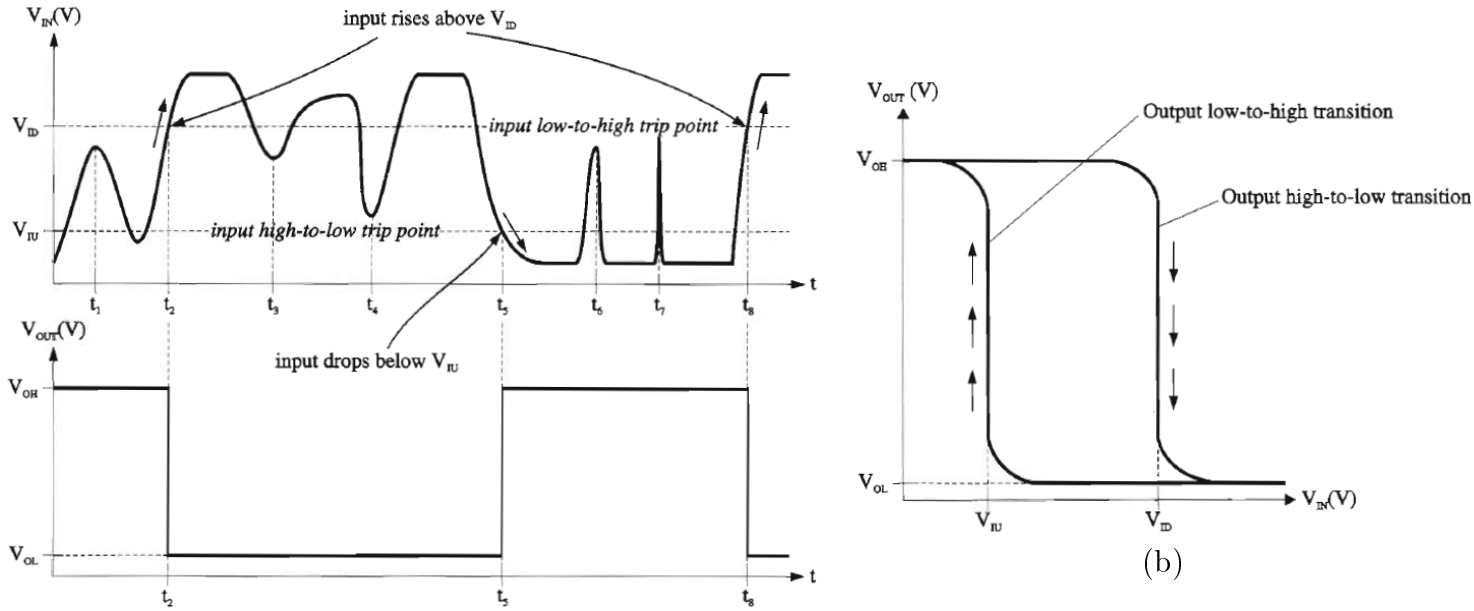


Figure 2.7.13: Schmitt trigger inverter: (a) Noisy input and the corresponding inverting output voltage waveforms, (b) VTC characteristics exhibiting hysteresis having different threshold levels V_{ID} and V_{IU} for high-to-low and low-to-high transitions, respectively.

As seen from Figure 2.7.13(b) above, VTC exhibits **hysteresis**, i.e., low-to-high path is not the same as the high-to-low path of the input-output relationship.

2.7.6.1 Basic Emitter-Coupled Schmitt Trigger Noninverter

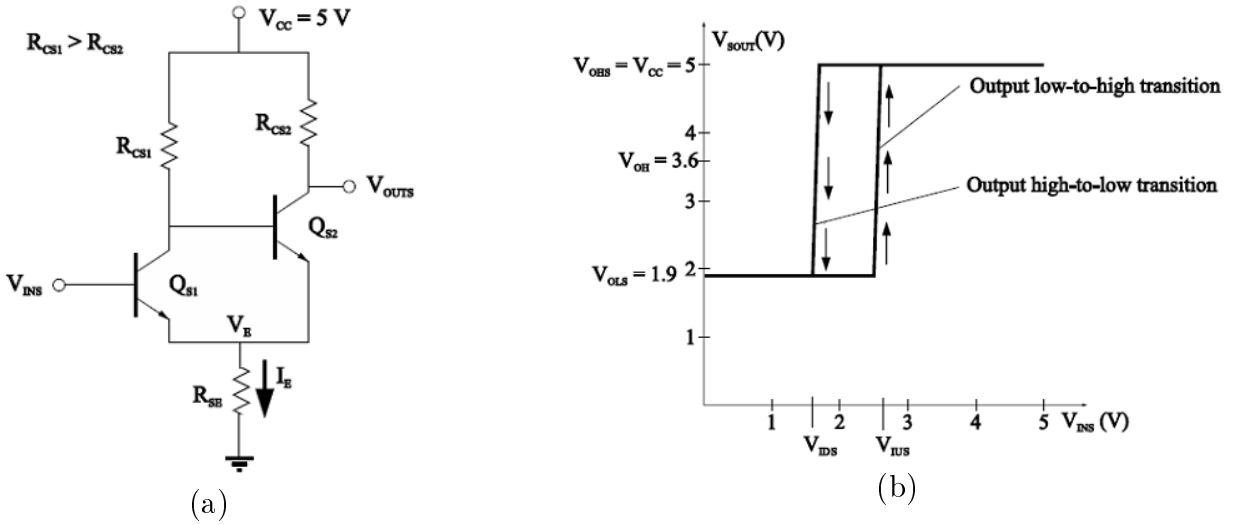


Figure 2.7.14: Basic emitter-coupled noninverting Schmitt Trigger: (a) Circuit, (b) VTC.

Hysteresis can be achieved by the basic emitter-coupled noninverting Schmitt Trigger circuit shown in Figure 2.7.14(a) above.

Let us first investigate, low-to-high path of the input. When input is LOW, e.g., $V_{INS} = 0\,\text{V}$, then Q_{S1} is cutoff and Q_{S2} is in saturation. Thus, the output is LOW, i.e., $V_{OUTS} = V_{OLS} = V_E + V_{CE,S2(SAT)}$. So, $I_{E,S2} = I_{B,S2} + I_{C,S2}$, i.e.,

$$\frac{V_E}{R_{SE}} = \frac{V_{CC} - V_E - V_{BE,S2(SAT)}}{R_{CS1}} + \frac{V_{CC} - V_E - V_{CE,S2(SAT)}}{R_{CS2}} \tag{2.7.6}$$

We find V_E as

$$V_E = \left(\frac{V_{CC} - V_{BE,S2(SAT)}}{R_{CS1}} + \frac{V_{CC} - V_{CE,S2(SAT)}}{R_{CS2}} \right) R_{eq} \tag{2.7.7}$$

where $R_{eq} = R_{CS1}||R_{CS2}||R_{SE}$.

Thus, V_{OLS} is given by

$$V_{OLS} = \left(\frac{V_{CC} - V_{BE,S2(SAT)}}{R_{CS1}} + \frac{V_{CC} - V_{CE,S2(SAT)}}{R_{CS2}} \right) R_{eq} + V_{CE,S2(SAT)} \tag{2.7.8}$$

As, we keep increasing the input, eventually Q_{S1} will become forward active at an input voltage $V_{INS} = V_{IUS} = V_E + V_{BE,S1(FA)}$. Then, V_E will increase and V_{OUTS} will start to rise.

Thus, V_{IUS} is given by

$$V_{IUS} = \left(\frac{V_{CC} - V_{BE,S2(SAT)}}{R_{CS1}} + \frac{V_{CC} - V_{CE,S2(SAT)}}{R_{CS2}} \right) R_{eq} + V_{BE,S1(FA)} \tag{2.7.9}$$

Once the input is further increased, voltage at Q_{S1} will go into saturation and Q_{S2} will turn off. Then, the output voltage will become HIGH at $V_{OUTS} = V_{OHS} = V_{CC} - I_{RCS2}R_{CS2}$. But, as there is no load $I_{RCS2} = 0$ and

$$V_{OHS} = V_{CC} \tag{2.7.10}$$

[]Now we can investigate the high-to-low path of the input. In this case Q_{S2} is cutoff and Q_{S1} is in saturation. The output will fall when Q_{S2} becomes forward active, i.e., when $V_{BE,S2} = V_{BE(FA)}$.

As $V_E = V_{INS} - V_{BE,S1(SAT)}$, $V_{BE,S2} = V_{B,S2} - V_E$, $V_{B,S2} = V_{CC} - I_{C,S1}R_{CS1}$ and $I_{C,S1} \approx I_{E,S1} = V_E/R_{SE}$, we can obtain the input in terms of $V_{BE,S2}$ as

$$V_{INS} = \frac{V_{CC} - V_{BE,S2}}{R_{CS1}/R_{SE} + 1} + V_{BE,S1(SAT)} \tag{2.7.11}$$

As the output will start to drop when Q_{S2} turns on, i.e., when $V_{BE,S2} = V_{BE(FA)}$, then we can find V_{IDS} as

$$V_{IDS} = \frac{V_{CC} - V_{BE,S2(FA)}}{R_{CS1}/R_{SE} + 1} + V_{BE,S1(SAT)} \tag{2.7.12}$$

Example 2.23: For the Schmitt Trigger noninverter circuit in Figure 2.7.14(a), determine the V_{OHS}, V_{OLS}, V_{IUS} and V_{IDS} values where $R_{CS1} = 4\,\text{k}\Omega$, $R_{CS2} = 2.5\,\text{k}\Omega$, and $R_{SE} = 1\,\text{k}\Omega$.

Solution: As $R_{eq} = R_{CS1}||R_{CS2}||R_{SE} = 606\,\Omega$,

$$V_{OHS} = 5\,\text{V} \tag{2.7.13}$$

$$V_{E,S2(SAT)} = \left(\frac{V_{CC} - V_{BE,S2(SAT)}}{R_{CS1}} + \frac{V_{CC} - V_{CE,S2(SAT)}}{R_{CS2}}\right) R_{eq} = 1.8\,\text{V} \tag{2.7.14}$$

$$V_{OLS} = V_{E,S2(SAT)} + V_{CE,S2(SAT)} = 2\,\text{V} \tag{2.7.15}$$

$$V_{IUS} = V_{E,S2(SAT)} + V_{BE,S1(FA)} = 2.5\,\text{V} \tag{2.7.16}$$

$$V_{IDS} = \frac{V_{CC} - V_{BE,S2(FA)}}{R_{CS1}/R_{SE} + 1} + V_{BE,S1(SAT)} = 1.66\,\text{V} \tag{2.7.17}$$

2.7.6.2 Schmitt Trigger NAND Gate

We can convert the basic emitter-coupled Schmitt Trigger noninverter in Figure 2.7.14(a) to a TTL compatible Schmitt Trigger NAND gate by connecting and ANDing diode section at the input and by adding a emitter-follower level shifter section with Q_L and D_L followed by a normal inverting driver splitter connected a totem-pole output section at the output, as shown in Figure 2.7.15 below.

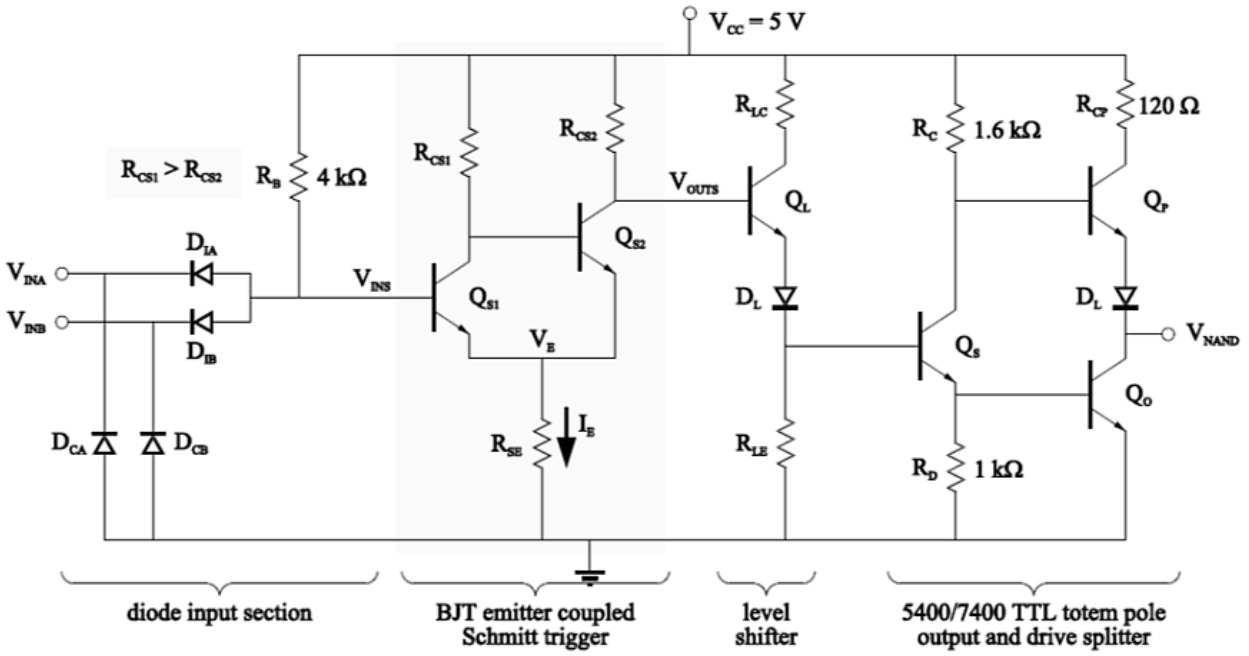


Figure 2.7.15: Standard 5424/7424 Schmitt Trigger NAND gate.

Circuit symbol for a Schmitt Trigger NAND gate is shown in Figure 2.7.16 below.

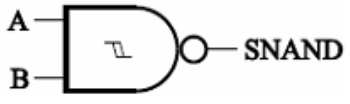


Figure 2.7.16: Circuit symbol for a Schmitt Trigger NAND gate.

An example VTC for a standard Schmitt Trigger NAND gate is shown in Figure 2.7.17 below.

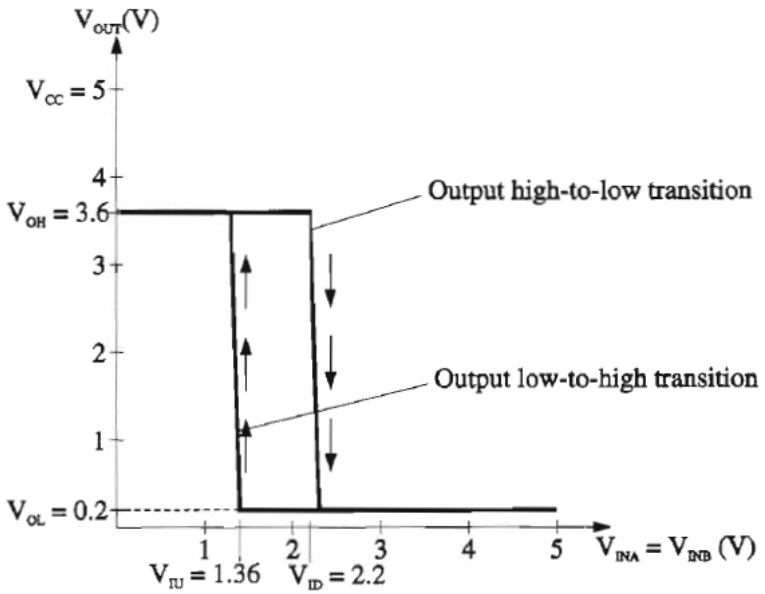


Figure 2.7.17: An example VTC for a standard Schmitt Trigger NAND gate.

Example 2.24: For the Schmitt Trigger NAND circuit in Figure 2.7.15, determine the V_{OH}, V_{OL}, V_{IU} and V_{ID} values where $R_{CS1} = 4\,\text{k}\Omega$, $R_{CS2} = 2.5\,\text{k}\Omega$, and $R_{SE} = 1\,\text{k}\Omega$.

HINT: Use the results in Example 2.23.

Solution:

$$V_{OH} = V_{CC} - V_{BE,P(FA)} - V_{D,L(ON)} = 3.6\,\text{V} \tag{2.7.18}$$

$$V_{OL} = V_{CE,O(SAT)} = 0.2\,\text{V} \tag{2.7.19}$$

$$V_{ID} = V_{IUS} - V_{D,I(ON)} = 1.8\,\text{V} \tag{2.7.20}$$

$$V_{IU} = V_{IDS} - V_{D,I(ON)} = 0.96\,\text{V} \tag{2.7.21}$$

2.7.7 Tri-State Buffers

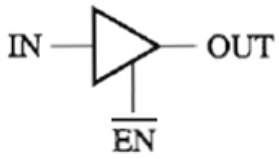


Figure 2.7.18: Circuit symbol for a low-enabled tri-state buffer (or noninverter).

Circuit symbol and truth table for a low-enabled tri-state buffer (or noninverter) are given in Figure 2.7.18 above and Table 2.16 below, respectively.

Table 2.16: Truth table for a low-enabled tri-state buffer.

V_{IN}	$\overline{V_{EN}}$	V_{OUT}
LOW	LOW	LOW
HIGH	LOW	HIGH
LOW	HIGH	HIGH IMPEDANCE (Z)
HIGH	HIGH	HIGH IMPEDANCE (Z)

High impedance Z-state nodes are floating, i.e., **not connected**. So, high impedance Z-state nodes are **not** at ground, **not** at V_{CC} and have **no** driving ability.

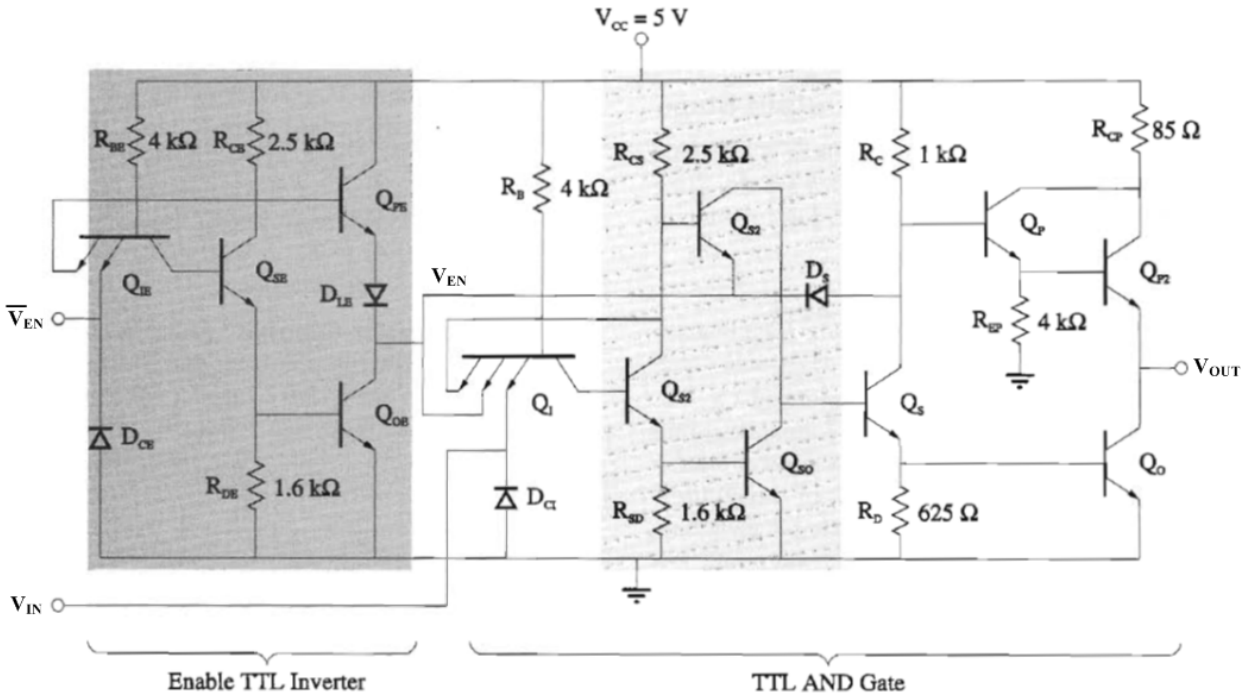


Figure 2.7.19: Circuit schematic for a low-enabled tri-state buffer (or noninverter).

Enable-disable functionality is basically achieved by connecting a diode D_S to the enable input of Q_I which is also ANDed together with the actual input.

- When V_{EN} is HIGH, D_S is OFF. So, the circuit operates like a normal noninverter and output is determined by the input V_{IN}.
- When V_{EN} is LOW, Q_S and Q_O are OFF due to AND operation, and D_S is also ON. As D_S is ON, voltage at the base of Q_P drops to $V_{EN} + V_{D,S(ON)}$ which is not high enough to turn on Q_{P2}. So, both Q_O are Q_{P2} are OFF, and output V_{OUT} is not connected to pull-up or pull-down drivers regardless of the value of the input V_{IN}. In other words, when V_{EN} is LOW, the circuit is disabled and the output is in high impedance state.

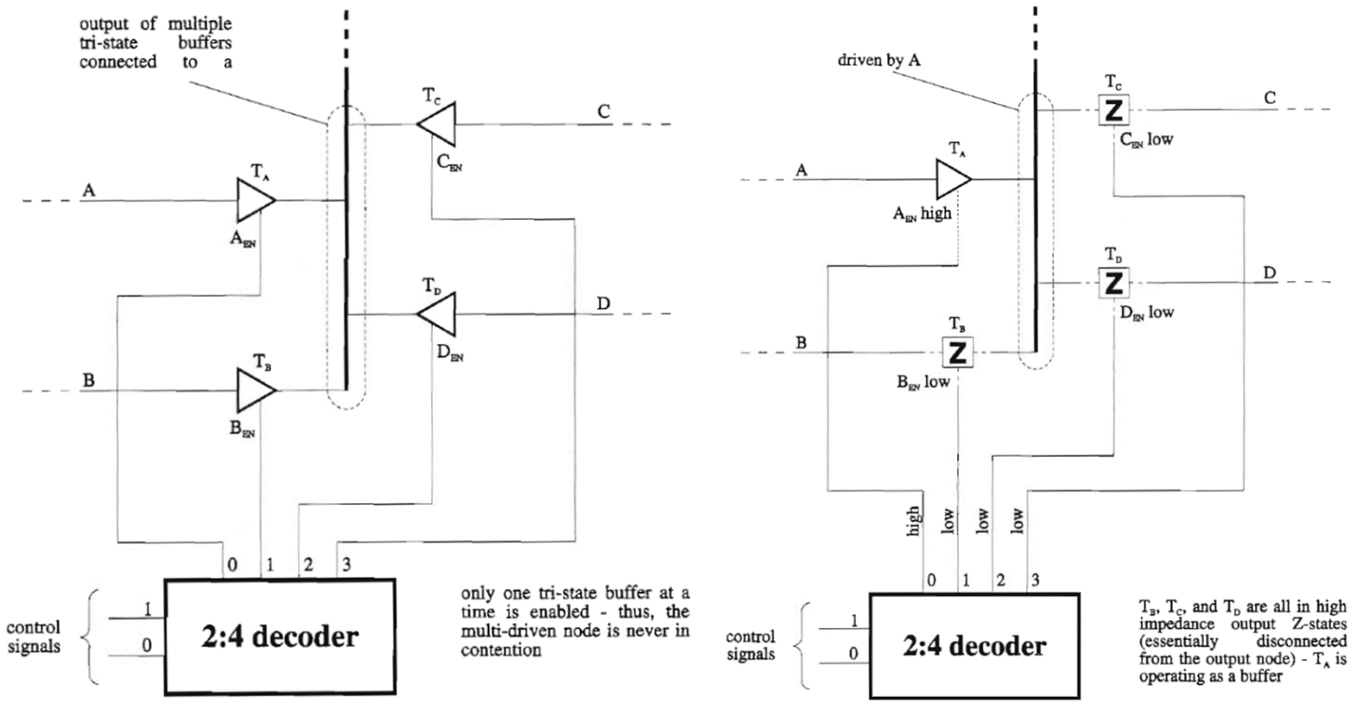


Figure 2.7.20: Example usage of high-enabled tri-state buffers: (a) Four-buffers connected to a single bus, (b)Case of T_A is enabled, T_B, T_C and T_D are disabled.

Figure 2.7.20(a) shows an example of four tri-state buffers connected to a single bus. Figure 2.7.20(b) shows how to enable a single buffer at a time using a 2:4 decoder, e.g., acting as a 4-to-1 multiplexer with two select inputs.

Tri-state buffers are often used to drive multi-bit circuit busses as shown in Figure 2.7.21 below.

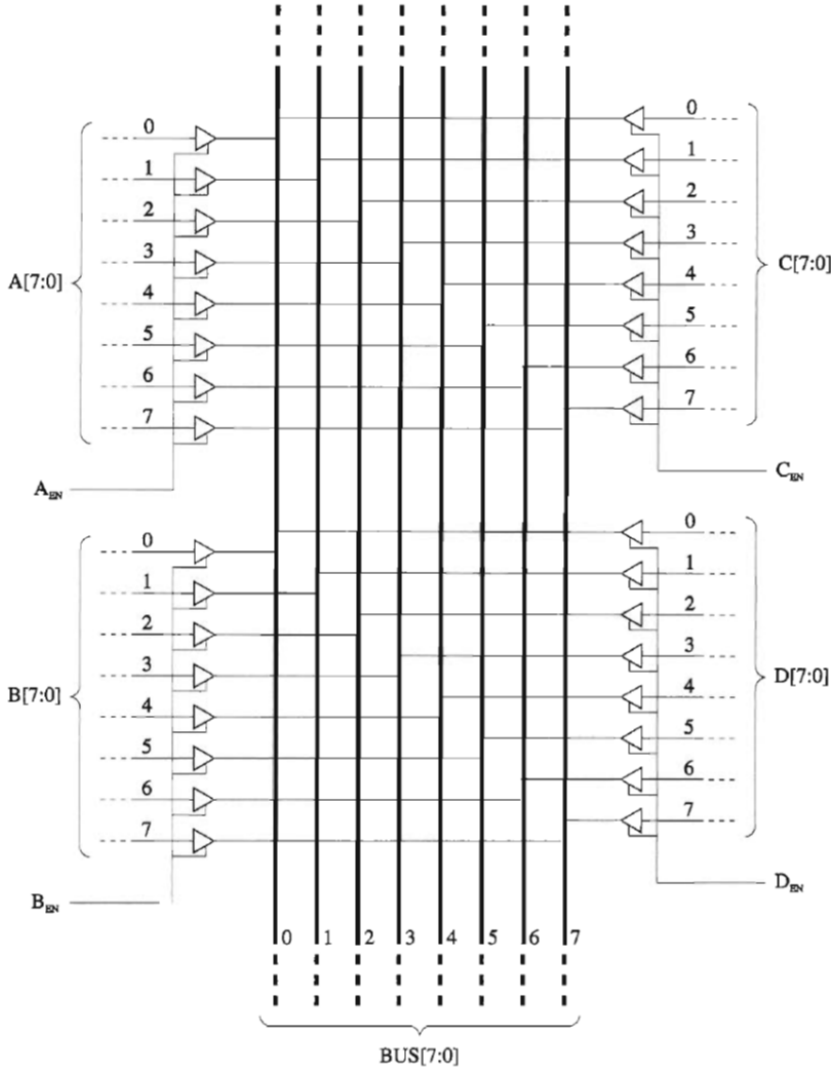


Figure 2.7.21: 8-bit data bus driven by four 8-bit register outputs where one enable signal enables or disable all 8-bit register outputs.

2.8 NMOS and CMOS Gates