eration is achieved by using complementary transistors (Q_1 and Q_2) before the matched *npn* output transistors (Q_3 and Q_4). Notice that transistors Q_1 and Q_3 form a Darlington connection that provides output from a low-impedance emitter-follower. The connection of transistors Q_2 and Q_4 forms a feedback pair, which similarly provides a low-impedance drive to the load. Resistor R_2 can be adjusted to minimize crossover distortion by adjusting the dc bias condition. The single input signal applied to the push-pull stage then results in a full cycle output to the load. The quasi-complementary push-pull amplifier is presently the most popular form of power amplifier.

EXAMPLE 15.10

For the circuit of Fig. 15.19, calculate the input power, output power, and power handled by each output transistor and the circuit efficiency for an input of 12 V rms.

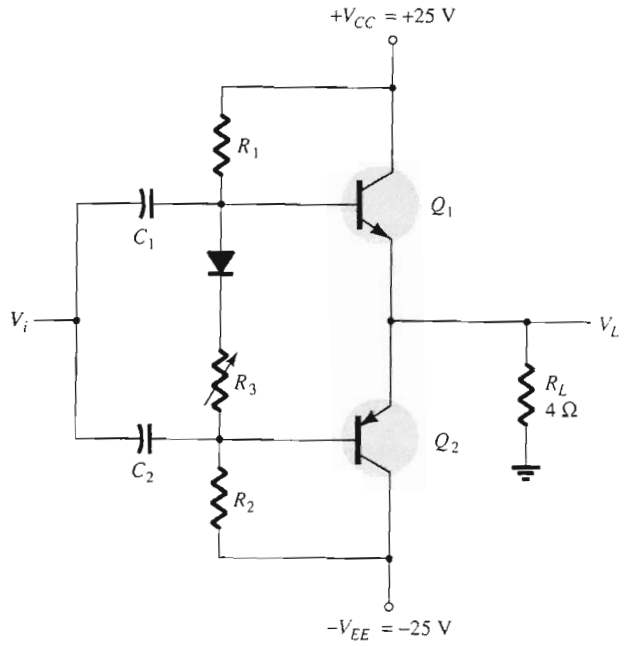

Figure 15.19 Class B power amplifier for Examples 15.10–15.12.

Solution

The peak input voltage is

$$V_i(\text{p}) = \sqrt{2}\, V_i\,(\text{rms}) = \sqrt{2}\,(12\text{ V}) = 16.97\text{ V} \approx 17\text{ V}$$

Since the resulting voltage across the load is ideally the same as the input signal (the amplifier has, ideally, a voltage gain of unity),

$$V_L(\text{p}) = 17\text{ V}$$

and the output power developed across the load is

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(17\text{ V})^2}{2(4\ \Omega)} = \mathbf{36.125\ W}$$

The peak load current is

$$I_L(\text{p}) = \frac{V_L(\text{p})}{R_L} = \frac{17\text{ V}}{4\ \Omega} = 4.25\text{ A}$$

from which the dc current from the supplies is calculated to be

$$I_{\text{dc}} = \frac{2}{\pi} I_L(\text{p}) = \frac{2(4.25\text{ A})}{\pi} = 2.71\text{ A}$$

so that the power supplied to the circuit is

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} = (25\text{ V})(2.71\text{ A}) = \mathbf{67.75\text{ W}}$$

The power dissipated by each output transistor is

$$P_Q = \frac{P_{2Q}}{2} = \frac{P_i - P_o}{2} = \frac{67.75\text{ W} - 36.125\text{ W}}{2} = \mathbf{15.8\text{ W}}$$

The circuit efficiency (for the input of 12 V, rms) is then

$$\%\,\eta = \frac{P_o}{P_i} \times 100\% = \frac{36.125\text{ W}}{67.75\text{ W}} \times 100\% = \mathbf{53.3\%}$$

EXAMPLE 15.11

For the circuit of Fig. 15.19, calculate the maximum input power, maximum output power, input voltage for maximum power operation, and the power dissipated by the output transistors at this voltage.

Solution

The maximum input power is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi R_L} = \frac{2(25\text{ V})^2}{\pi 4\,\Omega} = \mathbf{99.47\text{ W}}$$

The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(25\text{ V})^2}{2(4\,\Omega)} = \mathbf{78.125\text{ W}}$$

[Note that the maximum efficiency is achieved:]

$$\%\,\eta = \frac{P_o}{P_i} \times 100\% = \frac{78.125\text{ W}}{99.47\text{ W}}100\% = 78.54\%$$

To achieve maximum power operation the output voltage must be

$$V_L(\text{p}) = V_{CC} = 25\text{ V}$$

and the power dissipated by the output transistors is then

$$P_{2Q} = P_i - P_o = 99.47\text{ W} - 78.125\text{ W} = \mathbf{21.3\text{ W}}$$

EXAMPLE 15.12

For the circuit of Fig. 15.19, determine the maximum power dissipated by the output transistors and the input voltage at which this occurs.

Solution

The maximum power dissipated by both output transistors is

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L} = \frac{2(25\text{ V})^2}{\pi^2 4\,\Omega} = \mathbf{31.66\text{ W}}$$

This maximum dissipation occurs at

$$V_L = 0.636V_L(\text{p}) = 0.636(25\text{ V}) = \mathbf{15.9\text{ V}}$$

(Notice that at $V_L = 15.9$ V the circuit required the output transistors to dissipate 31.66 W, while at $V_L = 25$ V they only had to dissipate 21.3 W.)
