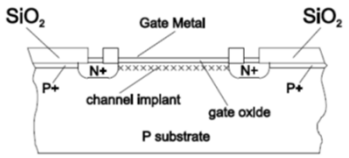
MOS Logic

MOS Logic

- NMOS gates
  - Fabrication
  - Modes of operation
- NMOS Inverters and Analysis
  - General NMOS Inverter
  - Resistor Loaded NMOS Inverter
  - E-MOSFET loaded NMOS Inverter
  - D-MOSFET loaded NMOS Inverter

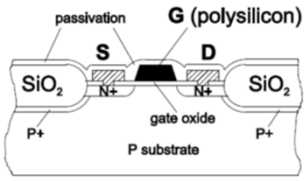
NMOS (n-channel E-MOSFET) Fabrication Examples

METAL GATE NMOS



Cross-section

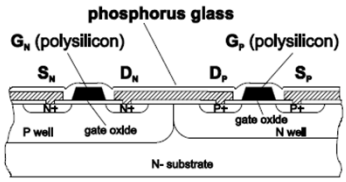
SILICON GATE NMOS



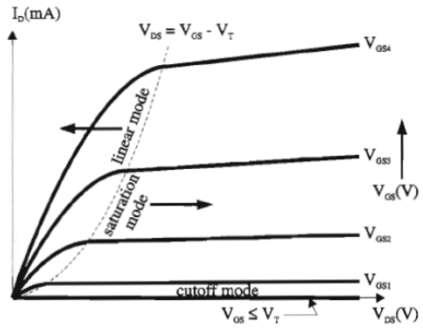
Cross-section

CMOS Fabrication Example

Twin-Tub CMOS



IV Characteristics



SATURATION

$$I_D(SAT) = \frac{k}{2}(V_{GS} - V_T)^2$$

LINEAR

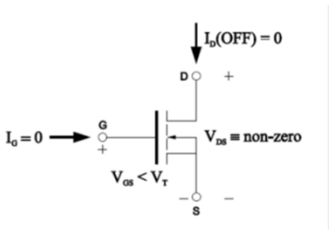
$$I_D(LIN) = k\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Device transconductance parameter ≡

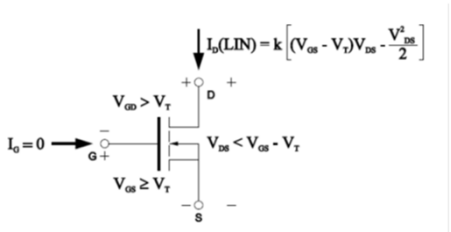
$$k = k'\left(\frac{W}{L}\right)$$

k': *Process transconductance parameter*

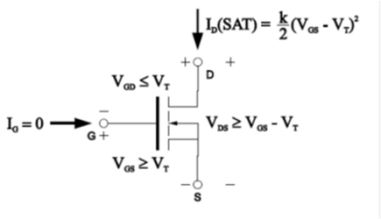
NMOS modes of operation



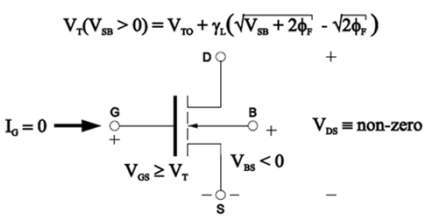
(a) Cutoff mode



(b) Linear mode

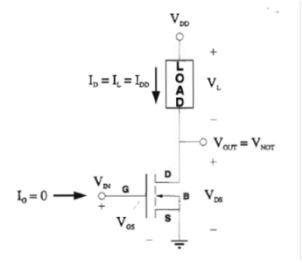


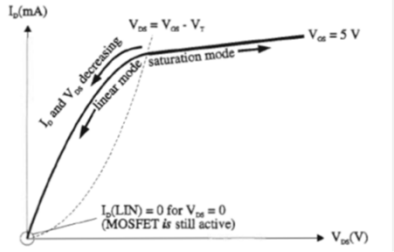
(c) Saturation mode

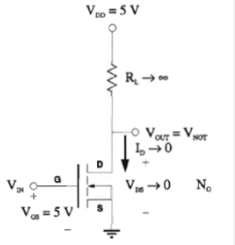


(d) body-bias effect on threshold voltage

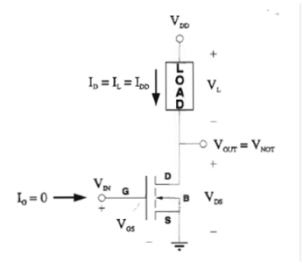
General NMOS Inverter

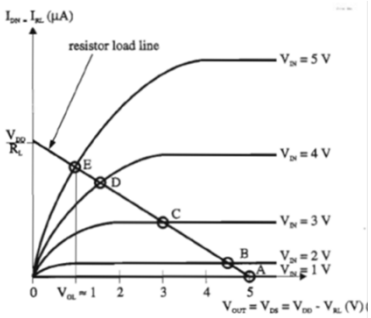


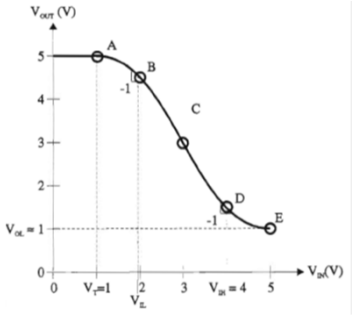




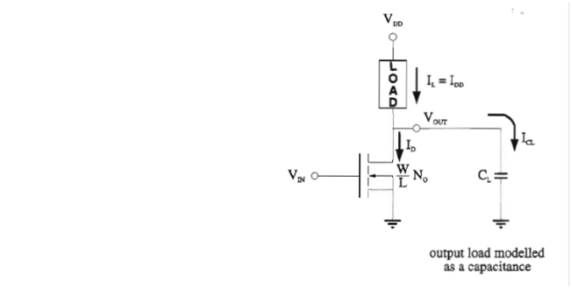
Graphical analysis when load is a resistor

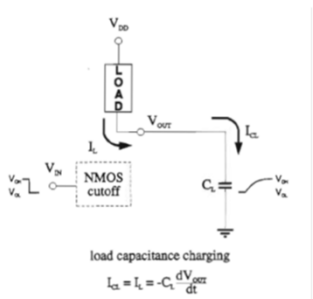


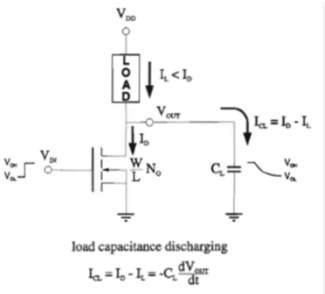




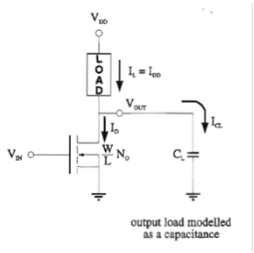
Load capacitance







Power dissipation



(a) Static power dissipation

$$P_{DD} = V_{DD} (I_{DD(OH)} + I_{DD(OL)}) / 2$$
$$\cong V_{DD} I_{DD(OL)} / 2$$

$$P_{TOTAL} = P_{DD} + P_D$$

(b) Transient power dissipation

$$P_D = C_L \, f \, V^2_{DD}$$

f: frequency at which the gate is switched

Resistor Loaded NMOS

Resistor Loaded NMOS Inverter

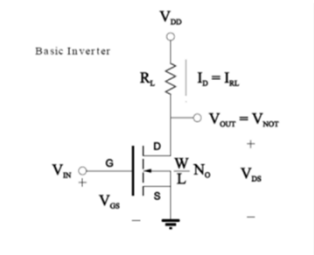
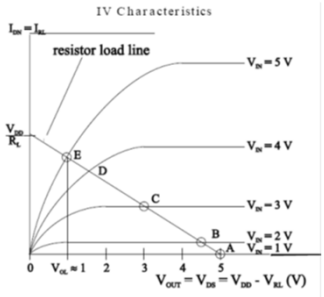
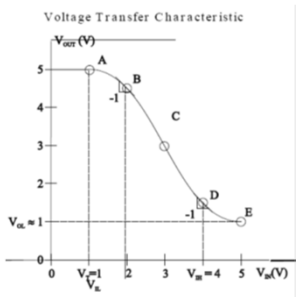


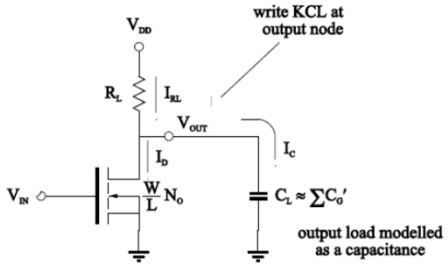
TABLE 18.1 States of N_O for the Resistor Loaded NMOS Inverter

Critical Point	State of N_O
V_{OH}	Cutoff
V_{IL}	Saturation
V_{IH}	Linear
V_{OL}	Linear
V_M	Saturation

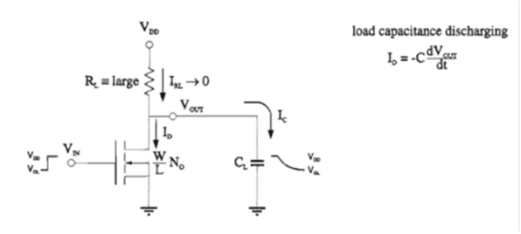


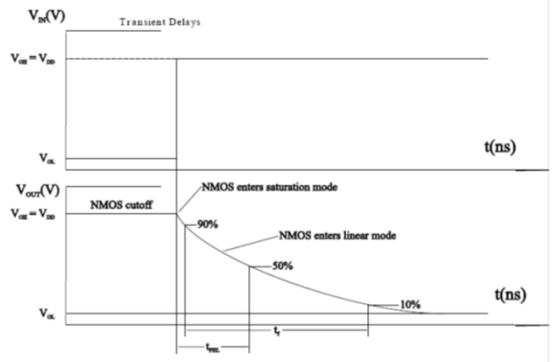


Propagation Delay



Fall time





E-MOSFET Loaded NMOS

E-MOSFET Loaded NMOS Inverter

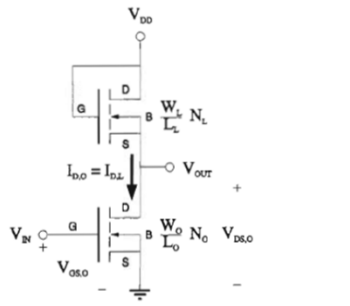
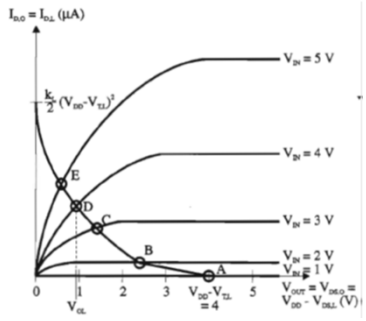
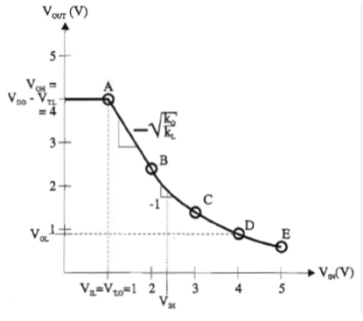


TABLE 19.1 States of Transistors for Saturated Enhancement-Only Loaded NMOS Inverter

Critical Point	Output N_O	Load N_L
V_{OH}	Cutoff	Saturation
V_{IL}	EOC	Saturation
V_M	Saturation	Saturation
V_{IH}	Linear	Saturation
V_{OL}	Linear	Saturation





D-MOSFET Loaded NMOS

D-MOSFET Loaded NMOS Inverter

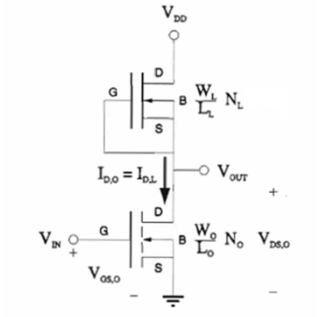
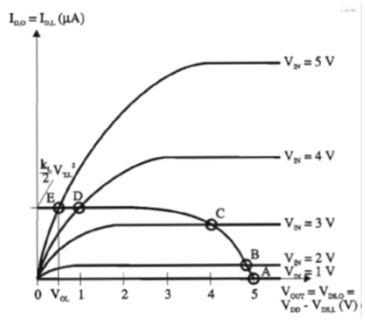
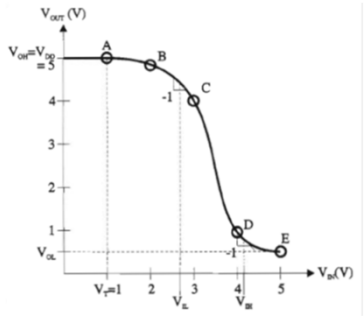


TABLE 21.1 States of Transistors for Enhancement-Depletion Loaded NMOS Inverter

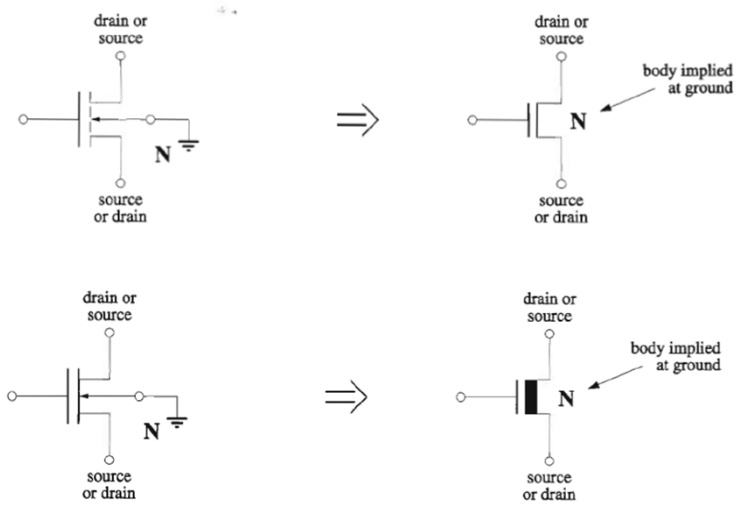
Critical Point	Output N_O	Load N_L
V_{OH}	Cutoff	Linear
V_{IL}	Saturation	Linear
V_M	Saturation	Saturation
V_{IH}	Linear	Saturation
V_{OL}	Linear	Saturation



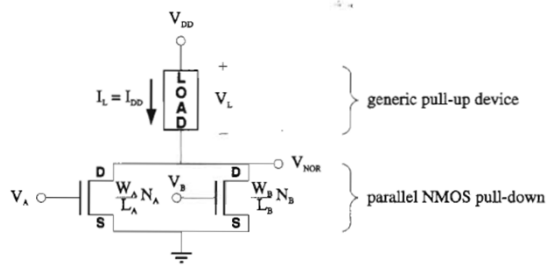


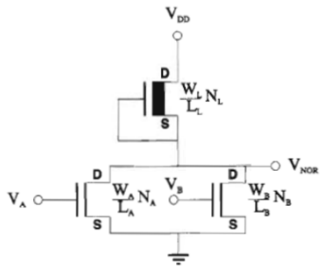
NMOS Gates

Symbol Shorthands



NOR Gate



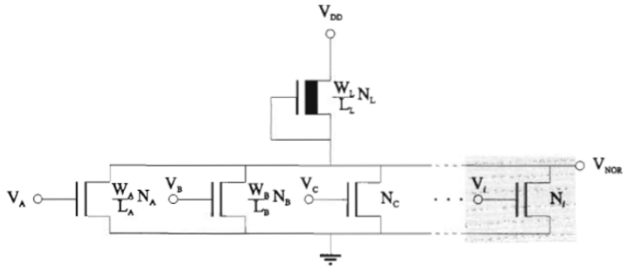


$$V_{OL}(R\ loaded) \approx \frac{V_{DD}}{k_O R_L (V_{DD} - V_{T,O}) + 1}$$

$$V_{OL}(E\text{-}D\ loaded) = \frac{k_L V_{T,L}^2}{2k_O (V_{DD} - V_{T,O})}$$

$$k_O = k' \left(\frac{W_A}{L_A} + \frac{W_B}{L_B} \right)$$

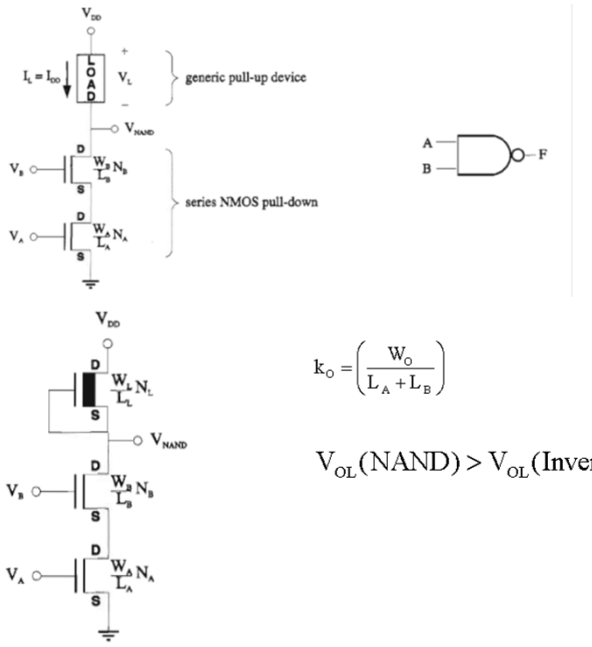
NOR Gates



$$V_{OL}(E\text{-}D\ loaded) = \frac{k_L V_{T,L}^2}{2k_O (V_{DD} - V_{T,O})}$$

$$V_{OL}(two\ NOR\ inputs\ high) < V_{OL}(inverter)$$

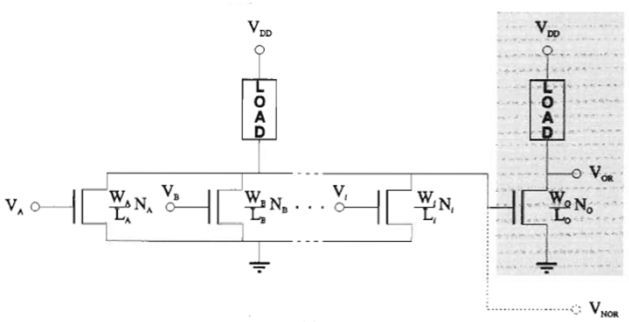
NAND Gate

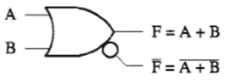


$$k_O = \left(\frac{W_O}{L_A + L_B}\right)$$

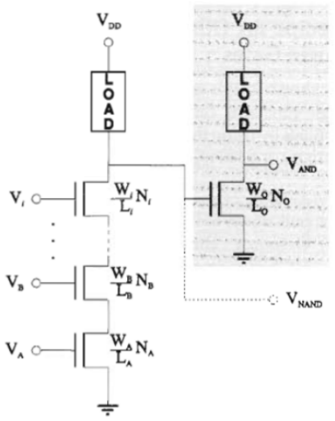
$$V_{OL}(\text{NAND}) > V_{OL}(\text{Inverter})$$

OR Gates

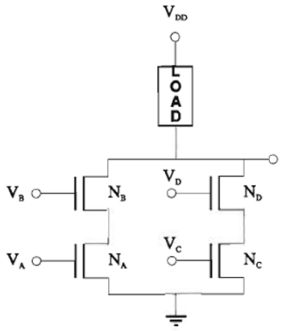




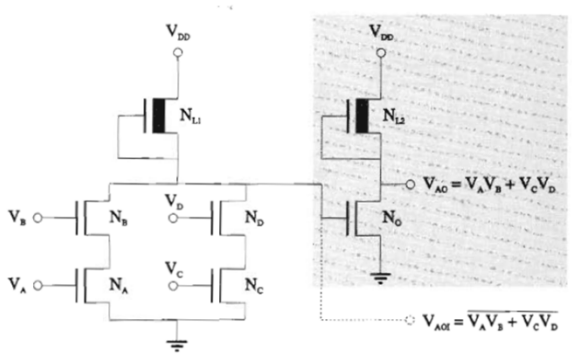
AND Gates



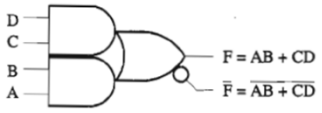
Example



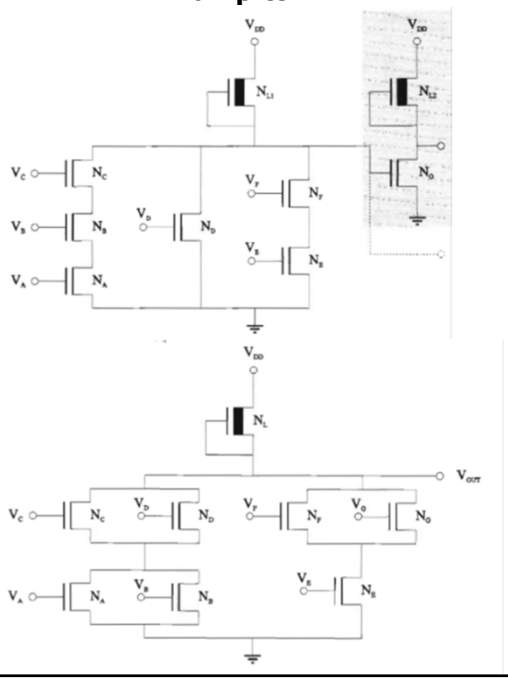
AOI (AND-OR-INVERT) Gates



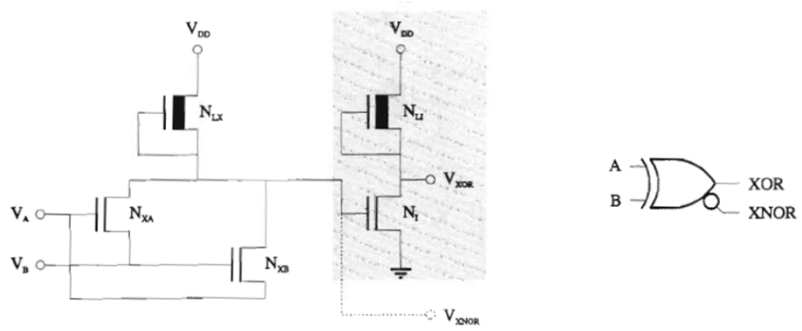
(a)



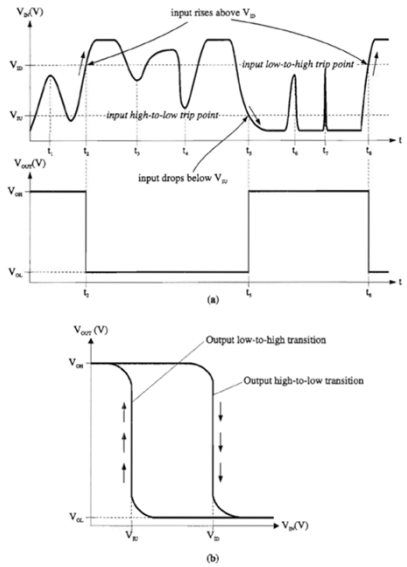
Examples



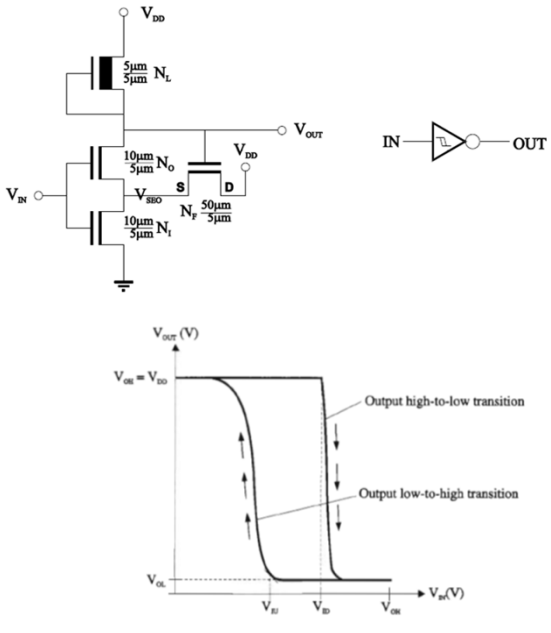
XOR/XNOR Gates



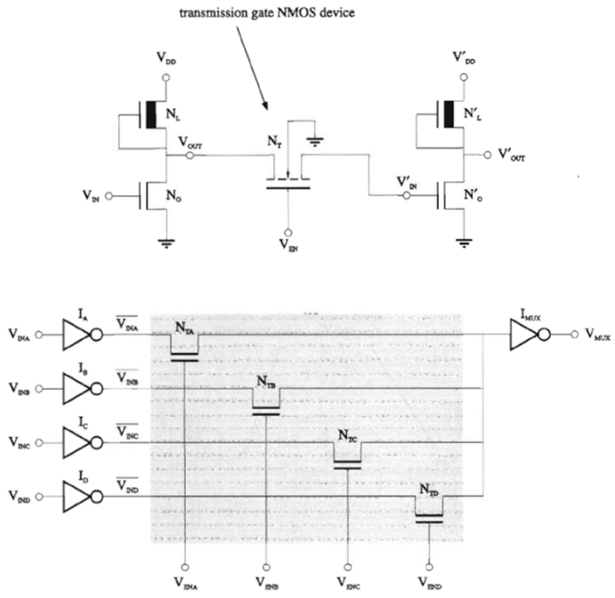
Hysteresis



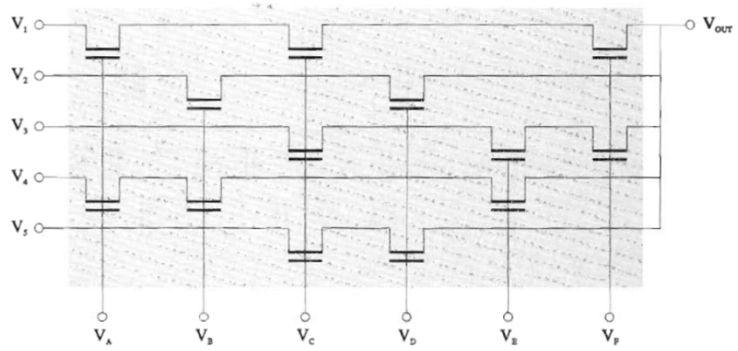
Schmitt Trigger



Transmission Gate

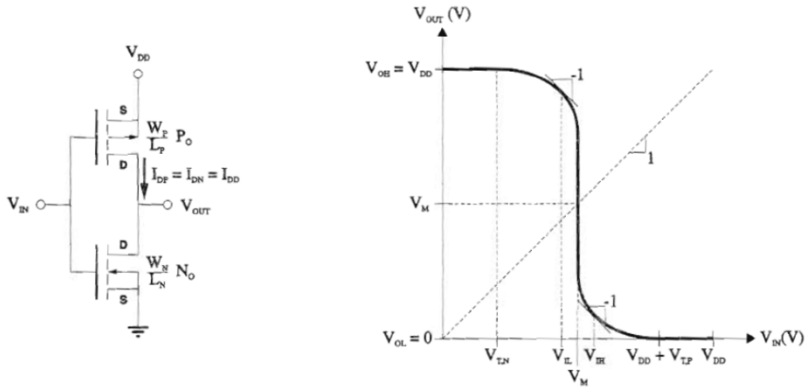


Transmission Gate Array



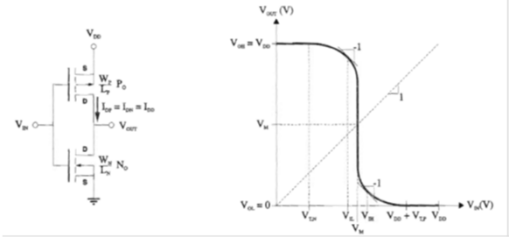
CMOS Logic

CMOS Inverter

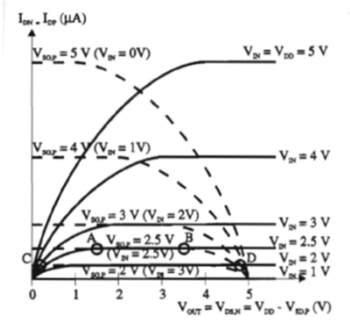


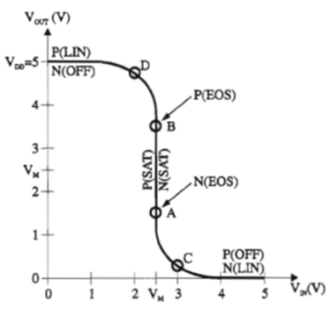
Critical Point	NMOS N_O	PMOS P_O
V_{OH}	Cutoff	Linear
V_{IL}	Saturation	Linear
V_M	Saturation	Saturation
V_{IH}	Linear	Saturation
V_{OL}	Linear	Cutoff

CMOS Inverter



Critical Point	NMOS N_O	PMOS P_O
V_{OH}	Cutoff	Linear
V_{IL}	Saturation	Linear
V_M	Saturation	Saturation
V_{IH}	Linear	Saturation
V_{OL}	Linear	Cutoff





Symmetric CMOS Inverter

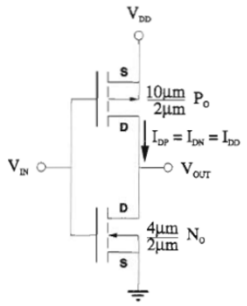


FIGURE 23.5 Symmetric CMOS Inverter with $W_P/L_P = 2.5\ W_N/L_N$

Capacitance Effect on Transition - 1

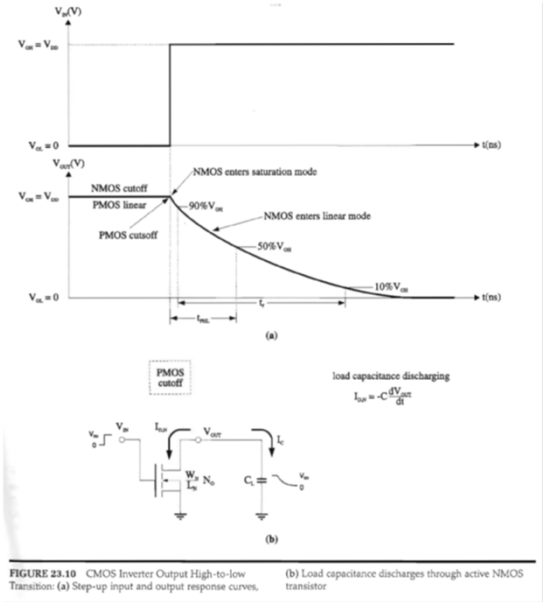


FIGURE 23.10 CMOS Inverter Output High-to-low Transition: **(a)** Step-up input and output response curves, **(b)** Load capacitance discharges through active NMOS transistor

Capacitance Effect on Transition - 2

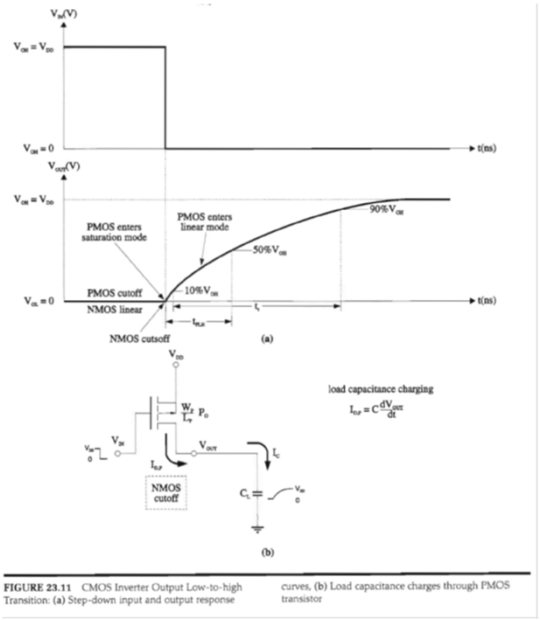


FIGURE 23.11 CMOS Inverter Output Low-to-high Transition: (a) Step-down input and output response curves, (b) Load capacitance charges through PMOS transistor

Electrostatic Discharge (ESD) Protection

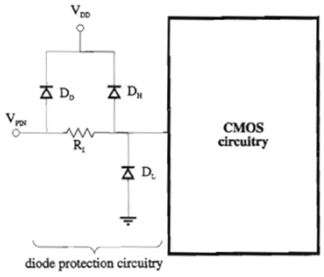


FIGURE 23.20 Diode Input Protection Circuitry for Metal-gate CMOS

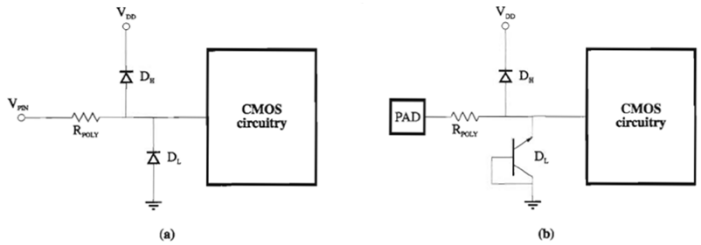
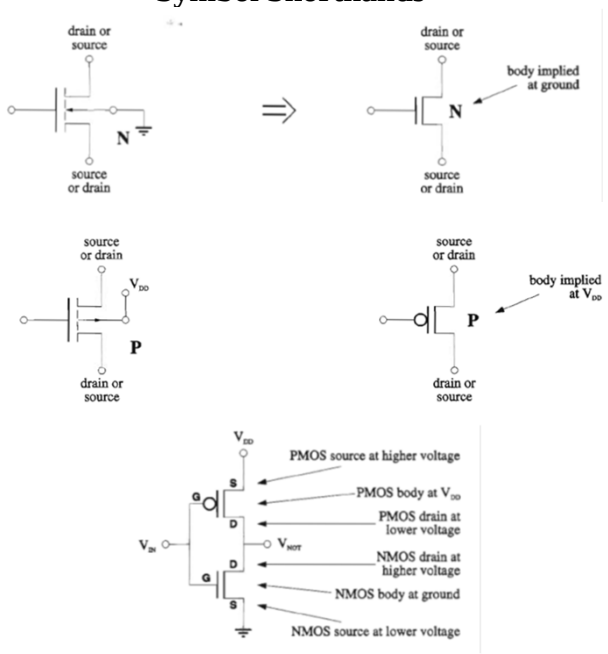


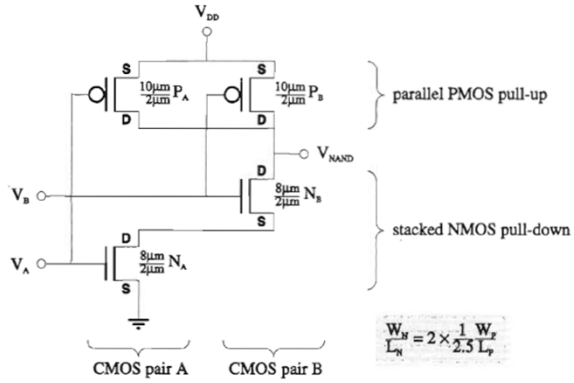
FIGURE 23.21 Diode Input Protection Circuitry for Silicon Gate CMOS: (a) Circuitry, (b) D_L is layed out as a base-collector connected BJT diode

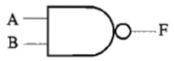
CMOS Gates

Symbol Shorthands



CMOS NAND Gate

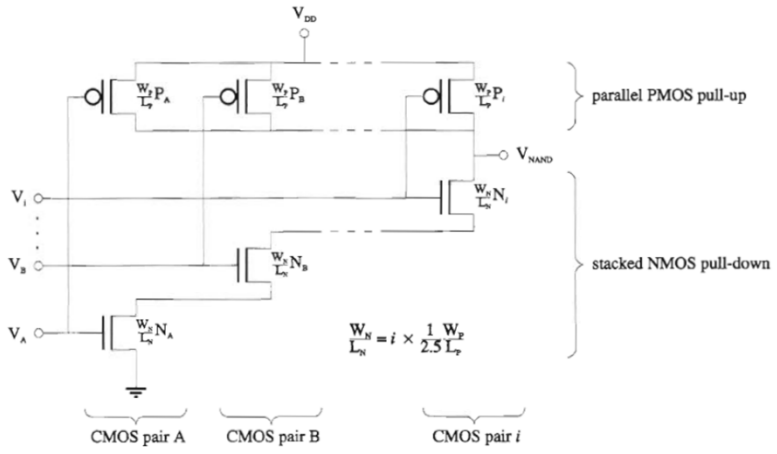




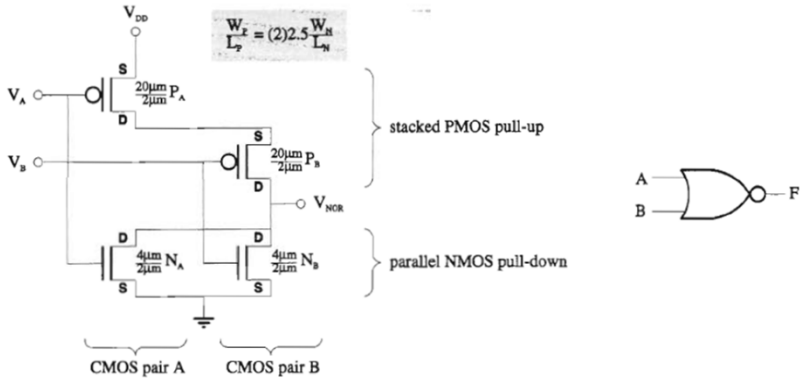
V_A	V_B	N_A	N_B	P_A	P_B	Pull-Up Path(s)	Pull-Down Path	V_{OUT}
low	low	off	off	on	on	P_A, P_B*	none	high
low	high	off	on	on	off	P_A	none	high
high	low	on	off	off	on	P_B	none	high
high	high	on	on	off	off	none	N_A and N_B**	low

*For V_A and V_B low, two output pull-up paths to V_{DD} are present through P_A and P_B
**For V_A and V_B high, a single output pull-down path to ground through N_A and N_B is present

CMOS NAND Gates



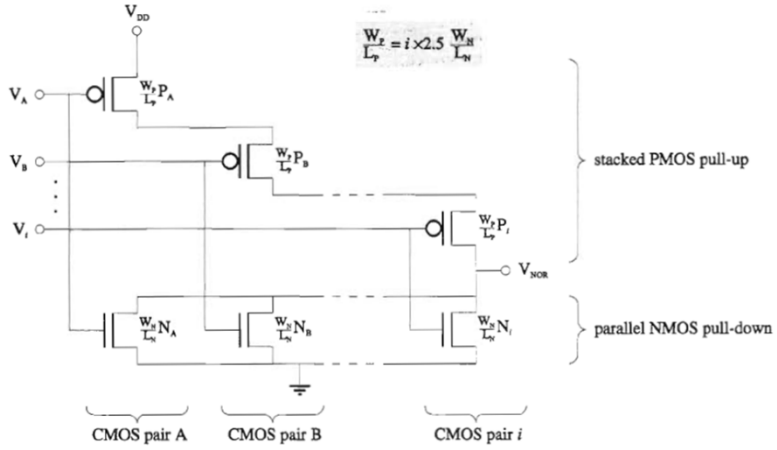
CMOS NOR Gate



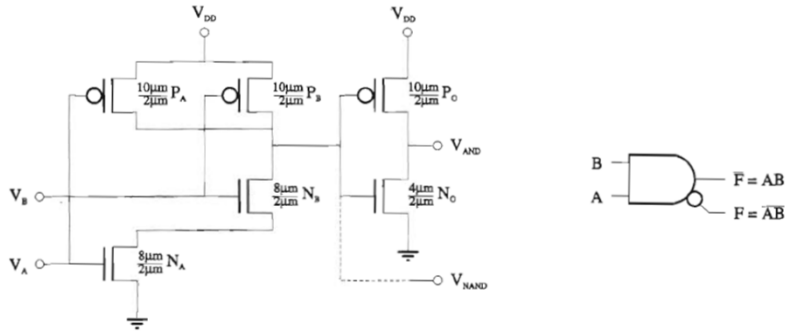
V_A	V_B	N_A	N_B	P_A	P_B	Pull-Up Path	Pull-Down Path(s)	V_{OUT}
low	low	off	off	on	on	P_A and P_B*	none	high
low	high	off	on	on	off	none	N_B	low
high	low	on	off	off	on	none	N_A	low
high	high	on	on	off	off	none	N_A, N_B**	low

*For V_A and V_B low a single output pull-up path to V_{DD} through P_A and P_B is present
**For V_A and V_B high two output pull-down paths to ground are present through N_A and N_B

CMOS NOR Gates



CMOS AND/NAND Gate



CMOS OR/NOR Gate

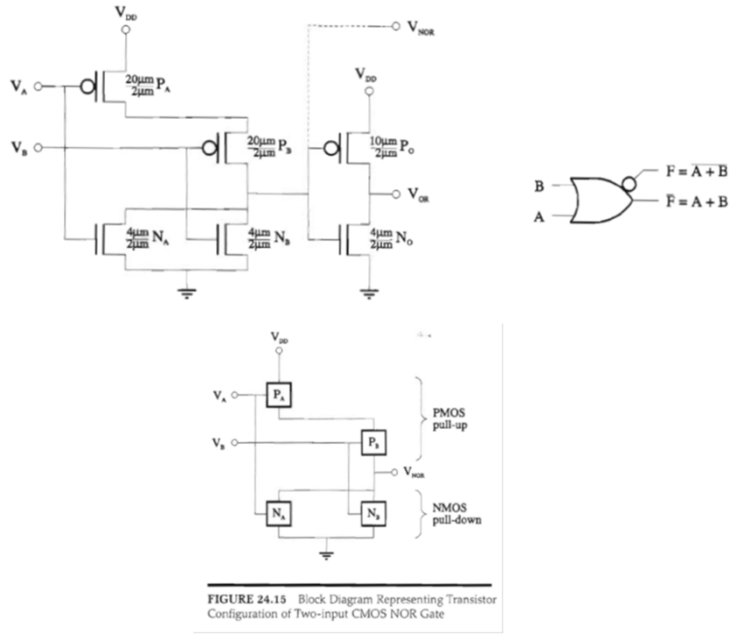
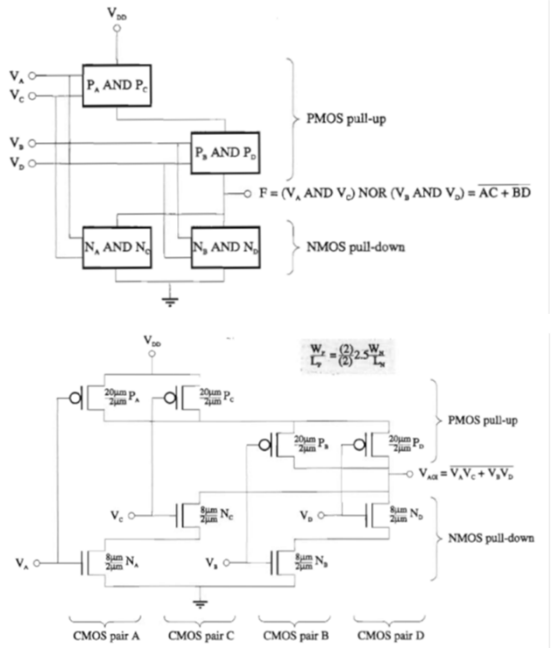
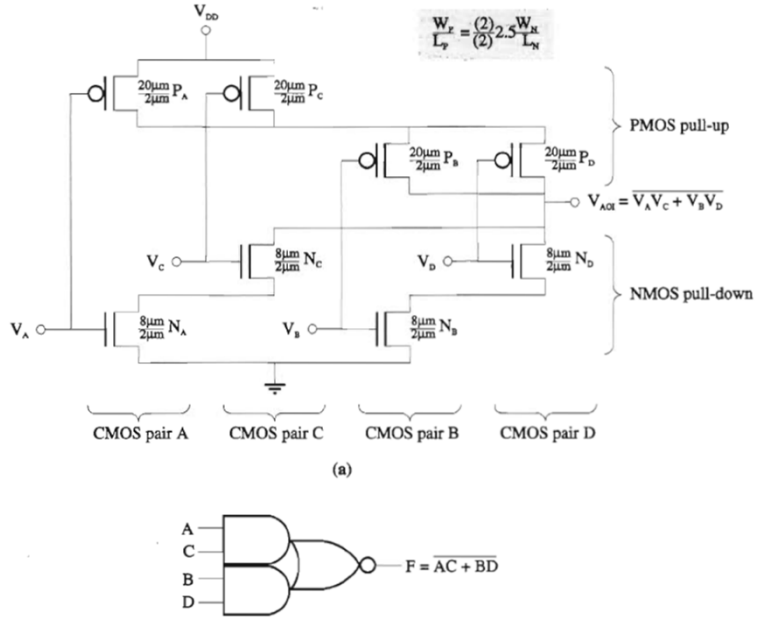


FIGURE 24.15 Block Diagram Representing Transistor Configuration of Two-input CMOS NOR Gate

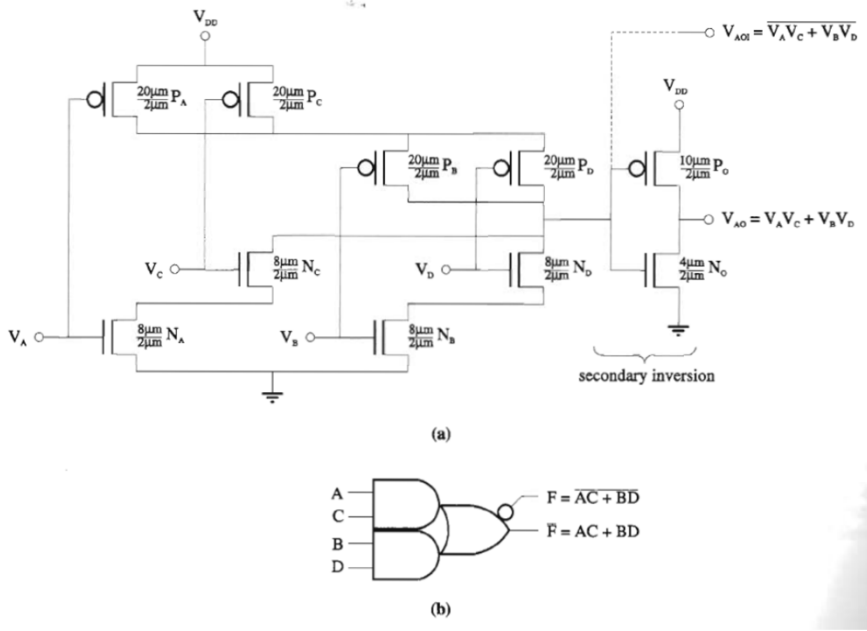
CMOS AOI Gates



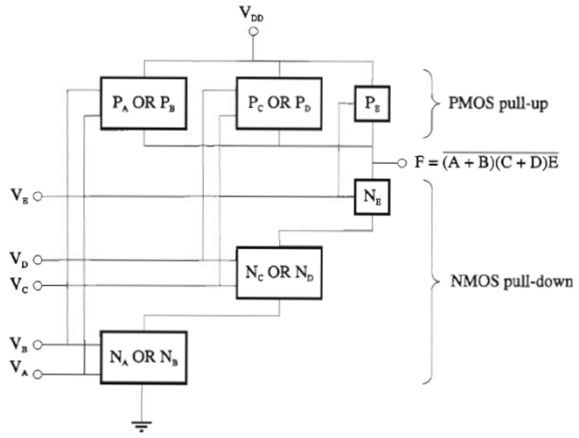
CMOS AOI Gates



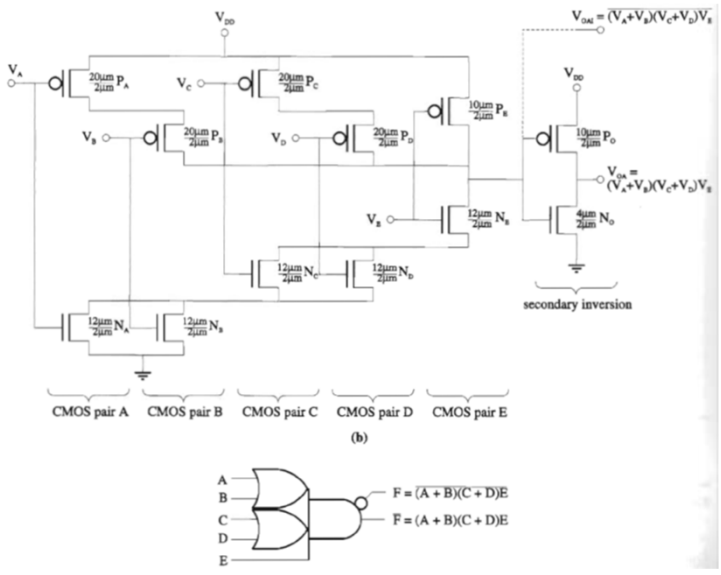
CMOS AND-OR Gate



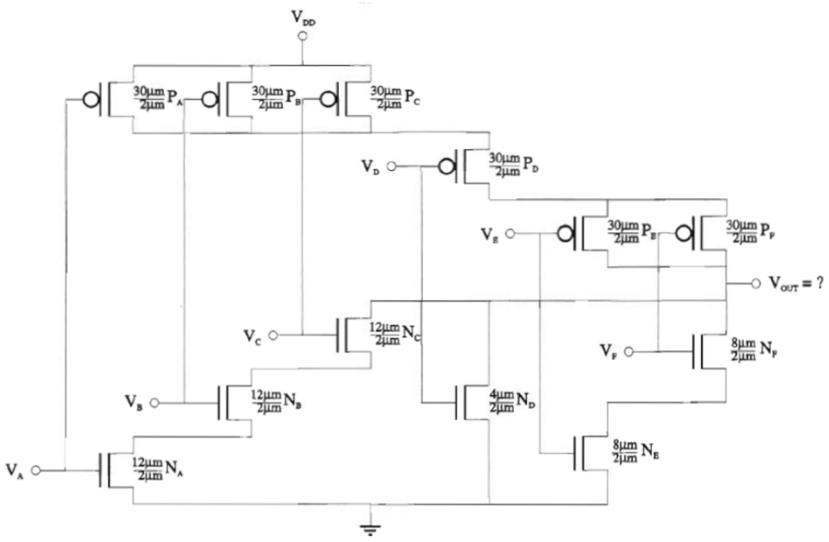
CMOS OAI Gates

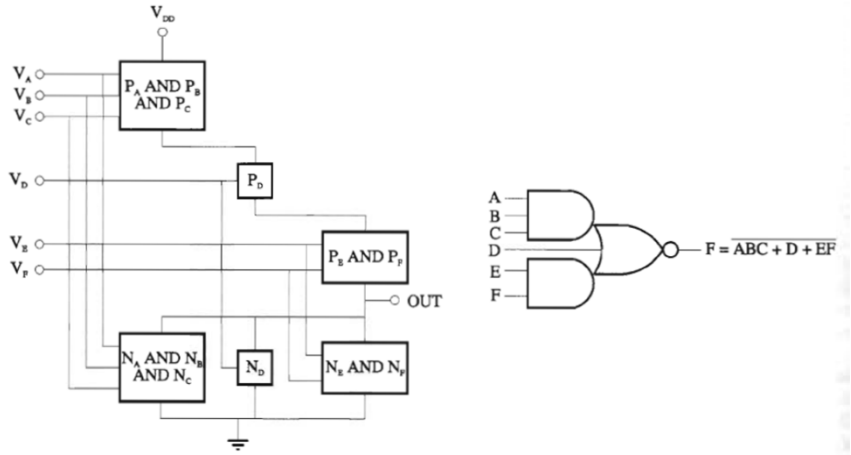


CMOS AOI Gates

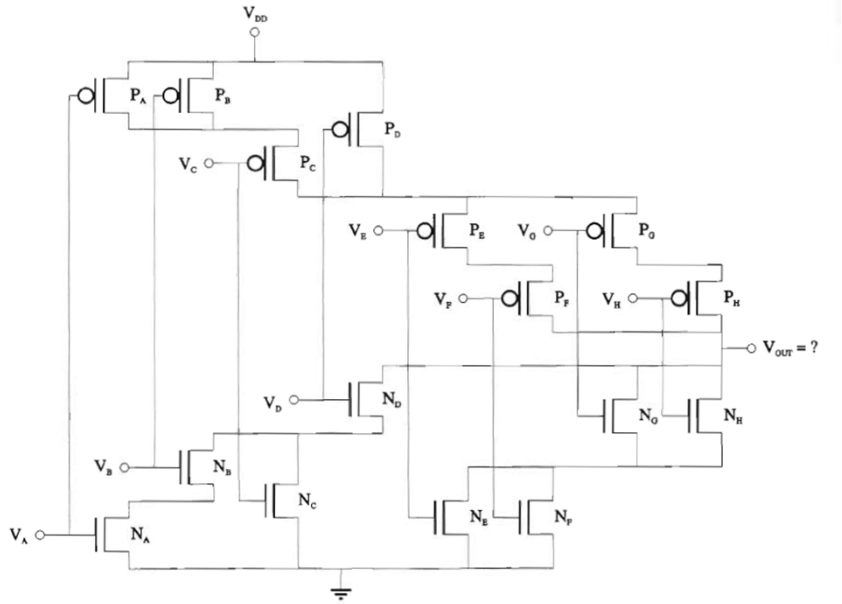


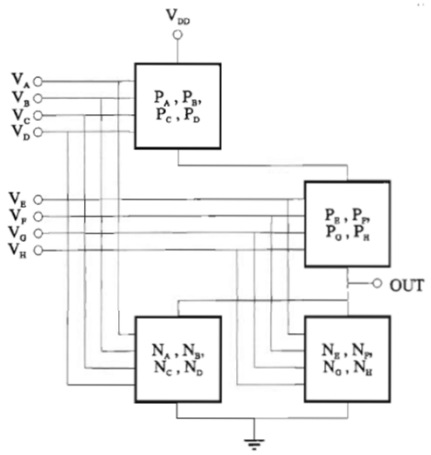
Example

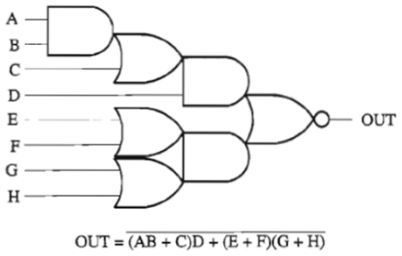



V_{DD}
V_A
V_B
V_C
P_A AND P_B AND P_C
V_D
P_D
V_E
V_F
P_E AND P_F
OUT
N_A AND N_B AND N_C
N_D
N_E AND N_F
A
B
C
D
E
F
$F = \overline{ABC + D + EF}$

Example


V_{DD}
P_A
P_B
P_D
V_C
P_C
V_E
P_E
V_G
P_G
V_F
P_F
V_H
P_H
$V_{OUT} = ?$
V_D
N_D
N_G
N_H
V_B
N_B
N_C
N_E
N_F
V_A
N_A





$$OUT = \overline{(AB + C)D + (E + F)(G + H)}$$

XOR Gate