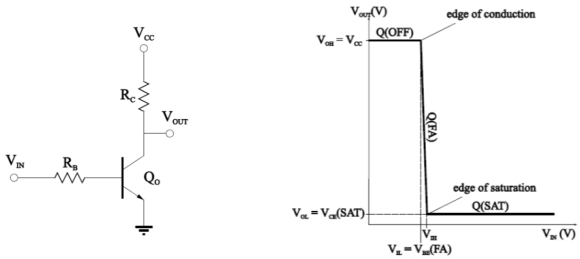
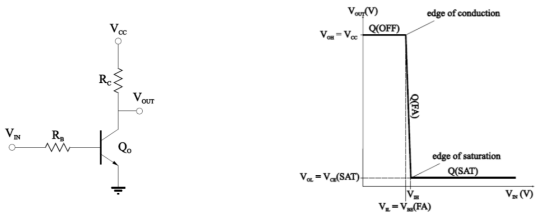
Contents

Resistor-Transistor Logic (RTL)

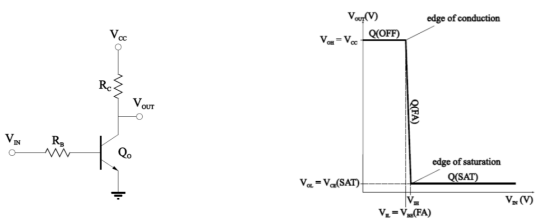
- Resistor-Transistor Logic (RTL) which is introduced in 1962, is constructed from resistors and BJTs as shown in the figure on the left below.



- A basic RTL inverter and its VTC are shown in the figure on the left and right above, respectively.



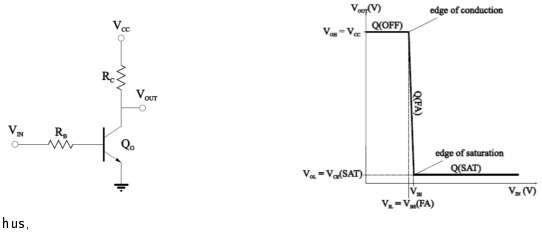
- Here, Q_O is in cutoff (OFF) state when the input voltage is zero, i.e., $V_{IN} = 0$, consequently output is HIGH as $V_{OUT} = V_{CC}$ (because $I_C = 0$).
- When the input voltage is enough, i.e., $V_{IN} = V_{BE(FA)}$, to turn on Q_O into the forward active (FA) mode, then current I_C will start to flow.
- Hence, V_{OUT} starts to drop with increasing V_{IN} as $V_{OUT} = V_{CC} - I_C R_C$, $I_C = \beta_F I_B$ and $I_B = \frac{V_{IN} - V_{BE,O(FA)}}{R_B}$.
- If we increase V_{IN} further, at some point (i.e., when $V_{IN} = V_{IH}$) Q_O goes into saturation. Consequently, output becomes LOW and remains constant at $V_{OUT} = V_{CE(SAT)}$.



- We can summarize the state of the BJT transistor Q_O for output-high and output-low states as indicated in the table below.

State of Active Elements for Output-High and Output-Low States

Element	V_{OH}	V_{OL}
Q_O	Cutoff (OFF)	Saturated (SAT)

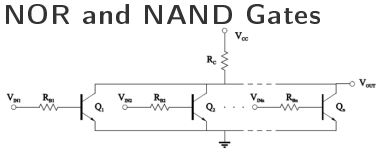


- Thus,

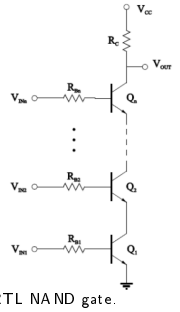
$$
\begin{aligned}
V_{OH} &= V_{CC} \\
V_{OL} &= V_{CE(SAT)} \\
V_{IL} &= V_{BE(FA)} \\
V_{IH} &= I_{B(EOS)} R_B + V_{BE(EOS)} \\
&= \frac{I_{C(EOS)}}{\beta_F} R_B + V_{BE(EOS)} \\
&= \frac{V_{CC} - V_{CE(EOS)}}{\beta_F R_C} R_B + V_{BE(EOS)}
\end{aligned}
$$

where EOS is **edge of saturation**, and hence $V_{BE(EOS)} = V_{BE(SAT)}$ and $V_{CE(EOS)} = V_{CE(SAT)}$.

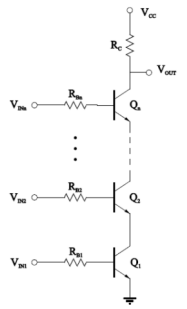
Basic RTL NOR and NAND Gates



- Figure above shows a basic RTL NOR gate.



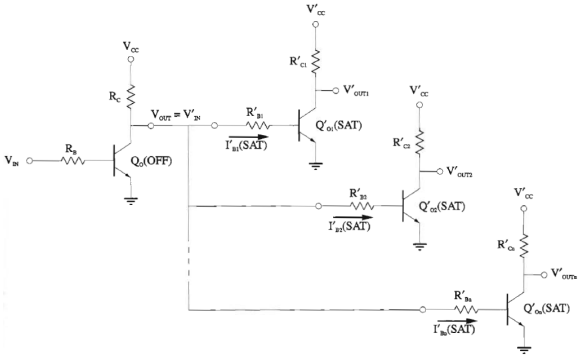
- Figure above shows a basic RTL NAND gate.

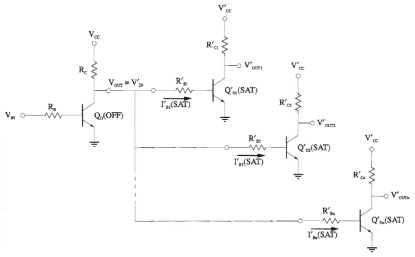


Example 1: For the basic RTL NAND gate above, determine the maximum fan-in if all stack BJTs have $V_{CE(SAT)} = 0.17\,\text{V}$ and all load gates have $V_{BE(FA)} = 0.7\,\text{V}$.

Basic RTL Fan-Out

- When a basic RTL inverter is in **output-low** state, any load gate would be in cutoff mode and draw no input current.
- Thus, maximum fan-out will be determined by the **output-high** state as shown below.



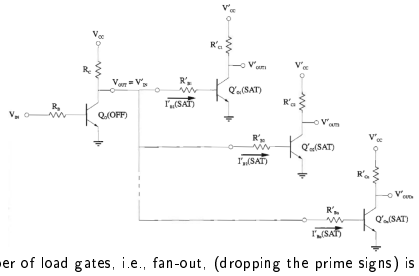


- Output voltage is given by $V_{OH} = V_{CC} - I_{OH}R_C$ where $I_{OH} = I_{RC}$ and $V_{OUT} = V_{OH}$. So, $\boldsymbol{V_{OH}}$ is **not constant** and decreases with each added load gates, as the output current I_{OH} increases by each added load gate.
- Thus, output current I_{OH} which is the sum of the identical input currents I'_{IH} of N load gates, is given by

$$I_{OH} = \frac{V_{CC} - V_{OH}}{R_C} = NI'_{IH}$$

where I'_{IH} is given by

$$I'_{IH} = \frac{V_{OH} - V'_{BE(SAT)}}{R'_B}.$$



- Then, number of load gates, i.e., fan-out, (dropping the prime signs) is given by

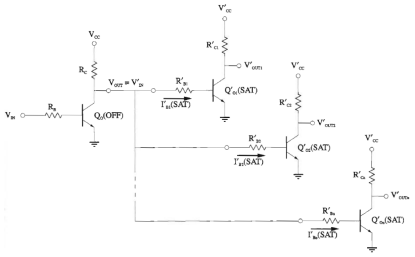
$$N = \frac{V_{CC} - V_{OH}}{V_{OH} - V_{BE(SAT)}} \frac{R_B}{R_C}$$

- Consequently, **maximum fan-out** is given by

$$N_{\text{max}} = \left\lfloor \frac{V_{CC} - V_{OH(\text{min})}}{V_{OH(\text{min})} - V_{BE(SAT)}} \frac{R_B}{R_C} \right\rfloor$$

- As $V_{OH(\text{min})} = V_{IH}$,

$$\boxed{N_{\text{max}} = \left\lfloor \frac{V_{CC} - V_{IH}}{V_{IH} - V_{BE(SAT)}} \frac{R_B}{R_C} \right\rfloor}$$



Example 2: Determine the maximum fan-out for a basic RTL inverter with $V_{CC} = 5\,\text{V}$, $R_B = 10\,\text{k}\Omega$, $R_C = 1\,\text{k}\Omega$, $\beta_F = 25$, $V_{BE(SAT)} = 0.8\,\text{V}$ and $V_{CE(SAT)} = 0.2\,\text{V}$.

Basic RTL Power Dissipation

- As $V_{OL} = V_{CE(SAT)}$ all load gates will be in cutoff mode. So, **output-low current supplied** is independent of load gates and given by

$$I_{CC(OL)} = \frac{V_{CC} - V_{CE,O(SAT)}}{R_C}$$

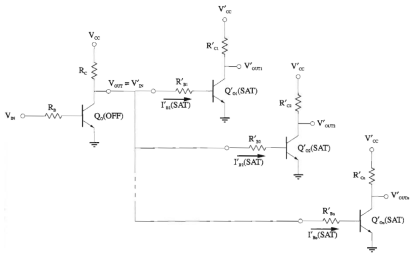
- However, **output-high current supplied** depends on the number of load gates connected and given by

$$I_{CC(OH)} = \frac{V_{CC} - V'_{BE(SAT)}}{R_C + R'B/N}$$

If there is no load, $I_{CC(OH)} = 0$.

- Consequently, **average power dissipation** is given by

$$P_{CC(\text{avg})} = \frac{I_{CC(OL)} + I_{CC(OH)}}{2} V_{CC}$$

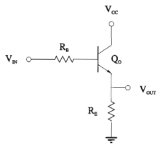


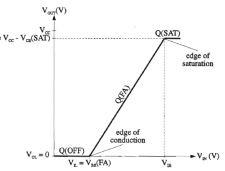
Example 3: Consider a basic RTL inverter with $V_{CC} = 5\,\text{V}$, $R_B = 10\,\text{k}\Omega$, $R_C = 1\,\text{k}\Omega$, $\beta_F = 25$, $V_{BE(SAT)} = 0.8\,\text{V}$ and $V_{CE(SAT)} = 0.2\,\text{V}$. Find the average power dissipated

a) no load

b) a fan-out of 1.

Basic RTL Non-Inverter

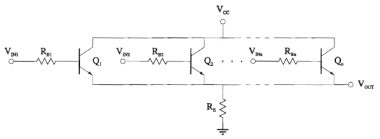




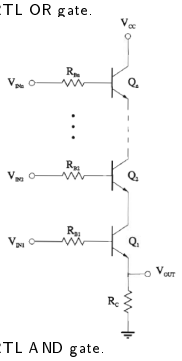
- For the basic RTL non-inverter shown in the figure above

$$\begin{aligned} V_{OH} &= V_{CC} - V_{CE(SAT)} \\ V_{OL} &= 0\,\text{V} \\ V_{IL} &= V_{BE(FA)} \\ V_{IH} &= I_{B(EOS)} R_B + V_{BC(EOS)} + V_{CC} \\ &= \frac{I_{E(EOS)}}{\beta_F + 1} R_B + V_{BC(EOS)} + V_{CC} \\ &= \frac{V_{CC} - V_{CE(EOS)}}{\beta_F + 1} \frac{R_B}{R_E} + V_{BC(EOS)} + V_{CC} \end{aligned}$$

where EOS is **edge of saturation**, and hence $V_{BC(EOS)} = V_{BC(SAT)}$ and $V_{CE(EOS)} = V_{CE(SAT)}$.

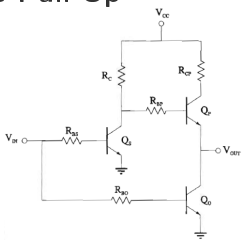


- Figure above shows a basic RTL OR gate.



- Figure above shows a basic RTL AND gate.

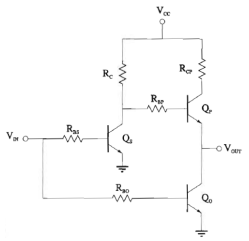
RTL with Active Pull-Up



- A method to increase the fan-out of RTL gates is to have an active pull-up configuration as shown in the figure above, where the purpose of each element in the circuit is listed in the table below.

Purpose of Each Element

Element	Purpose
R_{BS}, R_{BO}	Matched input resistors
Q_S	Drive splitter and pull-down of Q_P
R_C	Along with Q_S provides logic-inversion to output-high driver
R_{BP}	Limits base current to Q_P
Q_O	Output inverting BJT and active pull-down for output-low driver
Q_P	Provides active pull-up for output-high driver
R_{CP}	Part of active pull-up

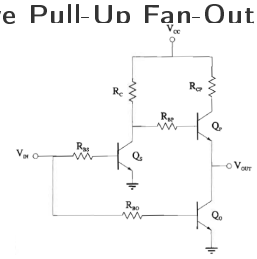


- The states of active elements are given in the table below.

State of Active Elements for Output-High and Output-Low States

Element	V_{OH}	V_{OL}
Q_O	Cutoff (OFF)	Saturated (SAT)
Q_S	Cutoff (OFF)	Saturated (SAT)
Q_P	Saturated (SAT) (for fan-out ≥ 1)	Cutoff (OFF)
	Edge of conduction (EOC) (for no load)	

RTL with Active Pull-Up Fan-Out

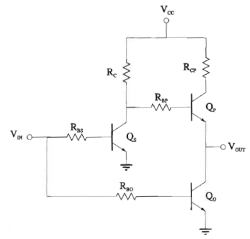


- Maximum fan-out will be determined by the **output-high** state.
- Output current $I_{OH} = I_{E,P(SAT)} = I_{C,P(SAT)} + I_{B,P(SAT)}$ which is the sum of the identical input currents I'_{IH} of N load gates, is given by

$$I_{OH} = \frac{V_{CC} - V_{CE,P(SAT)} - V_{OH}}{R_{CP}} + \frac{V_{CC} - V_{BE,P(SAT)} - V_{OH}}{R_C + R_{BP}} = N I'_{IH}$$

where I'_{IH} is

$$I'_{IH} = \frac{V_{OH} - V'_{BE(SAT)}}{R'_B/2}.$$

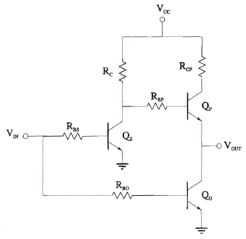


- Then, number of load gates, i.e., fan-out, (dropping the prime signs) is given by

$$N = \frac{V_{CC} - V_{CE(SAT)} - V_{OH}}{V_{OH} - V_{BE(SAT)}} \frac{R_B}{2R_{CP}} + \frac{V_{CC} - V_{BE(SAT)} - V_{OH}}{V_{OH} - V_{BE(SAT)}} \frac{R_B}{2(R_C + R_{BP})}$$

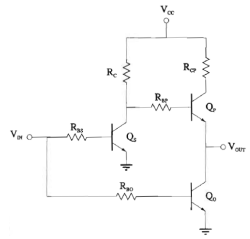
- As $V_{OH(\text{min})} = V_{IH}$, **maximum fan-out** is given by

$$N_{\text{max}} = \left\lfloor \frac{V_{CC} - V_{CE(SAT)} - V_{IH}}{V_{IH} - V_{BE(SAT)}} \frac{R_B}{2R_{CP}} + \frac{V_{CC} - V_{BE(SAT)} - V_{IH}}{V_{IH} - V_{BE(SAT)}} \frac{R_B}{2(R_C + R_{BP})} \right\rfloor$$



- If we ignore $I_{B,P(SAT)}$ (i.e., $(R_C + R_{BP}) \gg R_{CP}$), **maximum fan-out** simplifies to

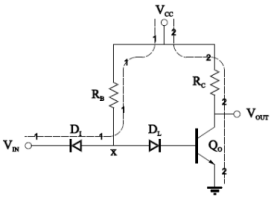
$$\boxed{N_{\text{max}} \approx \left\lfloor \frac{V_{CC} - V_{CE(SAT)} - V_{IH}}{V_{IH} - V_{BE(SAT)}} \frac{R_B}{2R_{CP}} \right\rfloor}$$

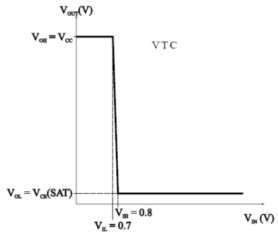


Example 4: Compare the maximum fan-out for the RTL inverter with active pull-up with that of basic RTL inverter where $V_{CC} = 5\,\text{V}$, $R_{BP} = R_{BS} = R_{BO} = 10\,\text{k}\Omega$, $R_C = 1\,\text{k}\Omega$, $R_{CP} = 100\,\Omega$, $V_{BE(SAT)} = 0.8\,\text{V}$, $V_{CE(SAT)} = 0.2\,\text{V}$ and $\beta_F = 25$.

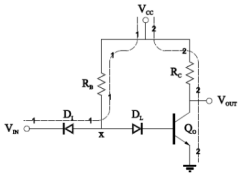
Diode-Transistor Logic (DTL)

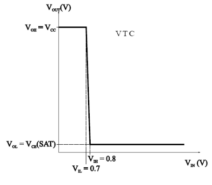
- Diode-Transistor Logic (DTL) which is introduced in 1964 in order to overcome the low fan-out of RTL, is constructed from diodes and BJTs as shown in the figure on the left below.





- A basic DTL inverter and its VTC are shown in the figure on the left and right above, respectively.

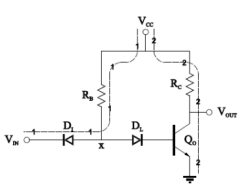


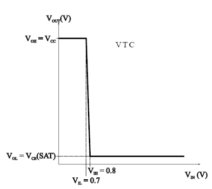


- When the input is low, e.g., $V_{IN} = 0\,\text{V}$, input diode D_I is forward biased so the voltage V_x between the diodes will be $V_x = V_{IN} + V_{D,I(ON)}$ and thus as $V_{BE,O} = V_x - V_{D,L(ON)} = V_{IN}$, output transistor Q_O will be in **cutoff** mode. Consequently, output is HIGH as $V_{OUT} = V_{CC}$ (because $I_C = 0$)

$$V_x = V_{IN} + V_{D,I(ON)} \qquad (\text{while } V_{IN} < V_{BE(SAT)})$$
$$V_{BE,O} = V_x - V_{D,L(ON)}$$
$$V_{BE,O} = V_{IN}$$

- When the input voltage is high enough, i.e., $V_{IN} = V_{BE(FA)}$, to turn on Q_O into the forward active (FA) mode, then current I_C will start to flow.
- Hence, V_{OUT} starts to drop with increasing V_{IN} as $V_{OUT} = V_{CC} - I_C R_C$.
- If we increase V_{IN} further, at some point (i.e., when $V_{IN} = V_{BE(SAT)}$), Q_O goes into saturation and D_I starts to turn off. As a result, V_{OUT} becomes LOW and remains constant at $V_{OUT} = V_{CE,O(SAT)}$.

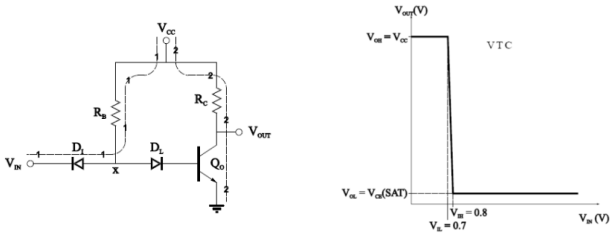




- We can summarize the state of the active elements for output-high and output-low states as indicated in the table below.

State of Active Elements for Output-High and Output-Low States

Element	V_{OH}	V_{OL}
Q_O	Cutoff (OFF)	Saturated (SAT)
D_L	Edge of Conduction (EOC)	Conducting (ON)
D_I	Conducting (ON)	Cutoff (OFF)

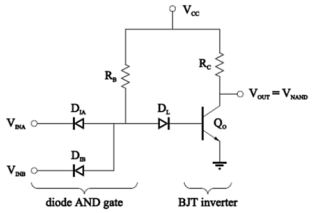


- Thus,

$$V_{OH} = V_{CC}$$
$$V_{OL} = V_{CE(SAT)}$$
$$V_{IL} = V_{BE(FA)}$$
$$V_{IH} = V_{BE(SAT)}$$

Basic DTL NAND Gate

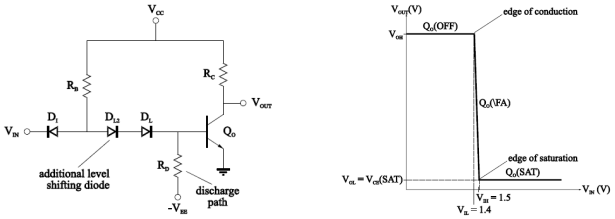
- NAND function is inherently provided by the DTL logic family by adding diodes in parallel at the input pointing outward (i.e., towards the input) as shown in the figure below for a two-input basic DTL NAND gate.



Example 5: Consider the DTL NAND gate in the figure above, and determine

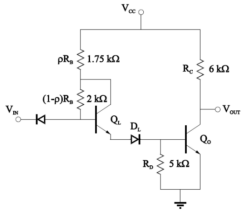
a) Truth table for V_{INA}, V_{INB} and V_{OUT} (using LOW-HIGH states),
b) States of D_{IA}, D_{IB} and Q_O when $V_{INA} = 0.4\,\text{V}$ and $V_{INB} = 0.7\,\text{V}$,
c) States of D_{IA}, D_{IB} and Q_O when $V_{INA} = 0.3\,\text{V}$ and $V_{INB} = 0.4\,\text{V}$,
d) States of D_{IA}, D_{IB} and Q_O when $V_{INA} = 0.53\,\text{V}$ and $V_{INB} = 0.55\,\text{V}$.

Diode Modified DTL



- As shown in the figure on the left above, basic DTL inverter can be improved by
  - by an additional diode D_{L2} to improve noise-margin-low V_{NML}.
  - by an additional discharge path (consisting of R_D and $-V_{EE}$) to the base of Q_O to improve the switching time from saturation to cutoff (i.e., to increase the low-to-high switching speed).

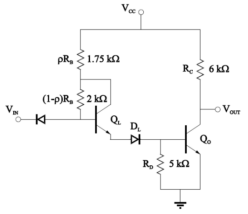
Transistor Modified DTL



- The fan-out of the modified DTL can be further increased by replacing D_{L2} with a self-biased BJT Q_L (prevented from going into saturation mode by ensuring always $V_{BC} < 0$) as shown in the figure above, where the purpose of each element in the circuit is listed in the table below.

Purpose of Each Element

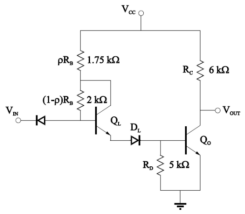
Element	Purpose
D_I	Input diode, provides ANDing and limits I_{IH}
ρR_B	Limits I_{IL}
$(1-\rho)R_B$	Self-biases Q_L and prevents Q_L from saturation
Q_L	Level shifting to improve V_{NML} and provides base driving current Q_O
D_L	Level-shifting diode for shifting transition width
R_D	Provides discharge path for saturation stored charge removal from base of Q_O
Q_O	Output inverting BJT and active pull-down for output-low driver
R_C	Part of passive pull-up



- The states of active elements in a transistor modified DTL inverter are given in the table below.

State of Active Elements for Output-High and Output-Low States

Element	V_{OH}	V_{OL}
Q_O	Cutoff (OFF)	Saturated (SAT)
D_L	Cutoff (OFF)	Conducting (ON)
Q_L	Cutoff (OFF)	Forward Active (FA)
D_I	Conducting (ON)	Cutoff (OFF)

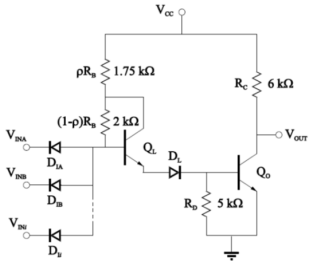


- Thus,

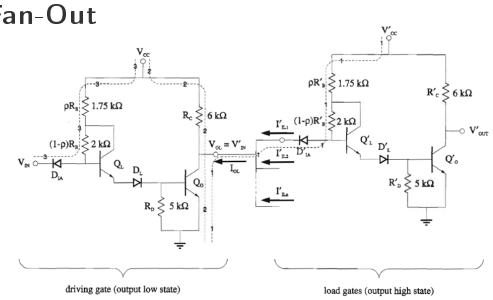
$$V_{OH} = V_{CC}$$
$$V_{OL} = V_{CE,O(SAT)}$$
$$V_{IL} = V_{BE,L(FA)} + V_{BE,O(FA)}$$
$$V_{IH} = V_{BE,L(FA)} + V_{BE,O(SAT)}$$

DTL NAND Gate

- NAND function is inherently provided by the DTL logic family by adding diodes in parallel at the input pointing outward as shown in the figure below.



DTL Fan-Out

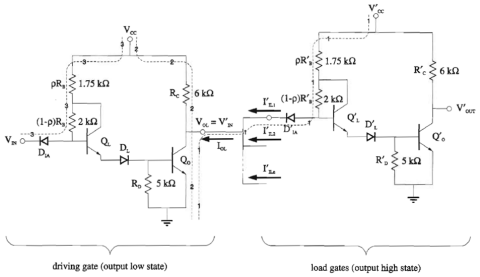


- Maximum fan-out will be determined by the **output-low** state, as when output is high input diode D'_I is cutoff (i.e., $I'_{IH} = 0$).
- From Path 2 and Path 1,

$$I_{OL} = I_{C,O(SAT)} - I_{RC(OL)}$$

$$I_{RC(OL)} = \frac{V_{CC} - V_{CE,O(SAT)}}{R_C}$$

$$I_{C,O(SAT)} = \sigma\beta_F I_{B,O(SAT)}$$



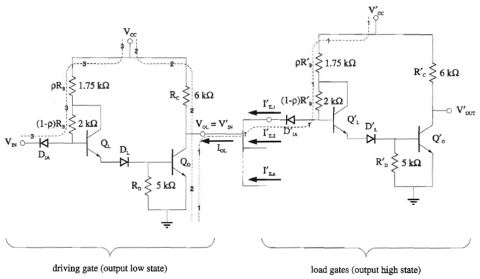
- Continuing,

$$I_{B,O(SAT)} = I_{E,L(FA)} - I_{RD(OL)}$$

$$I_{RD(OL)} = \frac{V_{BE,O(SAT)}}{R_D}$$

$$I_{E,L(FA)} = \frac{V_{CC} - V_{BE,L(FA)} - V_{D,L(ON)} - V_{BE,O(SAT)}}{\rho R_B + (1-\rho)\, R_B/\,(\beta_F + 1)}$$

$$\approx \frac{V_{CC} - V_{BE,L(FA)} - V_{D,L(ON)} - V_{BE,O(SAT)}}{\rho R_B}$$



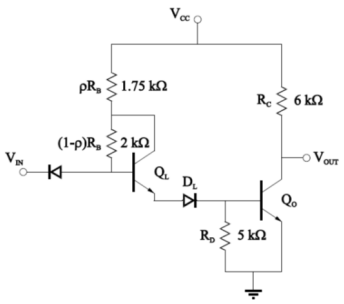
- From Path 1,

$$I'_{IL} = \frac{V_{CC} - V_{D,I(ON)} - V_{CE,O(SAT)}}{R_B}$$

- Thus, the **maximum fan-out** is given by

$$N_{\max} = \left\lfloor \frac{I_{OL(\max)}}{I'_{IL}} \right\rfloor = \left\lfloor \frac{I_{C,O(SAT)(\max)} - I_{RC(OL)}}{I'_{IL}} \right\rfloor$$

$$= \left\lfloor \frac{\sigma_{\max}\beta_F I_{B,O(SAT)} - I_{RC(OL)}}{I'_{IL}} \right\rfloor$$



Example 6: For the DTL gate above, determine the maximum fan-out for $\beta_F = 49$ and $\sigma_{\max} = 0.85$.

DTL Power Dissipation

Example 7: Calculate the average power dissipation for Example 6 above?