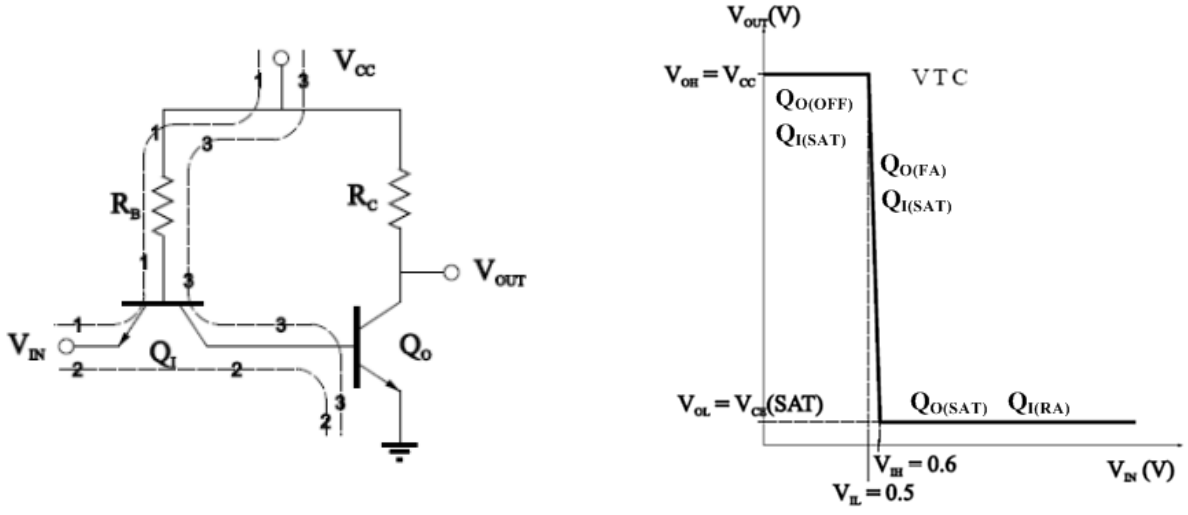
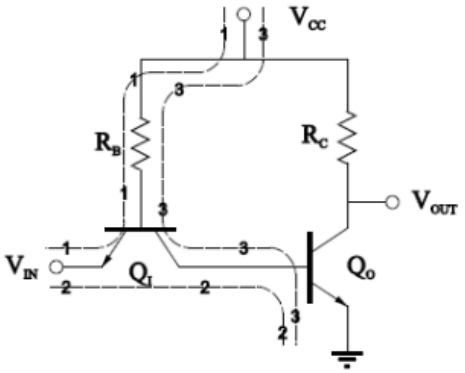
Contents

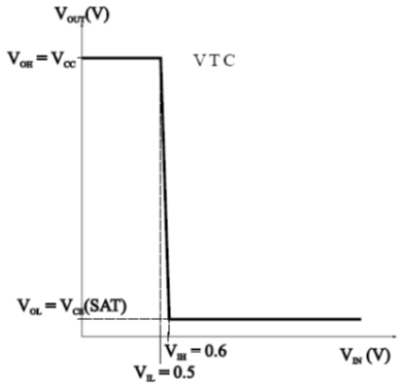
Transistor-Transistor Logic (TTL)

- Transistor-Transistor Logic (TTL) which is introduced in 1965 in order to provide increased fan-out, improved transient response and reduced chip area.



- A basic TTL inverter and its VTC are shown in the figure on the left and right above, respectively.
- Compare the TTL inverter with the DTL inverter in order to see how diodes D_I and D_L are represented by the base-emitter and base-collector junctions of the input transistor Q_I which replaced these two diodes.

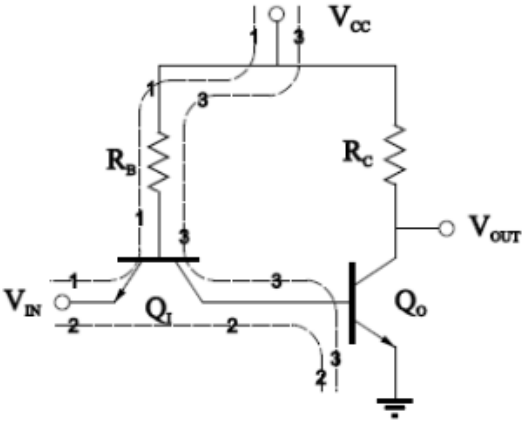


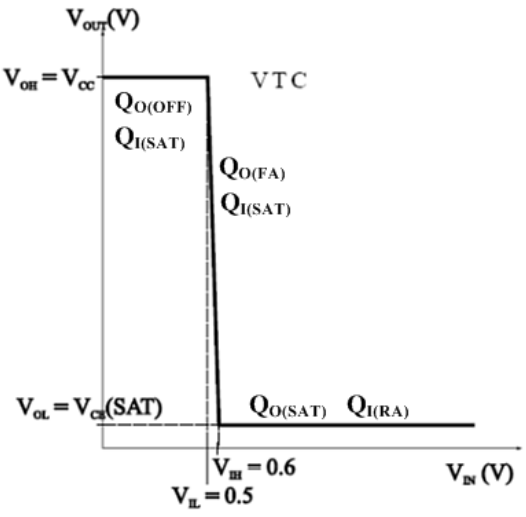


- When the input is low, e.g., $V_{IN} = 0\,\text{V}$, base-emitter junction of Q_I is forward biased, however voltage at the base of Q_I is not enough to turn on both base-collector junction of Q_I and base-emitter junction of Q_O, so Q_O is **cutoff**. So, collector current of Q_I is zero, i.e., $I_{C,I} = 0$. Thus, Q_I is in **saturation** mode (as $I_C < \beta_F I_B$).

$$V_{BE,O} = V_{IN} + V_{CE,I(SAT)} \qquad \text{(while } V_{IN} < V_{IH}\text{)}$$

- As Q_O is in **cutoff** mode when $V_{IN} = 0\,\text{V}$, the output is HIGH as $V_{OUT} = V_{CC}$.
- When the input voltage is high enough, i.e., $V_{IN} = V_{BE(FA)} - V_{CE(SAT)}$, Q_O goes into the forward active (FA) mode and current I_{RC} will start to flow. Then, V_{OUT} starts to drop with increasing V_{IN} as $V_{OUT} = V_{CC} - I_{RC}R_C$.
- If we increase V_{IN} further, at some point (i.e., when $V_{IN} = V_{BE(SAT)} - V_{CE(SAT)}$), Q_O goes into saturation and Q_I goes into reverse-active mode. As a result, V_{OUT} becomes LOW and remains constant at $V_{OUT} = V_{CE,O(SAT)}$.

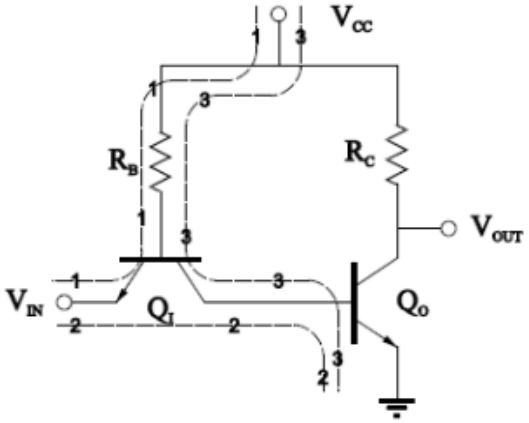


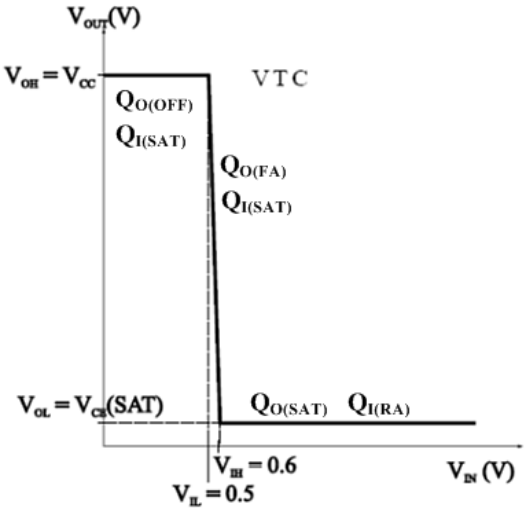


- We can summarize the state of the active elements for output-high and output-low states as indicated in the table below.

State of Active Elements for Output-High and Output-Low States

Element	V_{OH}	V_{OL}
Q_O	Cutoff (OFF)	Saturated (SAT)
Q_I	Saturated (SAT)	Reverse Active (RA)



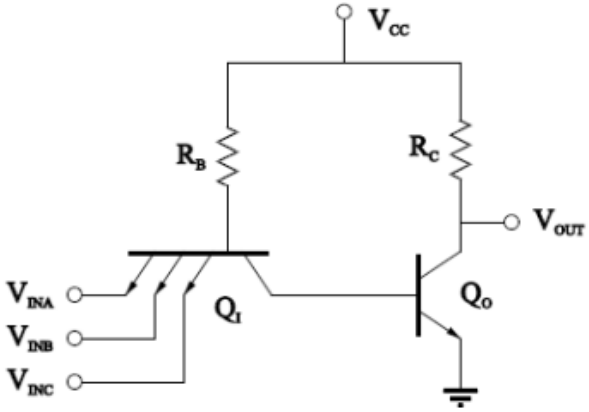


- Thus,

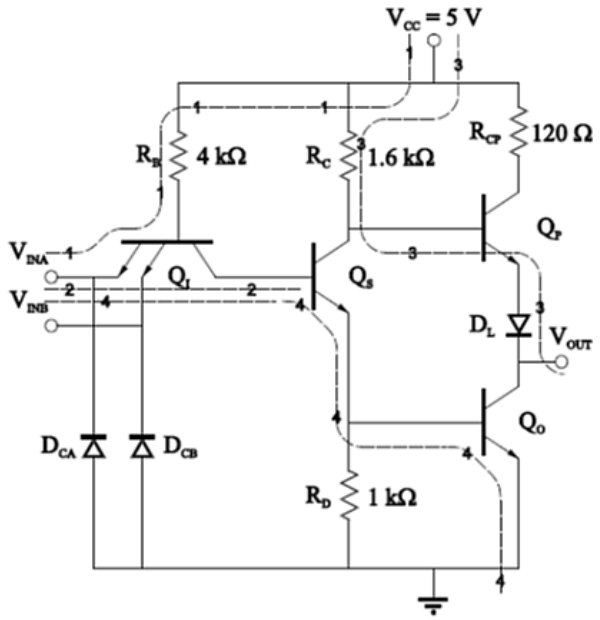
$$V_{OH} = V_{CC}$$
$$V_{OL} = V_{CE,O(SAT)}$$
$$V_{IL} = V_{BE,O(FA)} - V_{CE,I(SAT)}$$
$$V_{IH} = V_{BE,O(SAT)} - V_{CE,I(SAT)}$$

Basic TTL NAND Gate

- NAND function is inherently provided by the TTL logic family by using a multiple-emitter BJT (ensuring a much-less chip area) as shown in the figure below for a three-input basic TTL NAND gate.

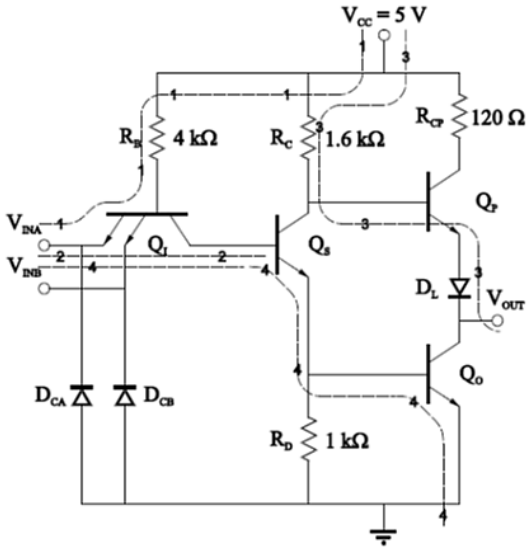


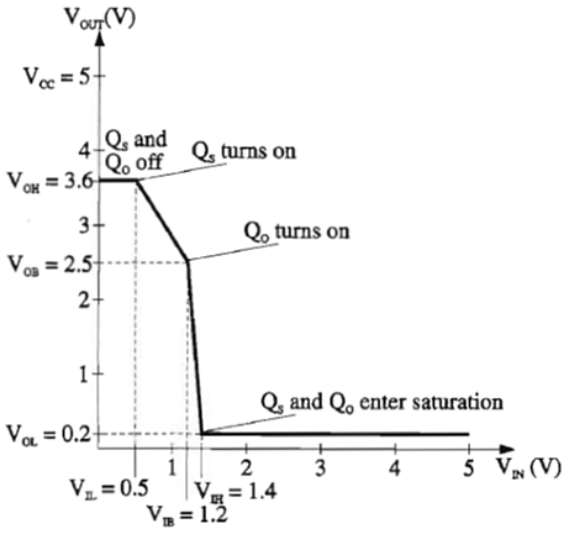
Standard TTL NAND Gate



Element	Purpose
Q_I	Multi-emitter input BJT, base-collector level shifting of transition width, pull-down of Q_S
R_B	Limits I_{IL}
Q_S	Drive splitter, provides base driving current to Q_O, base-emitter level shifting for shift of transition width, pull-down of Q_P
R_C	Along with Q_S provides logic inversion to output-high driver
Q_O	Output inverting BJT, output low driver for current sourcing pull-down
D_L	Diode level shifting between V_{CC} and output
R_D	Provides discharge path for saturation stored charge of Q_O
Q_P	Provides active current-sourcing pull-up
R_{CP}	Part of active pull-up and limits current spikes during output high-to-low transitions
D_{C1}, D_{C2}	Input clamping diodes to limit the negative swing of the inputs to one diode drop below ground

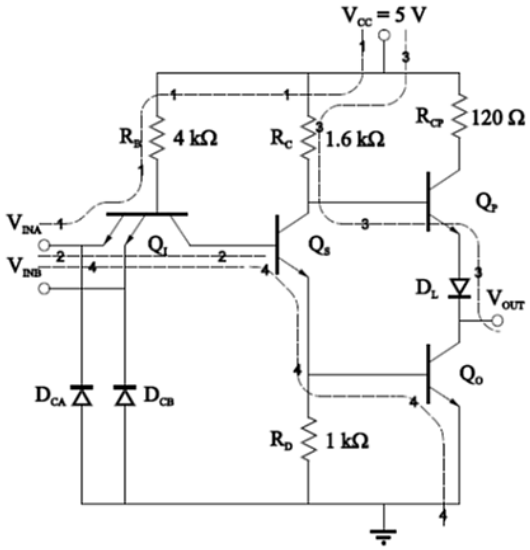
- Basic TTL inverter can be improved by adding a **totem-pole output** (stacking of two BJTs, a resistor and diode in the output branch) to provide active pull-up and pull-down sections, a drive-splitter transistor Q_S, a discharge resistor R_D and clamping diodes at the inputs as shown in the figure on the left above. The purpose of each element in the circuit is listed in the table on the right above.

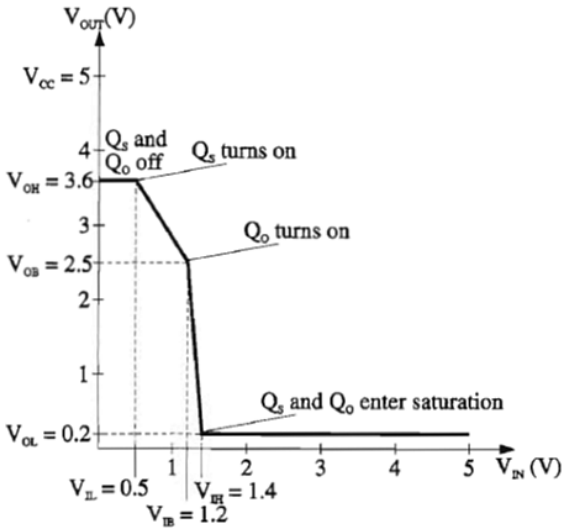




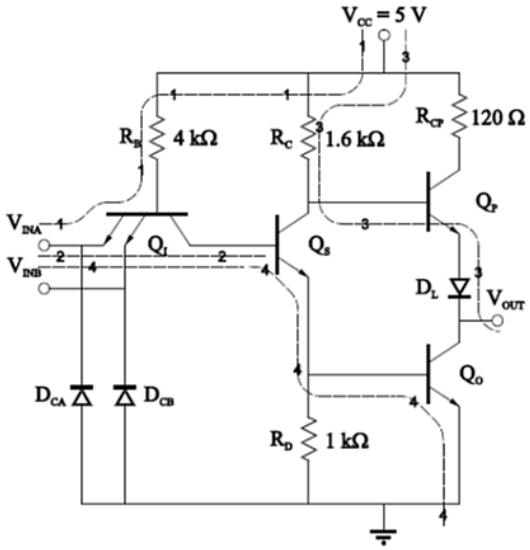
- When the input is low, e.g., $V_{IN} = 0$ V, base-emitter junction of Q_I is forward biased, however voltage at the base of Q_I is not enough to turn on both base-collector junction of Q_I and base-emitter junction of Q_S, so Q_S and Q_O are **cutoff**. So, collector current of Q_I is zero and Q_I is in **saturation** mode.
- When $V_{IN} = 0$ V, Q_S and Q_O are in **cutoff** mode and Q_P is in edge-of-conduction (EOC) mode (i.e., no current flows as there is no-load). So, as $I_{RC(OH)} = I_{B,P(EOC)} = 0$, the output is HIGH and given as

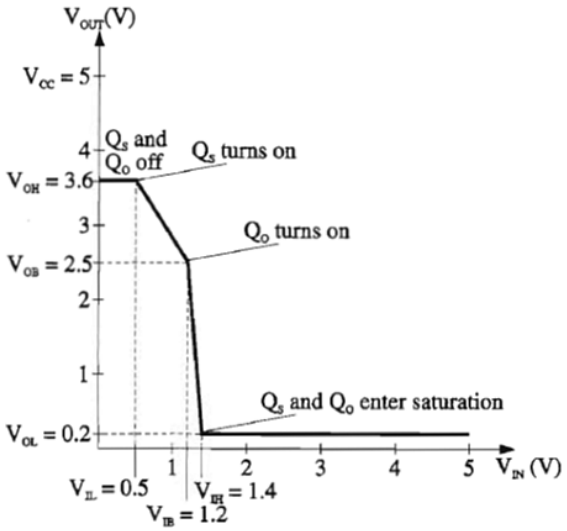
$$V_{OUT} = V_{CC} - I_{RC(OH)} R_C - V_{BE,P(EOC)} - V_{D,L(EOC)}$$
$$= V_{CC} - V_{BE,P(FA)} - V_{D,L(ON)}$$



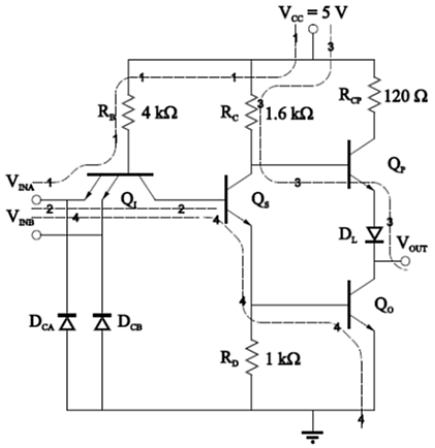


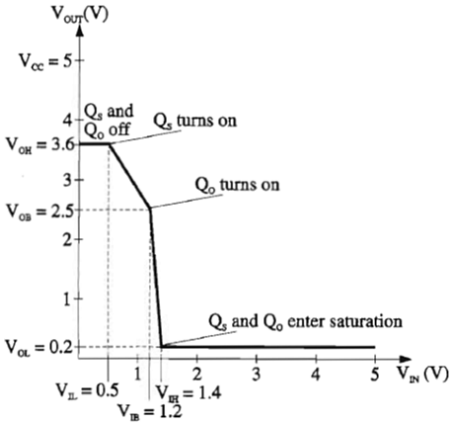
- When the input voltage is high enough, i.e., $V_{IN} = V_{BE,S(FA)} - V_{CE,I(SAT)}$, Q_S goes into the forward active (FA) mode and current I_{RC} will start to flow. Then, V_{OUT} starts to drop with increasing V_{IN} as $V_{OUT} = V_{CC} - I_{RC}R_C - V_{BE,P(EOC)} - V_{D,L(EOC)}$.
- If we increase V_{IN} further, then at some point (i.e., when $V_{IN} = V_{BE,O(FA)} + V_{BE,S(FA)} - V_{CE,I(SAT)}$), Q_O turns into forward active mode. As a result, V_{OUT} decreases more rapidly as $I_{C,O}$ also starts to flow and more current starts to flow from R_C. This point is called the **break point**. The input and output voltages at the break point are labelled as V_{IB} and V_{OB}, respectively.





- If V_{IN} is kept increasing, then at some point (i.e., when $V_{IN} = V_{BE,O(SAT)} + V_{BE,S(SAT)} - V_{CE,I(SAT)}$), both Q_S and Q_O go into the saturation mode, Q_P goes into cutoff mode and Q_I goes into the reverse-active mode. As a result, V_{OUT} becomes LOW and remains constant at $V_{OUT} = V_{CE,O(SAT)}$.

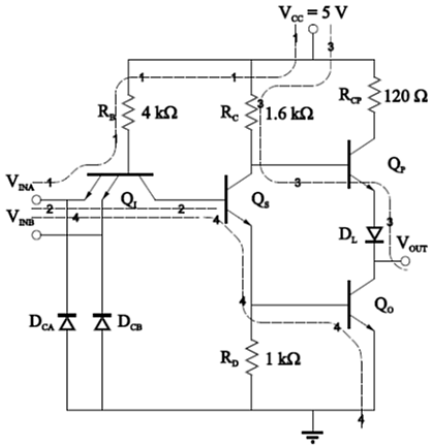


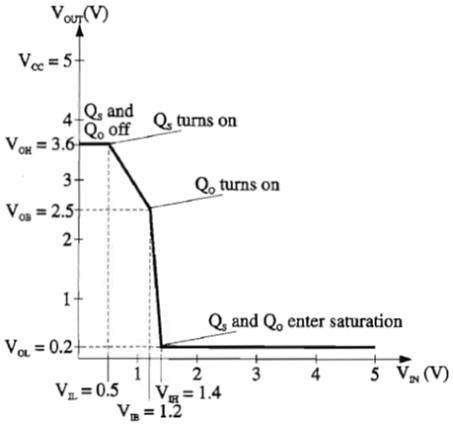


- The states of active elements in a standard TTL inverter are given in the table below.

State of Active Elements for Output-High and Output-Low States

Element	V_{OH}	V_{OB}	V_{OL}
Q_O	Cutoff (OFF)	Edge of conduction (EOC)	Saturated (SAT)
Q_S	Cutoff (OFF)	Forward active (FA)	Saturated (SAT)
Q_I	Saturated (SAT)	Saturated (SAT)	Reverse active (RA)
Q_P	Edge of conduction (EOC)	Edge of conduction (EOC)	Cutoff (OFF)
D_L	Edge of conduction (EOC)	Edge of conduction (EOC)	Cutoff (OFF)





- Thus,

$$V_{OH} = V_{CC} - V_{BE,P(FA)} - V_{D,L(ON)}$$

$$V_{OB} = V_{CC} - I_{C,S(FA)} R_C - V_{BE,P(FA)} - V_{D,L(ON)}$$

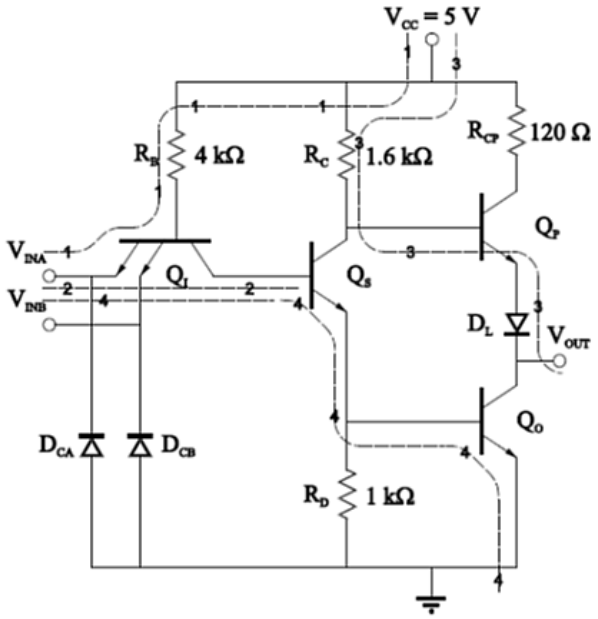
$$= V_{CC} - \frac{V_{BE,O(FA)}}{R_D} R_C - V_{BE,P(FA)} - V_{D,L(ON)}$$

$$V_{OL} = V_{CE,O(SAT)}$$

$$V_{IL} = V_{BE,S(FA)} - V_{CE,I(SAT)}$$

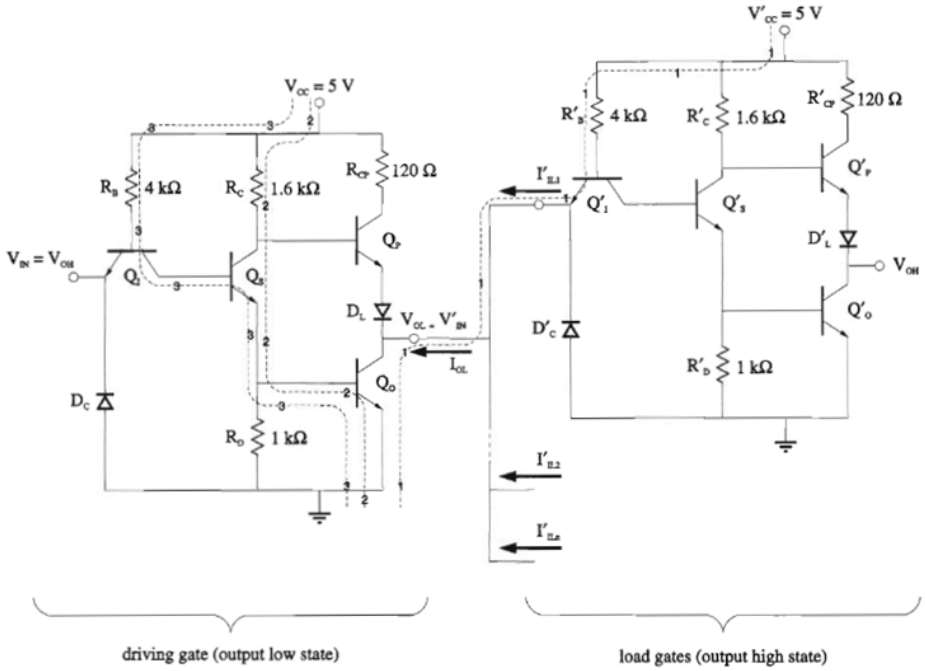
$$V_{IB} = V_{BE,O(FA)} + V_{BE,S(FA)} - V_{CE,I(SAT)}$$

$$V_{IH} = V_{BE,O(SAT)} + V_{BE,S(SAT)} - V_{CE,I(SAT)}$$



Example 1: For the TTL gate above, determine the VTC critical points V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_{IB} and V_{OB} for $\beta_F = 100$ and $\sigma_{\text{max}} = 0.85$.

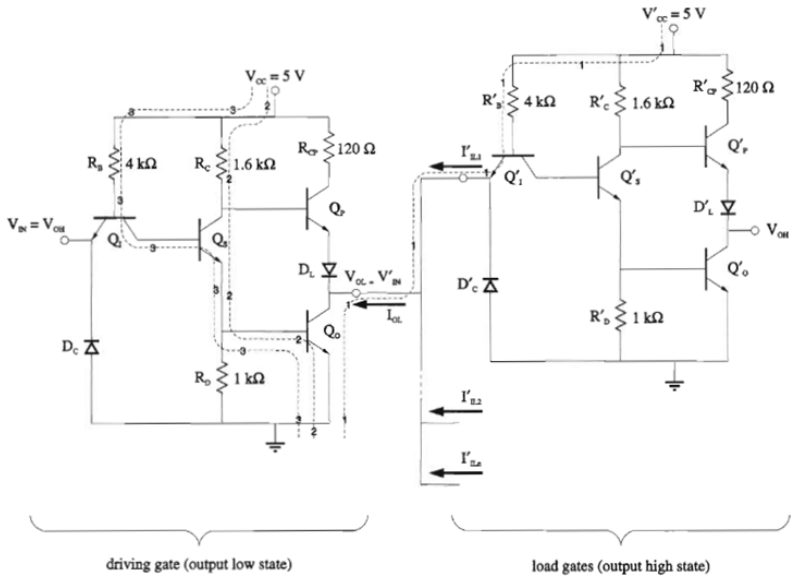
TTL Fan-Out



- Maximum fan-out will be determined by the **output-low** state, as when output is high input transistor Q'_I is in reverse active mode (i.e., $I'_{IH} = 0$).
- From Path 1,

$$I_{OL} = I_{C,O(SAT)} - I_{D,L(EOC)} = I_{C,O(SAT)}$$

$$I_{C,O(SAT)} = \sigma\beta_F I_{B,O(SAT)}$$



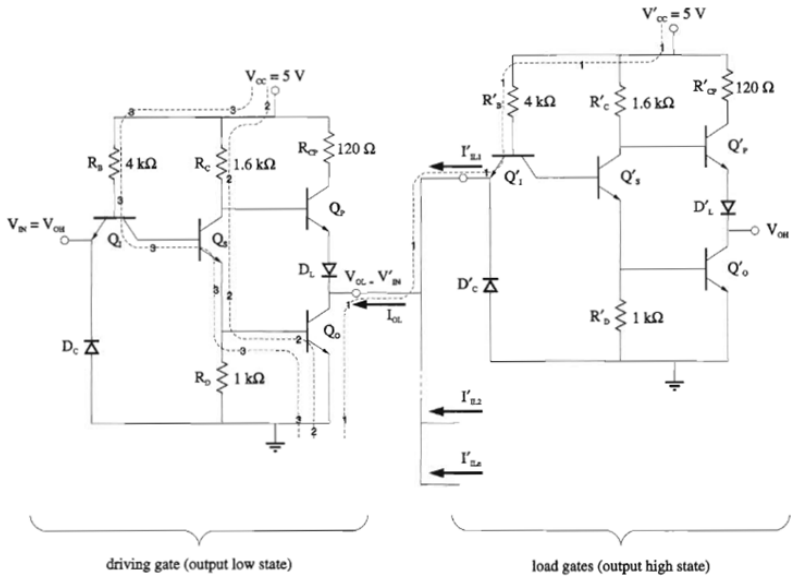
- Continuing

$$I_{B,O(SAT)} = I_{E,S(SAT)} - I_{RD(OL)}$$

$$I_{RD(OL)} = \frac{V_{BE,O(SAT)}}{R_D}$$

$$I_{E,S(SAT)} = I_{C,S(SAT)} + I_{B,S(SAT)}$$

$$I_{C,S(SAT)} = \frac{V_{CC} - V_{CE,S(SAT)} - V_{BE,O(SAT)}}{R_C} \qquad \text{(from Path 2)}$$



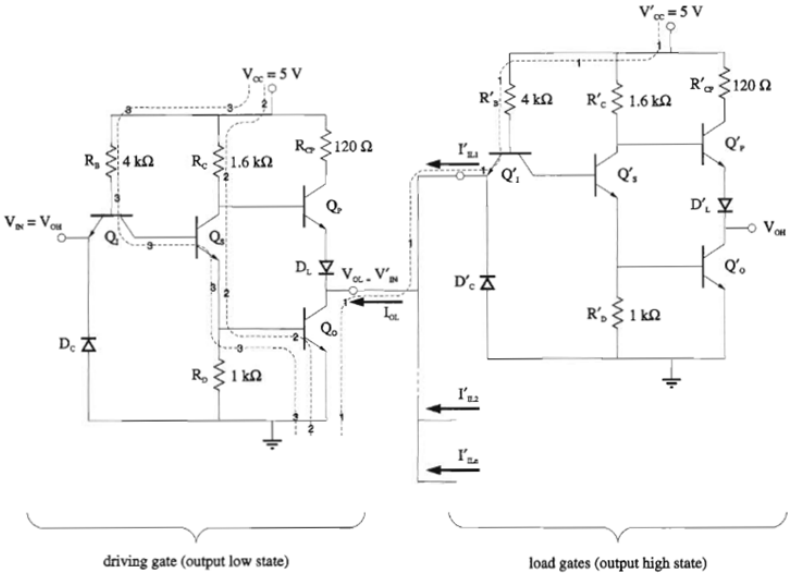
- From Path 3,

$$I_{B,S(SAT)} = I_{C,I(RA)}$$
$$= (1 + \beta_R) I_{B,I(RA)}$$

$$I_{B,I(RA)} = \frac{V_{CC} - V_{BC,I(RA)} - V_{BE,S(SAT)} - V_{BE,O(SAT)}}{R_B}$$

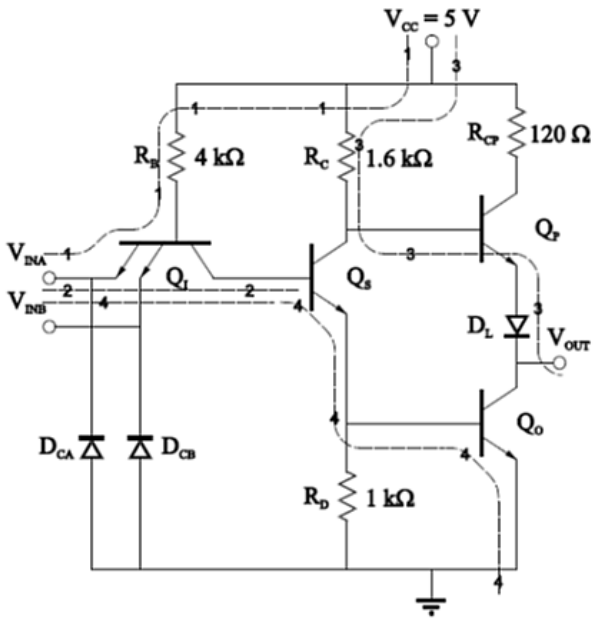
- From Path 1,

$$I'_{IL} = \frac{V_{CC} - V_{BE,I(SAT)} - V_{CE,O(SAT)}}{R_B}$$



- Thus, the **maximum fan-out** is given by

$$N_{\text{max}} = \left\lfloor \frac{I_{OL(\text{max})}}{I'_{IL}} \right\rfloor = \left\lfloor \frac{I_{C,O(SAT)(\text{max})}}{I'_{IL}} \right\rfloor$$
$$= \left\lfloor \frac{\sigma_{\text{max}} \beta_F I_{B,O(SAT)}}{I'_{IL}} \right\rfloor$$

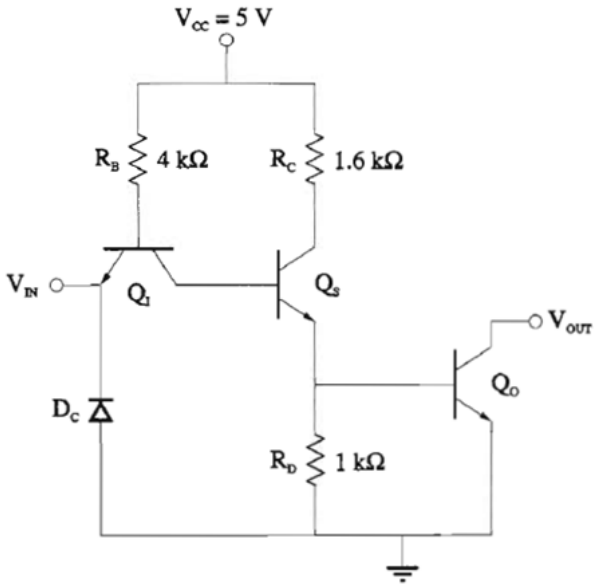


Example 2: For the TTL gate above, determine the maximum fan-out for $\beta_F = 25$, $\beta_R = 0.1$ and $\sigma_{\text{max}} = 0.85$.

TTL Power Dissipation

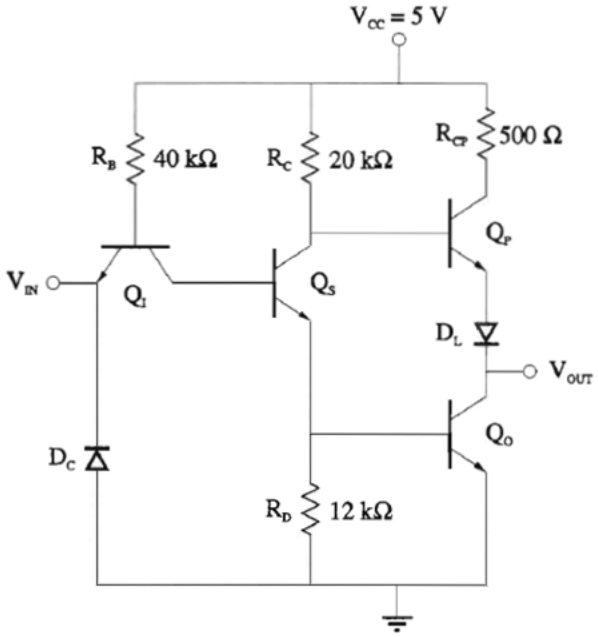
Example 3: Calculate the average power dissipation for Example 2 above?

Open-Collector TTL

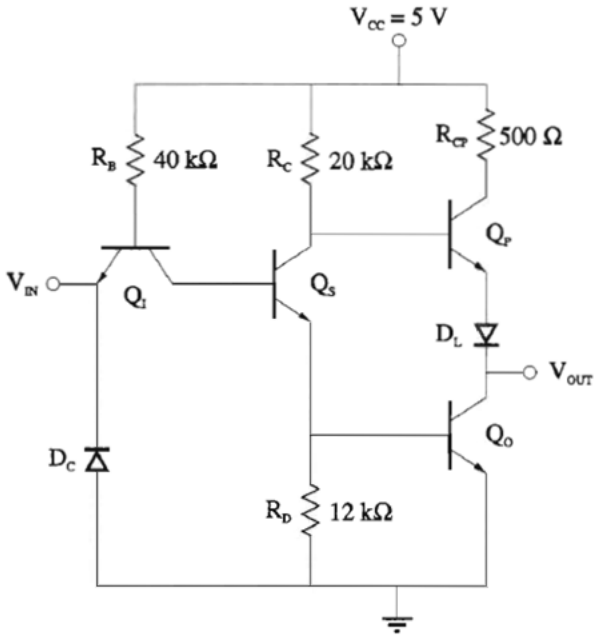


- Open-collector TTL gates, one of which is shown in the figure above, are often used in data busses where multiple gate outputs must be ANDed.
  - This can be accomplished by using a single pull-up resistor with open-collector TTL gates.
  - This type of connection is referred to as **wired-AND**.

Low Power TTL (LTTL)

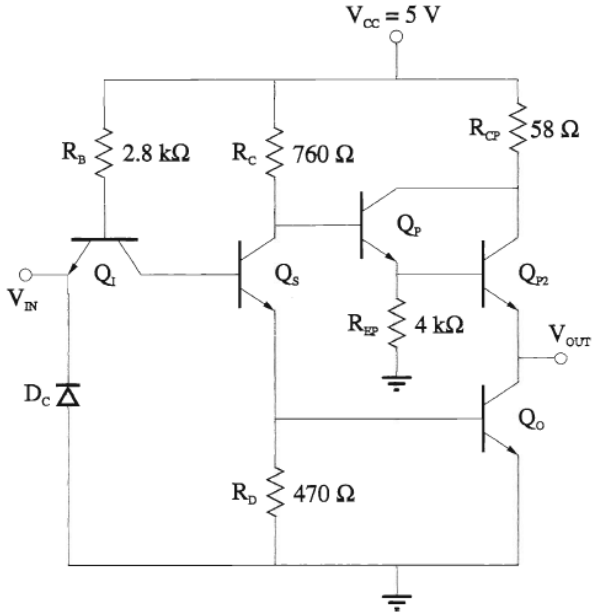


- Power dissipation can be lowered by just **increasing** the **resistance** values as shown in the figure above.
- However, this results in:
  - decreased fan-out,
  - longer transient response times.



Example 4: Calculate the average power dissipation for LTTL in the figure above and compare it with that of TTL which was calculated in Example 3.

High Speed TTL (HTTL)



- Switching speed can be increased by just **decreasing** the **resistance** values as shown in the figure above. An additional Darlington pair is also used to improve the low-to-high switching speed, together with R_{EP} resistor which provides a discharge path for Q_{P2} in order to improve the high-to-low switching speed.
- However, this results in
  - increased power dissipation.

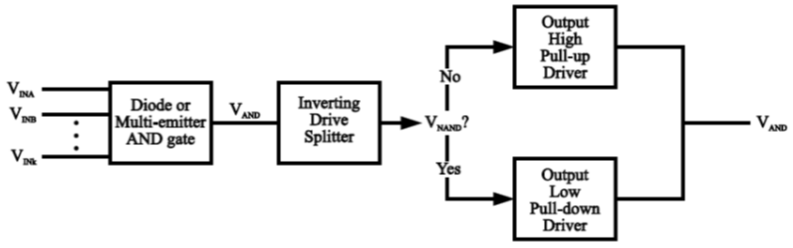
Other TTL Gates

In this section, we are going to investigate the following TTL gates

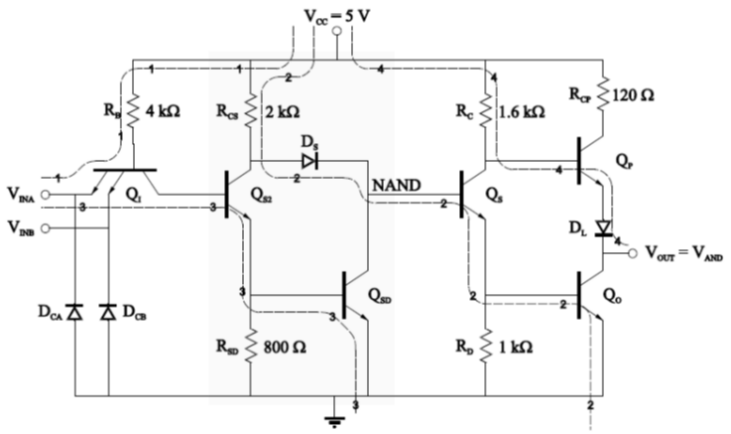
- AND gates
- NOR gates
- OR gates
- AND-OR-INVERT (AOI) gates
- XOR gates
- Schmitt Trigger Inverters and NAND gates
- Tri-State buffers

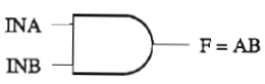
AND Gate

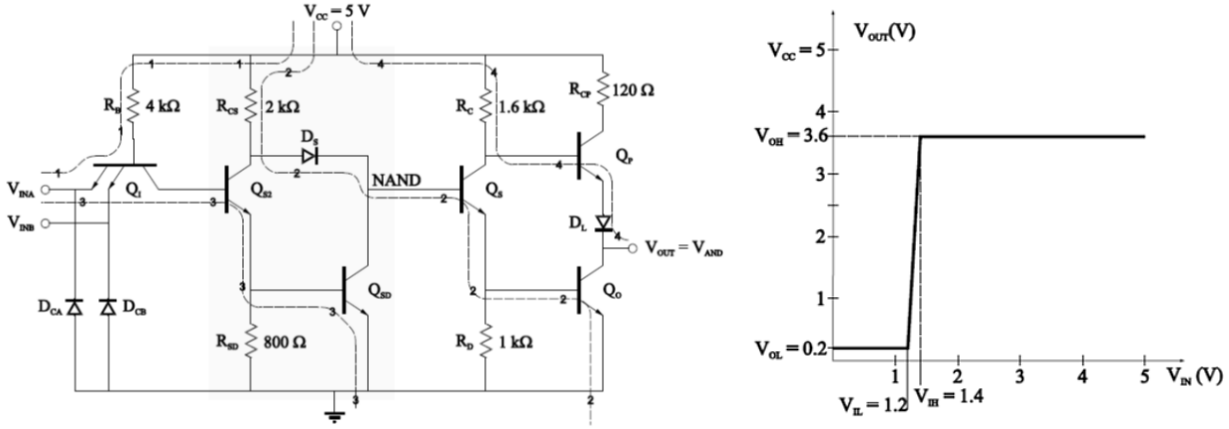
- NAND gate will become an AND date, if the output drivers are enabled in the inverse fashion. This is accomplished by using an **inverting driver splitter** as shown in the block diagram of the figure below.



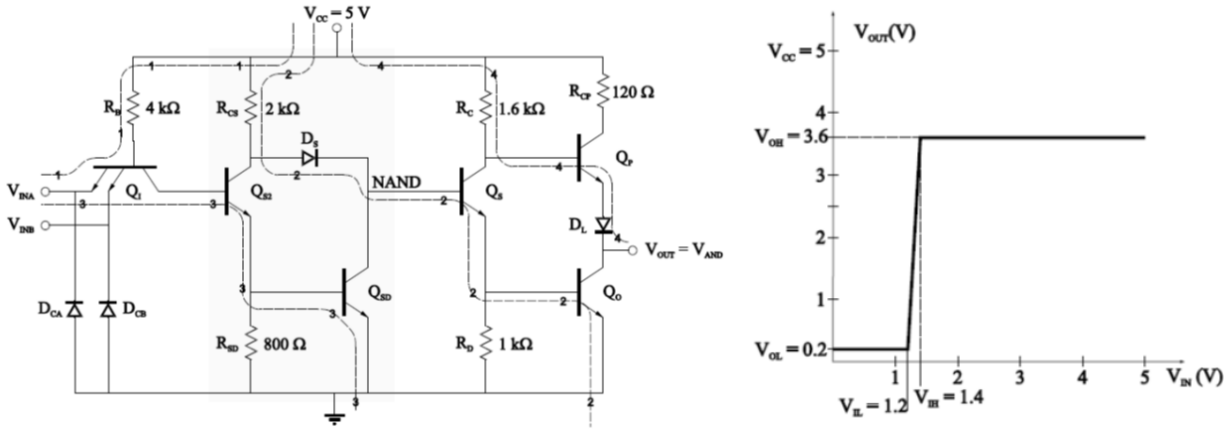
- This second level inversion is accomplished by Q_{S2}, Q_{SD}, D_S, R_{SD} and R_{CS} which are enclosed in the shaded block in the figure on the left below.







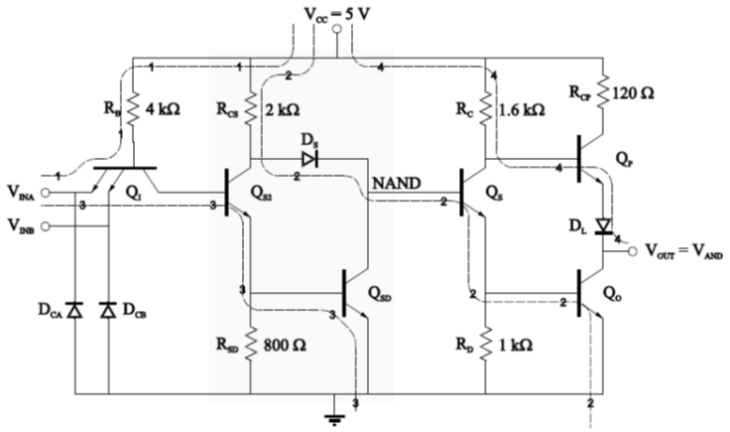
- When the input is low, e.g., $V_{IN} = 0\,\text{V}$, Q_I is saturated, Q_{S2} and Q_{SD} are cutoff. Consequently, Q_S and Q_O are saturated, and Q_P and D_L are cutoff. So, the output is LOW, i.e., $V_{OL} = V_{CE,O(SAT)}$.
- The output will start increase when Q_O goes from saturation mode to forward active mode. Only Q_{S2} being in forward active mode is not enough to decrease the voltage at the base of Q_S below $1.6\,\text{V}$ and change the state of Q_O. So, Q_{SD} needs to go into forward active mode as well. Thus, the value of the input to make the output rise is equal to $V_{IL} = V_{BE,SD(FA)} + V_{BE,S2(FA)} - V_{CE,I(SAT)}$.
- Q_S will turn off when the voltage at its base goes below $0.7\,\text{V}$ and this will occur suddenly when Q_{SD} and Q_{S2} go into saturation. Thus, the value of the input which makes the output high is given by $V_{IH} = V_{BE,SD(SAT)} + V_{BE,S2(SAT)} - V_{CE,I(SAT)}$. Then, Q_I goes into reverse active mode and the output stays high.

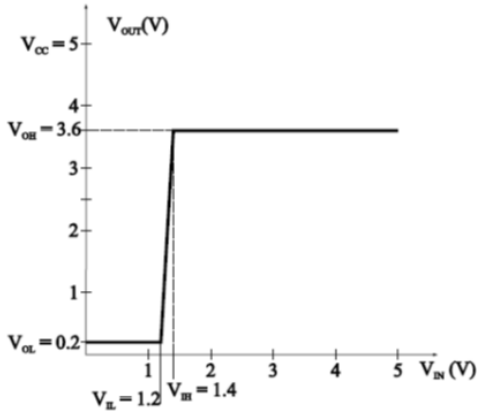


- The states of active elements in a standard TTL noninverter are given in the table below.

State of Active Elements for Output-High and Output-Low States

Element	V_{OL}	V_{OH}
Q_O	Saturated (SAT)	Cutoff (OFF)
Q_S	Saturated (SAT)	Cutoff (OFF)
Q_P	Cutoff (OFF)	Edge of conduction (EOC)
D_L	Cutoff (OFF)	Edge of conduction (EOC)
Q_{SD}	Cutoff (OFF)	Saturated (SAT)
Q_{S2}	Cutoff (OFF)	Saturated (SAT)
D_S	Conducting (ON)	Conducting (ON)
Q_I	Saturated (SAT)	Reverse active (RA)



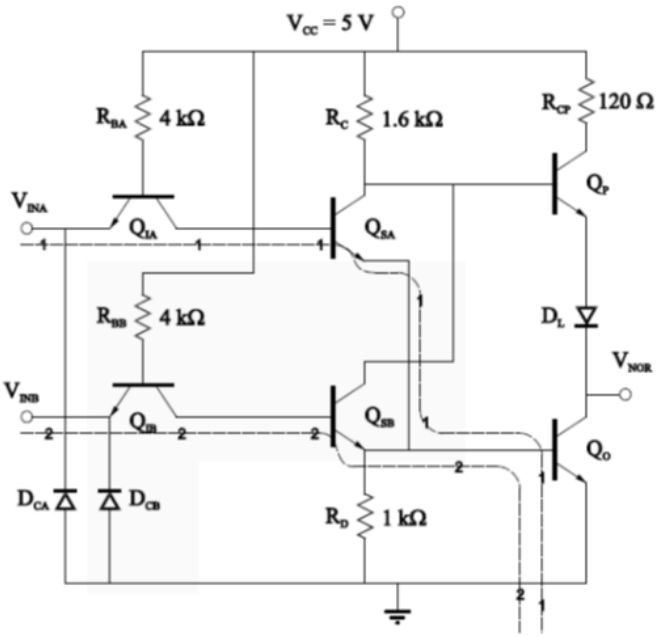


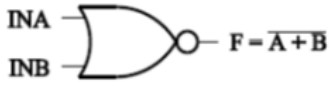
- A *knee* is not present in the VTC of the TTL AND gate in contrast to the VTC of the TTL NAND gate, and the transition region is more abrupt. Thus,

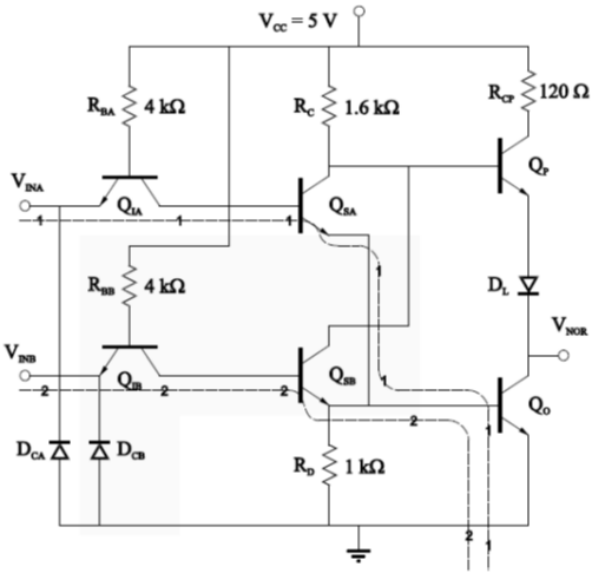
$$V_{OL} = V_{CE,O(SAT)}$$
$$V_{OH} = V_{CC} - V_{BE,P(FA)} - V_{D,L(ON)}$$
$$V_{IL} = V_{BE,SD(FA)} + V_{BE,S2(FA)} - V_{CE,I(SAT)}$$
$$V_{IH} = V_{BE,SD(SAT)} + V_{BE,S2(SAT)} - V_{CE,I(SAT)}$$

NOR Gate

- NOR function is obtained by using separate input sections Q_I, R_B and Q_S for the inputs where drive splitter transistors are connected in parallel (i.e., their collectors and emitters are connected together) as shown in the figure on the left below. Circuit symbol for the NOR gate is also displayed in the figure on the right below.





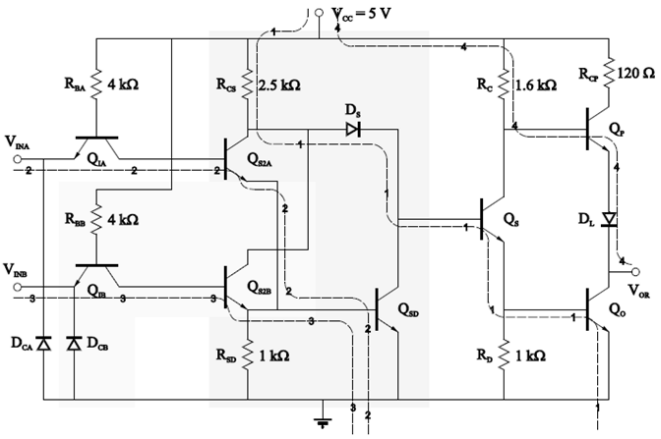


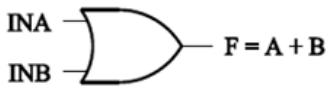
Example 5: For the two input TTL NOR gate above, determine the average power dissipation and compare the result with that of a standard TTL inverter calculated in Example 3.

NOTE: You need to consider all four possible input states.

OR Gate

- OR function is obtained by using separate input sections and parallel drive splitter transistors of the second lvel inversion circuitry as shown in the figure on the left below. Circuit symbol for the OR gate is also displayed in the figure on the right below.





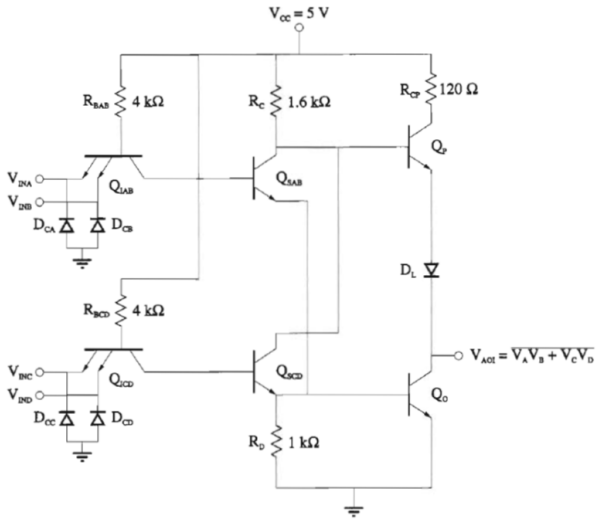
AND-OR-INVERT (AOI) Gates

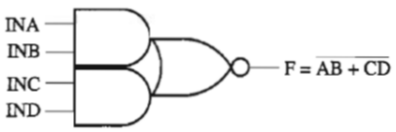
TTL gates performing more complex logic functions can be designed using the following rules

1. ANDing of signals
   - Multi-emitter input BJT sections
2. ORing of signals
   - Multiple input sections (Q_I and R_B)
   - Multiple and parallel connected drive splitting BJTs (Q_S)
3. If non-inverting ORing is desired
   - Additional logic inversion circuitry with parallel connected drive splitting BJTs
4. Totem-pole output branch

Example 6: Design a four-input AOI TTL gate which performs $V_{OUT} = \overline{V_A V_B + V_C V_D}$.

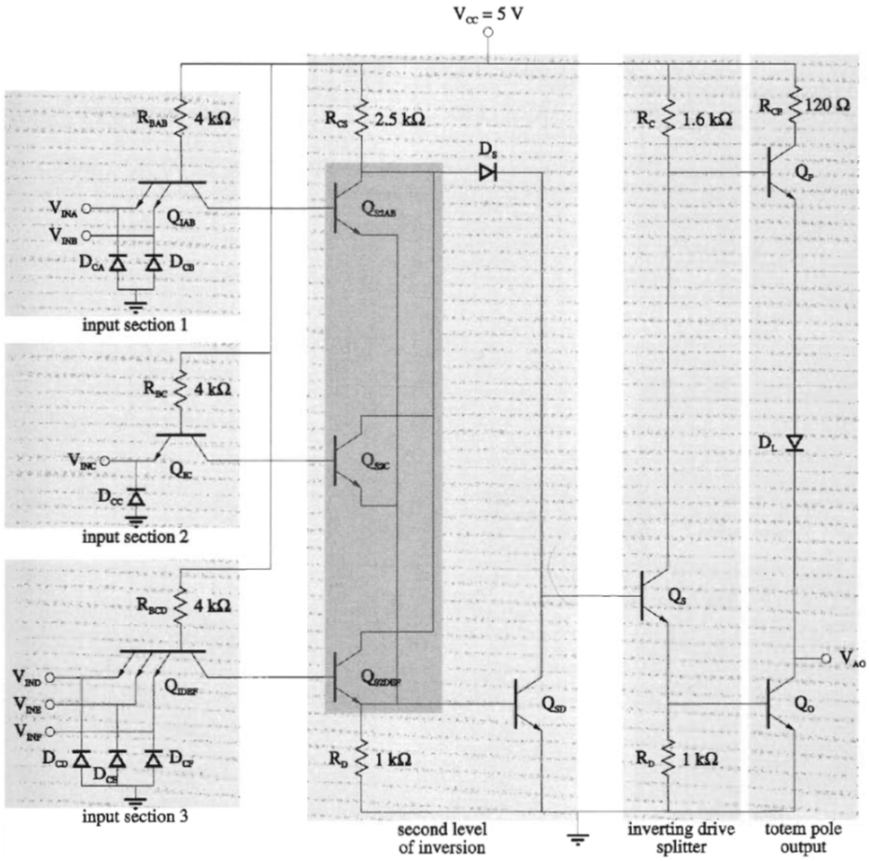
Solution:





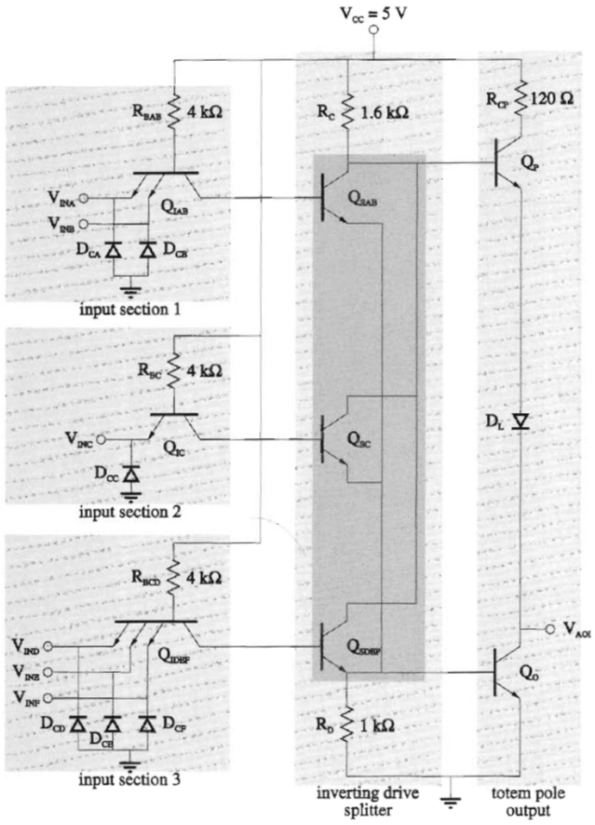
Example 7: Design a six-input AOI TTL gate which performs $V_{OUT} = V_A V_B + V_C + V_D V_E V_F$.

Solution:

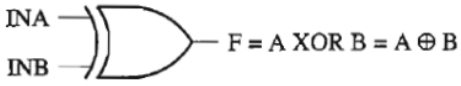


Example 8: Design a six-input AOI TTL gate which performs $V_{OUT} = \overline{V_A V_B + V_C + V_D V_E V_F}$.

Solution:



XOR Gate



- Circuit symbol and truth table for an XOR gate are given in the figure above and the table below, respectively.

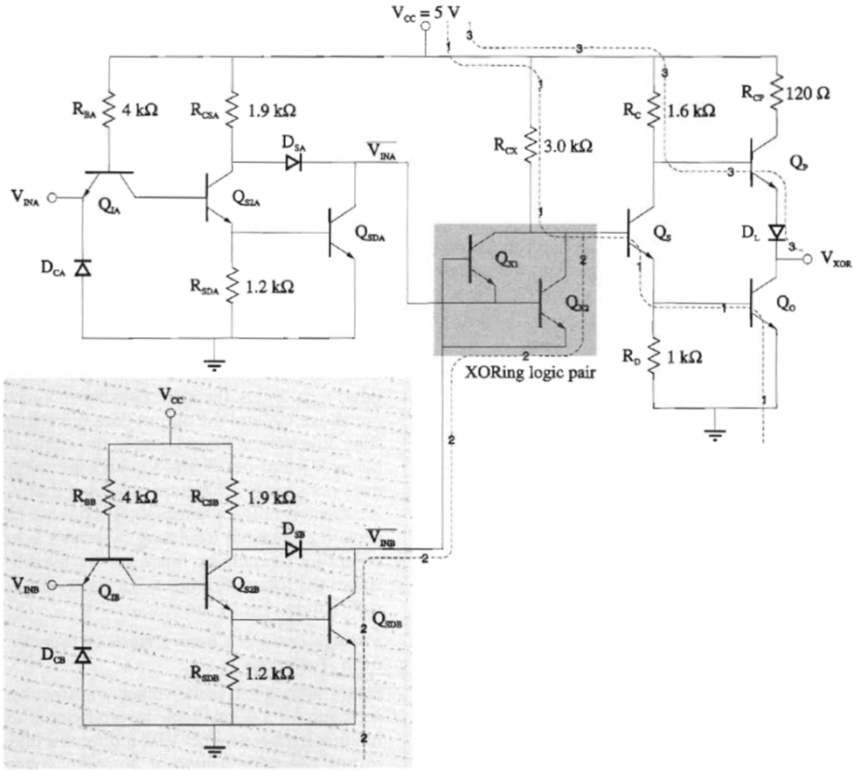
Truth Table for an XOR Gate

V_{INA}	V_{INB}	V_{OUT}
LOW	LOW	LOW
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

- As we notice, the output is LOW when the inputs are the same, and HIGH when the inputs are different.
- Also, the outputs will be the same, even when the inputs are inverted, i.e,

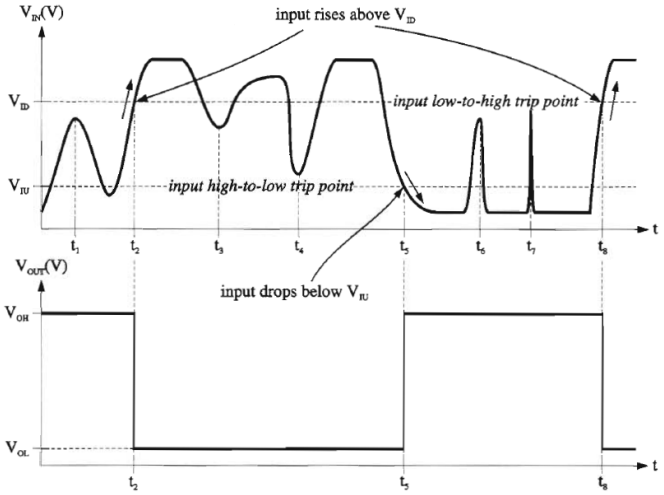
$$F = A \oplus B = \overline{A} \oplus \overline{B}$$

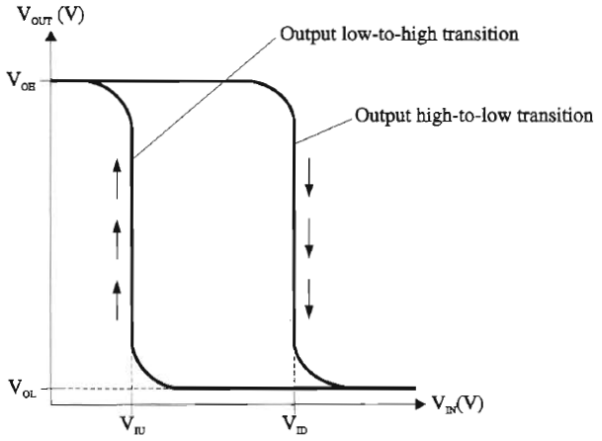
- We can form an **XORing logic pair** using two transistors: by connecting one input to the base of the first transistor and to the emitter of the second transistor, and connecting the other input to the base of the second transistor and to the emitter of the first transistor where the collectors of the transistors are connected together, as shown in the figure below.



Schmitt Trigger Inverters and NAND Gates

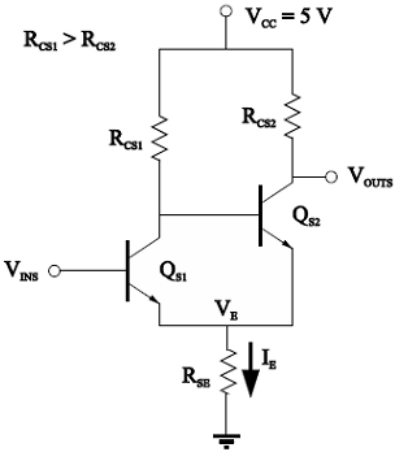
- Consider a noisy signal, shown at the top of the figure on the left below, as an input to an inverter gate. We need to produce a neat inverter output signal considering the input is LOW before t_2, HIGH between t_2 and t_3, LOW between t_5 and t_8 and HIGH after t_8, as shown at the bottom of the figure on the left below.

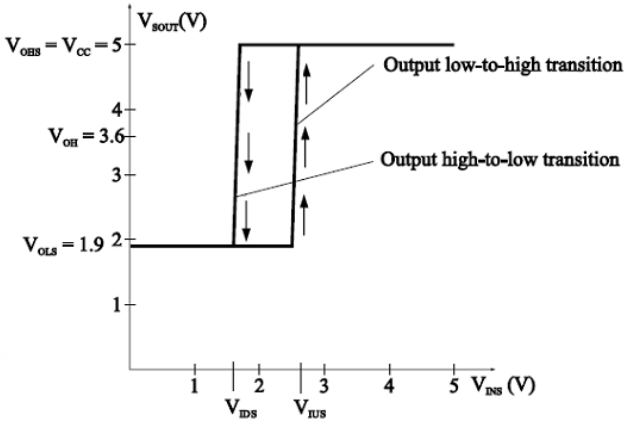




- As seen from the figure on the right above, VTC exhibits **hysteresis**, i.e., low-to-high path is not the same as the high-to-low path of the input-output relationship.

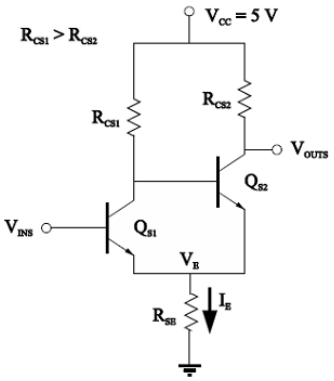
Basic Emitter-Coupled Schmitt Trigger Noninverter

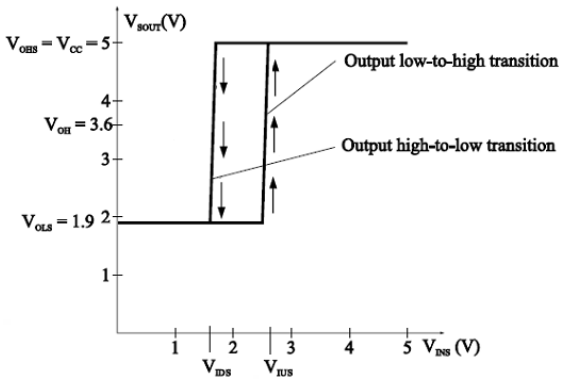




- Hysteresis can be achieved by the basic emitter-coupled noninverting Schmitt Trigger circuit shown in the figure on the left above.
- Let us first investigate, low-to-high path of the input. When input is LOW, e.g., $V_{INS} = 0$V, then Q_{S1} is cutoff and Q_{S2} is in saturation. Thus, the output is LOW, i.e., $V_{OUTS} = V_{OLS} = V_E + V_{CE,S2(SAT)}$. So, $I_{E,S2} = I_{B,S2} + I_{C,S2}$, i.e.,

$$\frac{V_E}{R_{SE}} = \frac{V_{CC} - V_E - V_{BE,S2(SAT)}}{R_{CS1}} + \frac{V_{CC} - V_E - V_{CE,S2(SAT)}}{R_{CS2}}$$





- We find V_E as

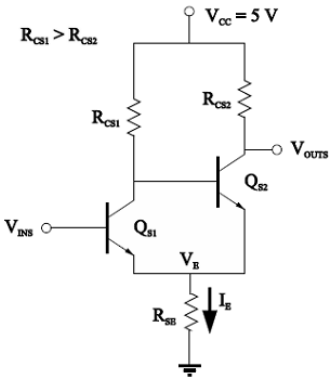
$$V_E = \left(\frac{V_{CC} - V_{BE,S2(SAT)}}{R_{CS1}} + \frac{V_{CC} - V_{CE,S2(SAT)}}{R_{CS2}} \right) R_{eq}$$

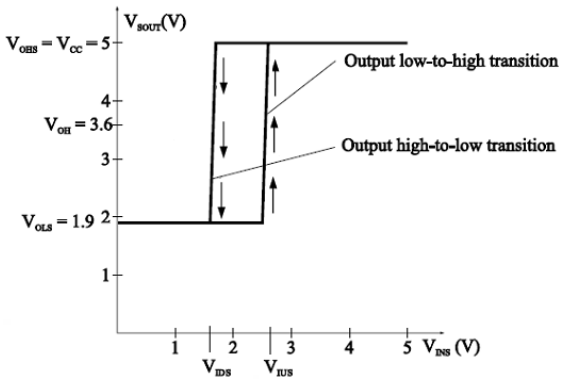
where $R_{eq} = R_{CS1} || R_{CS2} || R_{SE}$.

- Thus, V_{OLS} is given by

$$V_{OLS} = \left(\frac{V_{CC} - V_{BE,S2(SAT)}}{R_{CS1}} + \frac{V_{CC} - V_{CE,S2(SAT)}}{R_{CS2}} \right) R_{eq} + V_{CE,S2(SAT)}$$

- As, we keep increasing the input, eventually Q_{S1} will become forward active at an input voltage $V_{INS} = V_{IUS} = V_E + V_{BE,S1(FA)}$. Then, V_E will increase and V_{OUTS} will start to rise.





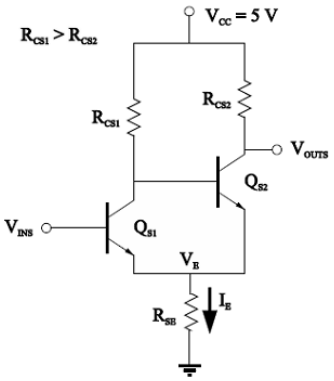
- Thus, V_{IUS} is given by

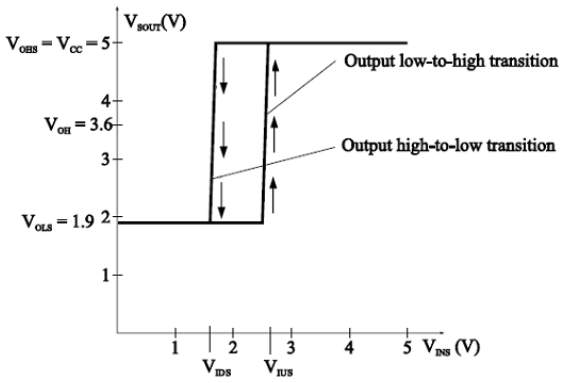
$$V_{IUS} = \left(\frac{V_{CC} - V_{BE,S2(SAT)}}{R_{CS1}} + \frac{V_{CC} - V_{CE,S2(SAT)}}{R_{CS2}} \right) R_{eq} + V_{BE,S1(FA)}$$

- Once the input is further increased, voltage at Q_{S1} will go into saturation and Q_{S2} will turn off. Then, the output voltage will become HIGH at $V_{OUTS} = V_{OHS} = V_{CC} - I_{RCS2} R_{CS2}$. But, as there is no load $I_{RCS2} = 0$ and

$$V_{OHS} = V_{CC}$$

Now we can investigate the high-to-low path of the input. In this case Q_{S2} is cutoff and Q_{S1} is in saturation. The output will fall when Q_{S2} becomes forward active, i.e., when $V_{BE,S2} = V_{BE(FA)}$.



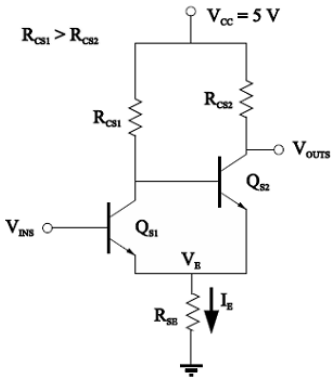


- As $V_E = V_{INS} - V_{BE,S1(SAT)}$, $V_{BE,S2} = V_{B,S2} - V_E$, $V_{B,S2} = V_{CC} - I_{C,S1}R_{CS1}$ and $I_{C,S1} \approx I_{E,S1} = V_E/R_{SE}$, we can obtain the input in terms of $V_{BE,S2}$ as

$$V_{INS} = \frac{V_{CC} - V_{BE,S2}}{R_{CS1}/R_{SE} + 1} + V_{BE,S1(SAT)}$$

- As the output will start to drop when Q_{S2} turns on, i.e., when $V_{BE,S2} = V_{BE(FA)}$, then we can find V_{IDS} as

$$V_{IDS} = \frac{V_{CC} - V_{BE,S2(FA)}}{R_{CS1}/R_{SE} + 1} + V_{BE,S1(SAT)}$$



Example 9: For the Schmitt Trigger noninverter circuit above, determine the V_{OHS}, V_{OLS}, V_{IUS} and V_{IDS} values where $R_{CS1} = 4\,\text{k}\Omega$, $R_{CS2} = 2.5\,\text{k}\Omega$, and $R_{SE} = 1\,\text{k}\Omega$.

Solution: As $R_{eq} = R_{CS1}||R_{CS2}||R_{SE} = 606\,\Omega$,

$$V_{OHS} = 5\,\text{V}$$

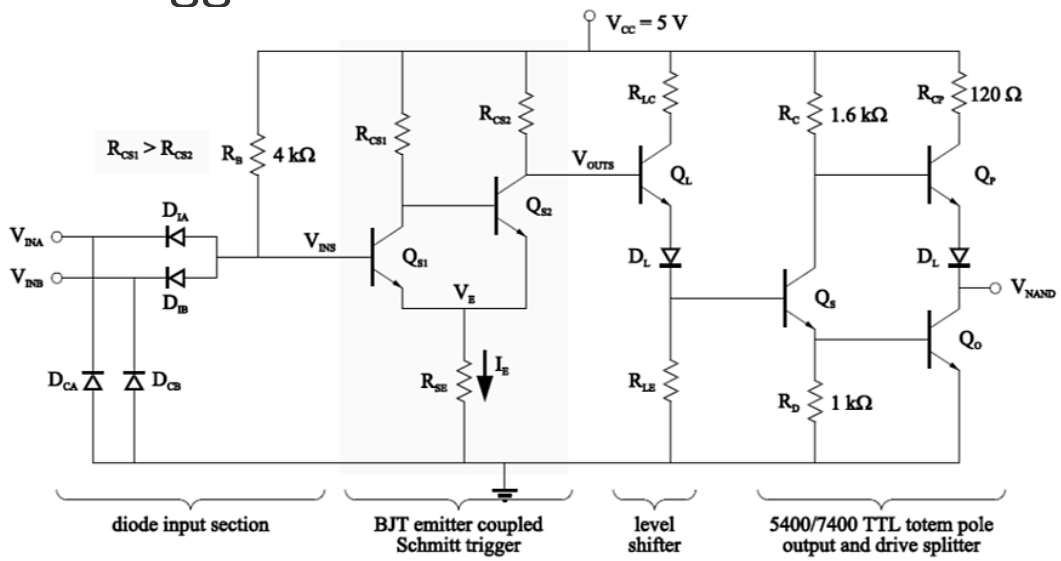
$$V_{E,S2(SAT)} = \left(\frac{V_{CC} - V_{BE,S2(SAT)}}{R_{CS1}} + \frac{V_{CC} - V_{CE,S2(SAT)}}{R_{CS2}}\right) R_{eq} = 1.8\,\text{V}$$

$$V_{OLS} = V_{E,S2(SAT)} + V_{CE,S2(SAT)} = 2\,\text{V}$$

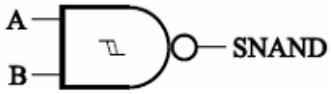
$$V_{IUS} = V_{E,S2(SAT)} + V_{BE,S1(FA)} = 2.5\,\text{V}$$

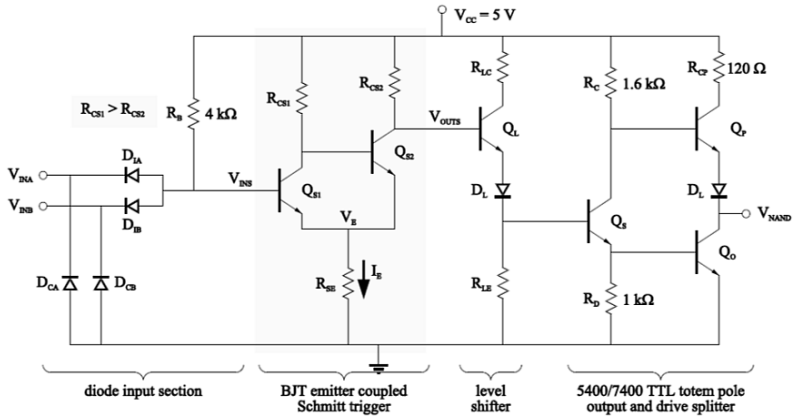
$$V_{IDS} = \frac{V_{CC} - V_{BE,S2(FA)}}{R_{CS1}/R_{SE} + 1} + V_{BE,S1(SAT)} = 1.66\,\text{V}$$

Schmitt Trigger NAND Gate

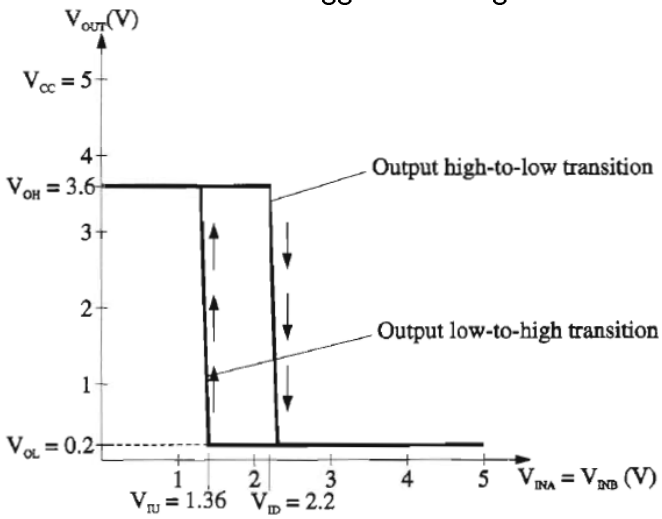


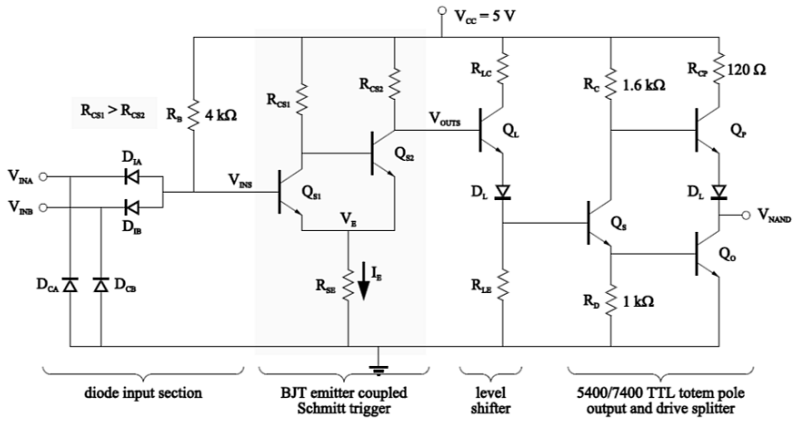
- We can convert the basic emitter-coupled Schmitt Trigger noninverter to a TTL compatible Schmitt Trigger NAND gate by connecting and ANDing diode section at the input and by adding a emitter-follower level shifter section with Q_L and D_L followed by a normal inverting driver splitter connected a totem-pole output section at the output, as shown in the circuit above.
- Circuit symbol for a Schmitt Trigger NAND gate is shown below.





- An example VTC for a standard Schmitt Trigger NAND gate is shown below.





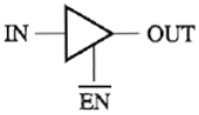
Example 10: For the Schmitt Trigger NAND circuit above, determine the V_{OH}, V_{OL}, V_{IU} and V_{ID} values where $R_{CS1} = 4\,\text{k}\Omega$, $R_{CS2} = 2.5\,\text{k}\Omega$, and $R_{SE} = 1\,\text{k}\Omega$.

HINT: Use the results in Example 9.

Solution:

$$V_{OH} = V_{CC} - V_{BE,P(FA)} - V_{D,L(ON)} = 3.6\,\text{V}$$
$$V_{OL} = V_{CE,O(SAT)} = 0.2\,\text{V}$$
$$V_{ID} = V_{IUS} - V_{D,I(ON)} = 1.8\,\text{V}$$
$$V_{IU} = V_{IDS} - V_{D,I(ON)} = 0.96\,\text{V}$$

Tri-State Buffers



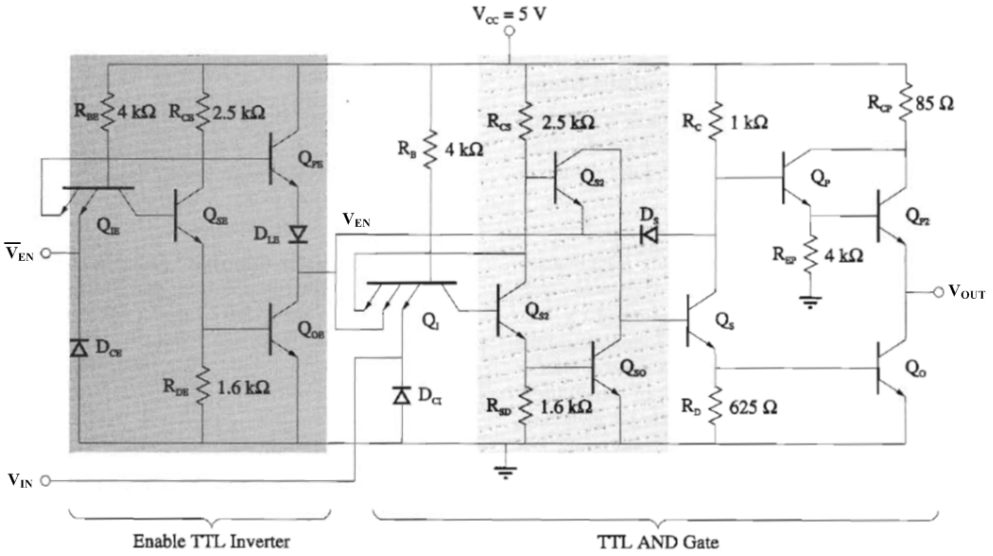
- Circuit symbol and truth table for a low-enabled tri-state buffer (or noninverter) are given in the figure above and the table below, respectively.

Truth Table for a Low-Enabled Tri-State Buffer

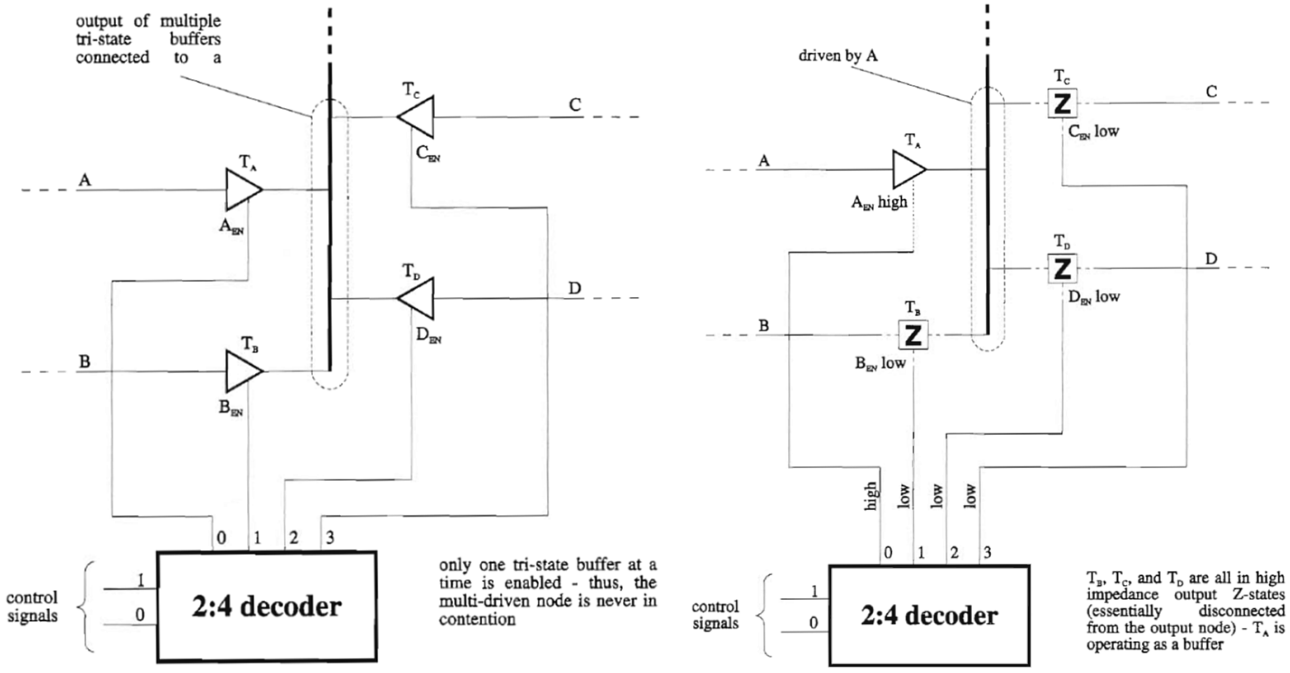
V_{IN}	$\overline{V_{EN}}$	V_{OUT}
LOW	LOW	LOW
HIGH	LOW	HIGH
LOW	HIGH	HIGH IMPEDANCE (Z)
HIGH	HIGH	HIGH IMPEDANCE (Z)

- High impedance Z-state nodes are floating, i.e., **not connected**. So, high impedance Z-state nodes are **not** at ground, **not** at V_{CC} and have **no** driving ability.

Tri-State Buffers



- Enable-disable functionality is basically achieved by connecting a diode D_S to the enable input of Q_I which is also ANDed together with the actual input.
  - When V_{EN} is HIGH, D_S is OFF. So, the circuit operates like a normal noninverter and output is determined by the input V_{IN}.
  - When V_{EN} is LOW, Q_S and Q_O are OFF due to AND operation, and D_S is also ON. As D_S is ON, voltage at the base of Q_P drops to $V_{EN} + V_{D,S(ON)}$ which is not high enough to turn on Q_{P2}. So, both Q_O are Q_{P2} are OFF, and output V_{OUT} is not connected to pull-up or pull-down drivers regardless of the value of the input V_{IN}.



- Figure on the left above shows an example of four tri-state buffers connected to a single bus. Figure on the right above shows how to enable a single buffer at a time using a 2:4 decoder, e.g., acting as a 4-to-1 multiplexer with two select inputs.

- Tri-state buffers are often used to drive multi-bit circuit busses as shown in the figure below.