INTRODUCTION

- Cochlear implants (CIs) are commonly accepted as therapeutic devices for clinical use and have restored hearing to more than 736,900 profoundly deaf people all around the world.
- They are complex electronic devices surgically implanted under the skin behind the ear. These devices use electrodes placed in the inner ear (the cochlea) to stimulate the auditory nerve of individuals.
- Aim of this project is to design a low-power cochlear implant chip at both schematic and layout level.

SPECIFICATIONS AND DESIGN REQUIREMENTS

- Equalizer circuit have 12 outputs with frequencies covering from 20Hz to 20kHz.
- Chip size arranged according to the SMD Package
- 3.3 V Supply
- 180 nm Technology
- 20 dB Dynamic Range
- Low Power Consumption

SOLUTION METHODOLOGY

CHIP DESIGNS AND SIMULATION RESULTS

- Internal and external chips which consist of all the circuits in the design, are sized according to the SMD package.
- Pins are determined according to system requirements. Floorplanning and pin configuration techniques are also taken into account.

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